For a PHY that includes an FEC functionand/or a PCS lane distribution function, the transmit and receive path data delays ~~may~~can show significant variation depending ~~upon the position of the within the FEC~~on how the packet's DDMP aligns to an FEC codeword and/or to a PCS lane distribution sequence. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the SFD DDMP is at the start of the FEC codeword and/or at the start of the PCS lane distribution sequence (when the multilane ability (3.1800.11) bit is set -- see 45.2.3.67.3). For example, for many PHYs with both FEC and PCS lane distribution, the start of anthe FEC ~~block~~codeword necessarily coincides with the start of a PCS lane distribution sequence periodically during their respective processions. This results in the maximum FEC and the maximum PCS lane distribution delays being allocated to the PHY TX and the minimum FEC and the minimum PCS lane distribution delays being allocated to the PHY RX. See 90A.7 for more information on the cascading delays of multiple functions.¶