Channel Capacity Calculator

Version 1.3

Ragnar Jonsson

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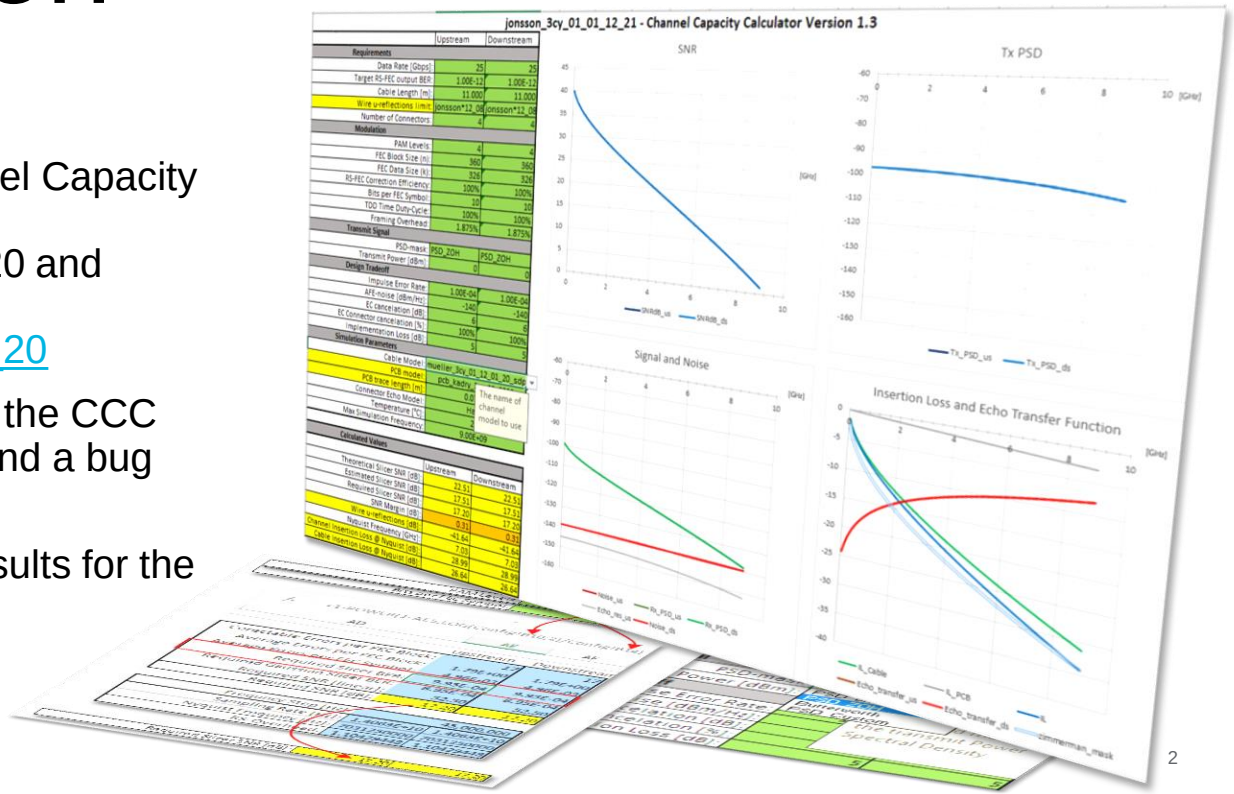
802.3cy

Introduction

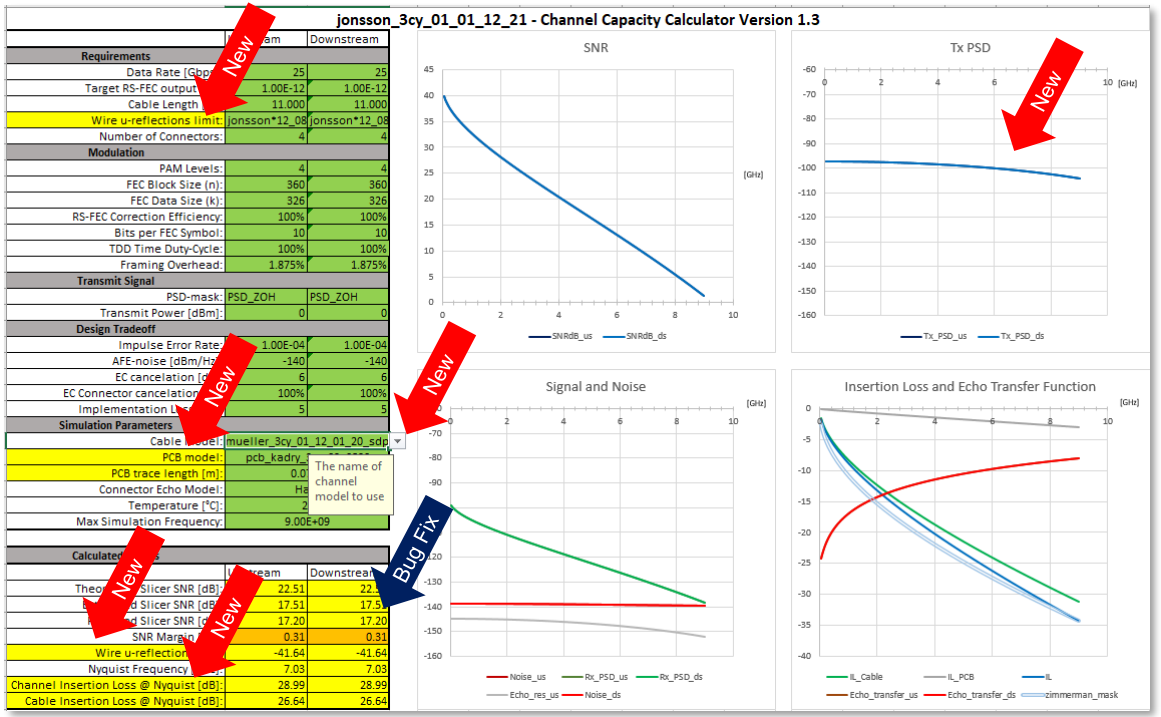
- We introduced the Channel Capacity Calculator (CCC) tool in jonsson_3cy_01_10_28_20 and updated it in [jonsson_3cy_01a_12_01_20]
- This contribution updates the CCC with new enhancements and a bug fix
- Examples are given of results for the updates



Updates In New Version

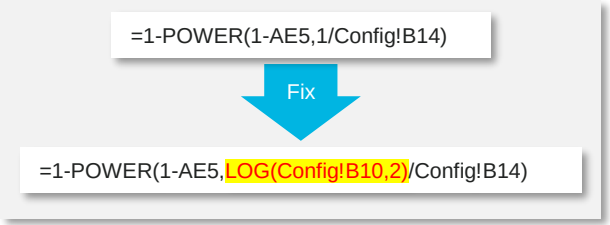
The following enhancements have been made to the CCC:

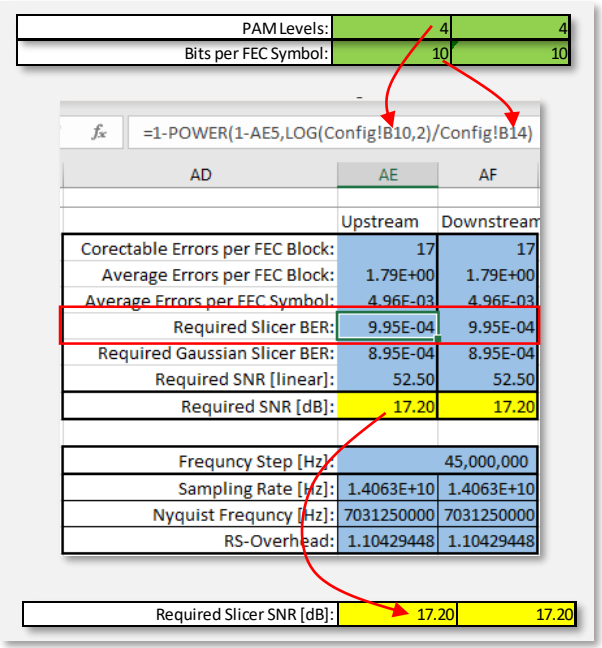
- Minor bug fix for required Slicer SNR calculation
- Separate modeling of PCB insertion loss
- New transmit PSD shapes, including Zero-Order-Hold added
- Enhanced user interface with pull-down selection, etc.



Bug Fix

- Bug reported by Charles Razzell
- The bug was in the calculation of coding gain from the RS-FEC
- The bug caused around -0.5dB error in SNR margin
- Nature of the bug:
  - Inconsistency in using bits vs symbols in error calculations
  - Used number of bits per FEC symbol to calculate the required BER at the slicer
  - Used number of PAM symbols (not bits) when calculating the required SNR
- Bug Fix:
  - Add factor log2(M) in cells “AE6” and “AF6” in the “Calculate” tab
  - The factor log2(M) gives the number of bits per PAM symbol for an PAM-M encoding

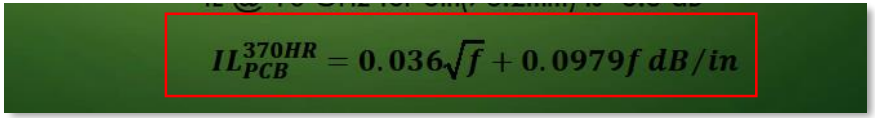




PCB Insertion Loss

- Separate modeling of PCB insertion loss has been added to the CCC
- Earlier suggestion to add to the length of the channel was insufficient and lead to confusion
- PCB model is taken from Kadry_3cy_02_0820
- Length of the PCB trace can be changed

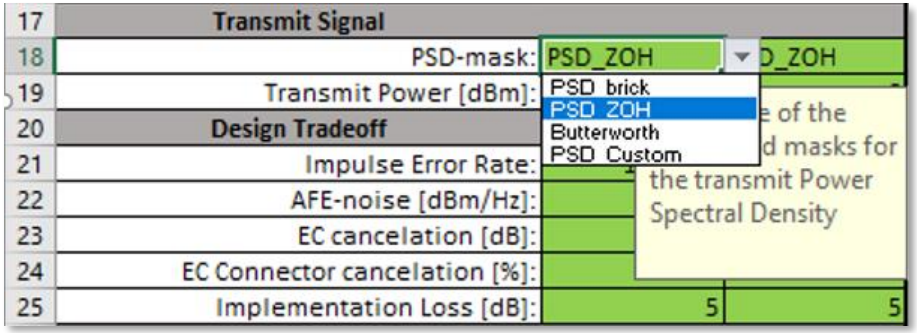
Simulation Parameters	
Cable Model:	mueller_3cy_01_12_01_20_sdp
NEW PCB model:	pcb_kadry_3cy_02_0820
NEW PCB trace length [m]:	0.0762
Connector Echo Model:	Hard
Temperature [°C]:	20
Max Simulation Frequency:	9.00E+09

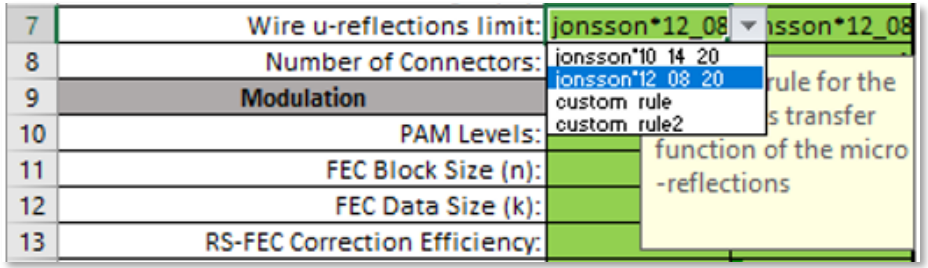


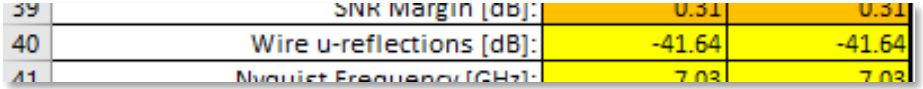
From https://www.ieee802.org/3/cy/public/aug20/Kadry_3cy_02_0820.pdf

Other Enhancements

- Enhancements to the user interface, with pull-down selections and input message
- New transmit PSD shapes, including Zero-Order-Hold and Butterworth added
- New micro-reflection limit rules added, but still possible to put a specific value as well
- New cable models added





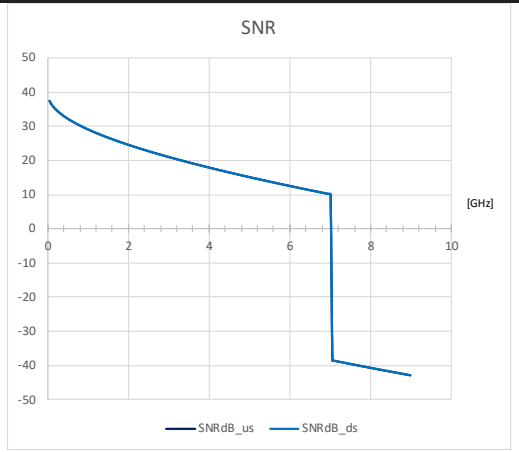


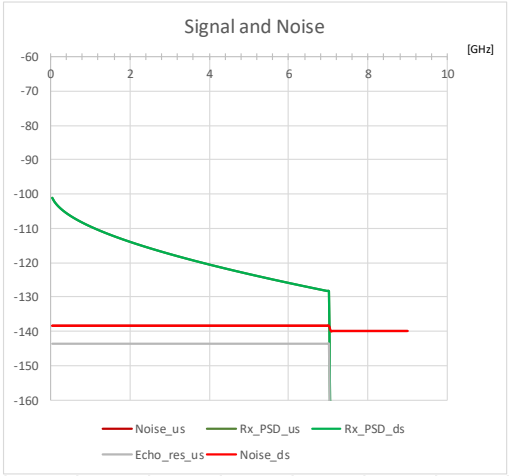
Example Calculations

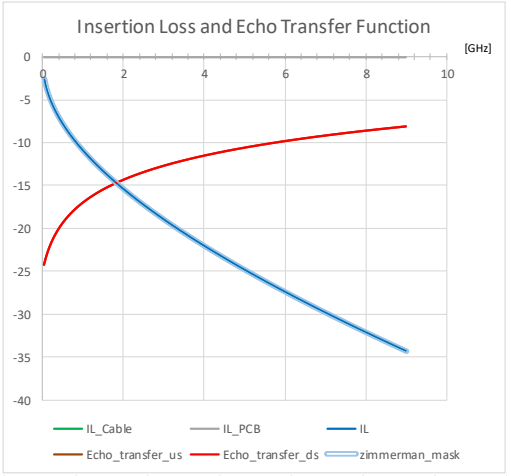
Effect of The Bug Fix

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
EC cancelation [dB]:	5	5
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	zimmerman_3cy_01a_1120	
PCB model:	none	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	20.28	20.28
Estimated Slicer SNR [dB]:	20.28	20.28
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	3.07	3.07
Wire u-reflections [dB]:	-40.00	-40.00
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	29.84	29.84
Cable Insertion Loss @ Nyquist [dB]:	29.84	29.84





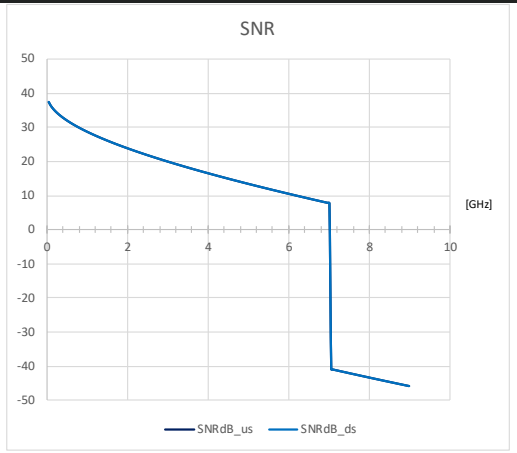


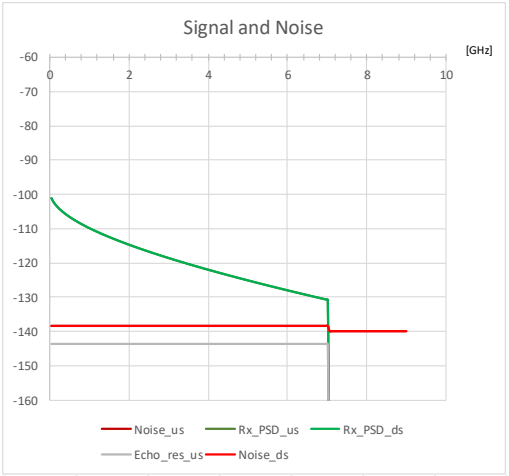
- To evaluate the effect of the bug fix, we can compare new results with result on Slide 7 of [jonsson_3cy_01a_12_01_20]
- With the same configuration the SNR margin is now 3.07dB, compared to 2.49dB before

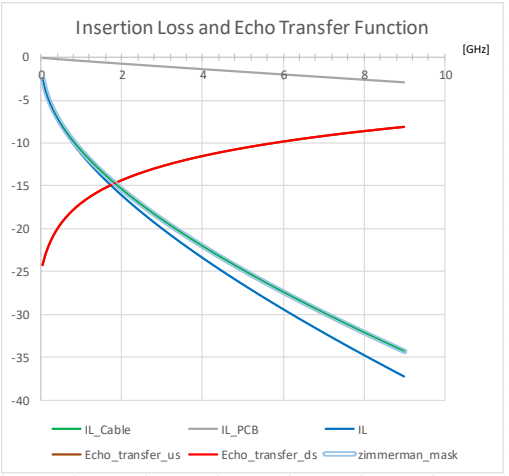
Effect of the PCB Insertion Loss

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
EC cancelation [dB]:	5	5
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	zimmerman_3cy_01a_1120	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	19.05	19.05
Estimated Slicer SNR [dB]:	19.05	19.05
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	1.85	1.85
Wire u-reflections [dB]:	-40.00	-40.00
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	32.19	32.19
Cable Insertion Loss @ Nyquist [dB]:	29.84	29.84





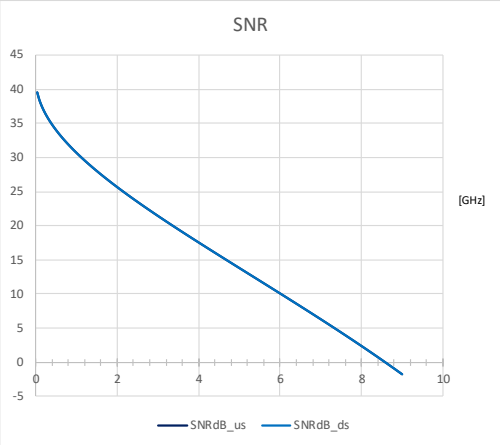


- Adding the Insertion Loss for 3in (0.0762m) PCB trace reduces the SNR margin from 3.07dB to 1.85dB
- This is a drop of 1.22dB

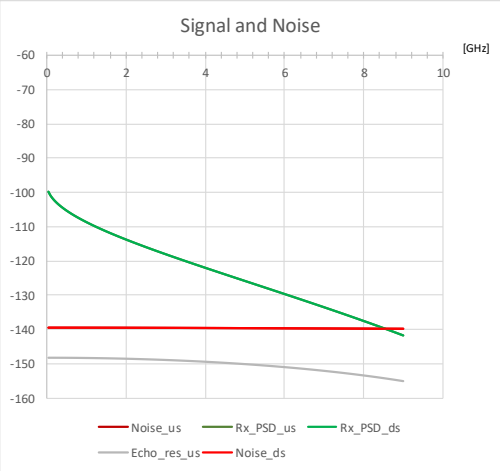
Performance of the Zimmerman mask with realistic implementation values

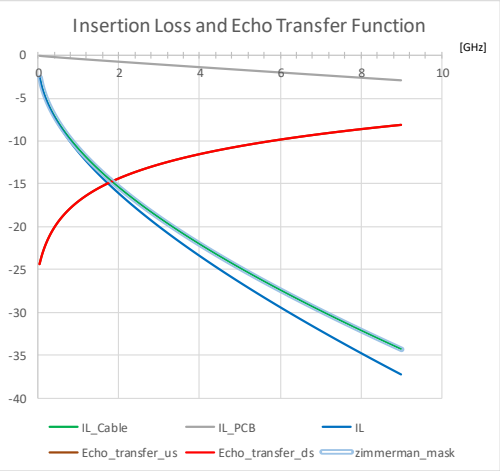
	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	ionsson*12_08_2	onsson*12_08_2
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
EC cancelation [dB]:	6	6
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	zimmerman_3cy_01a_1120	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	20.03	20.03
Estimated Slicer SNR [dB]:	15.03	15.03
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	-2.18	-2.18
Wire u-reflections [dB]:	-44.84	-44.84
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	32.19	32.19
Cable Insertion Loss @ Nyquist [dB]:	29.84	29.84



- Realistic implementation values including micro-reflection limits, ZOH PSD-mask, 6dB echo cancelation, and 5dB implementation loss
- This gives negative 2.18dB SNR-margin

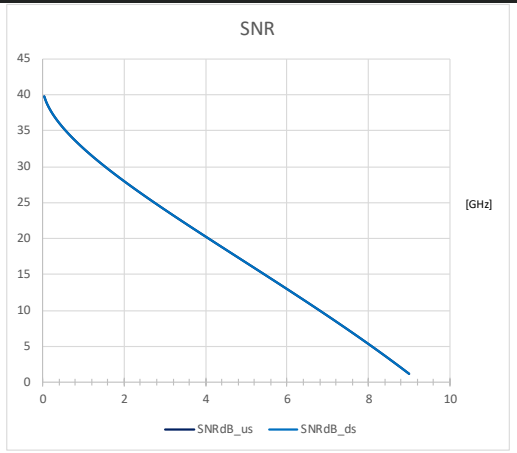


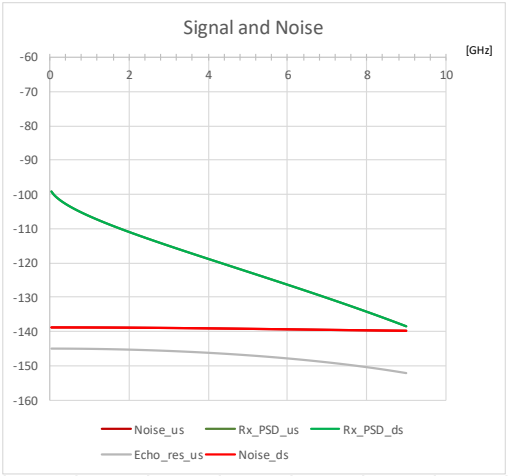


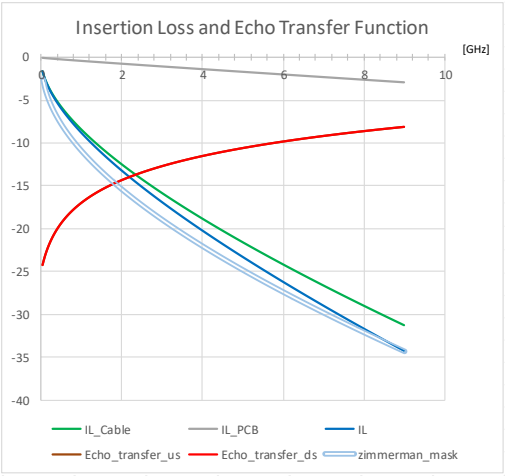
Performance of a good cable with realistic implementation values

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	ionsson*12_08_	onsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
EC cancelation [dB]:	6	6
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	22.51	22.51
Estimated Slicer SNR [dB]:	17.51	17.51
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	0.31	0.31
Wire u-reflections [dB]:	-41.64	-41.64
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	28.99	28.99
Cable Insertion Loss @ Nyquist [dB]:	26.64	26.64





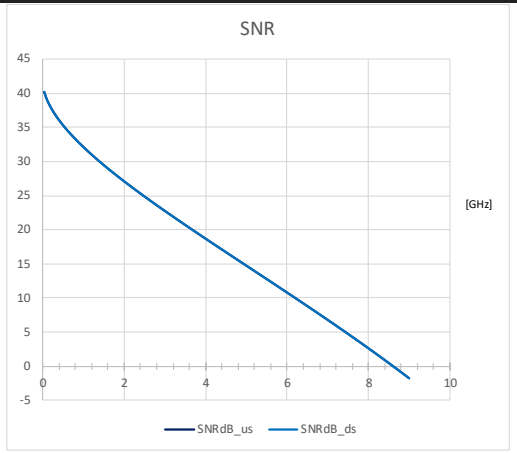


- Same realistic implementation values as before
- Using model for SDP cable from mueller_3cy_01_12_01_20
- This gives positive 0.31dB SNR-margin

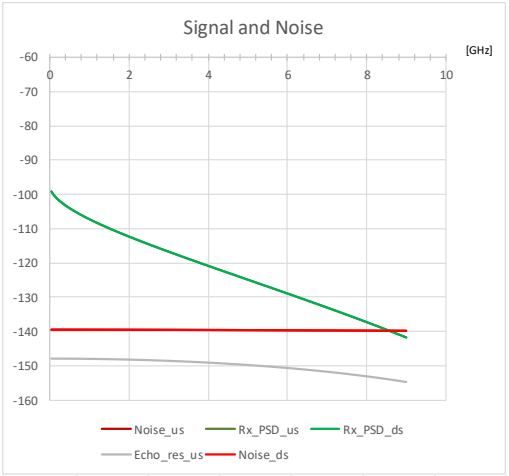
Performance of a good cable at T=95°C

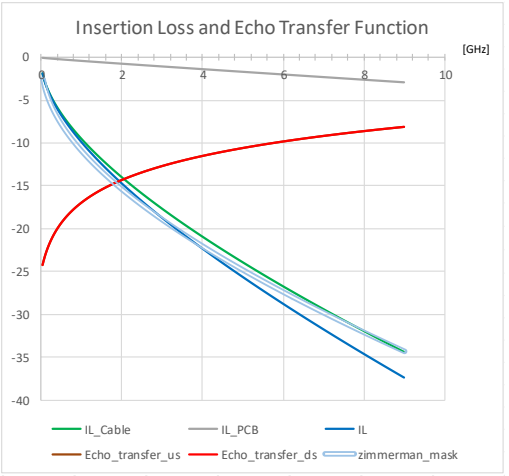
	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	ionsson*12_08_	onsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
EC cancelation [dB]:	6	6
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	95	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.09	21.09
Estimated Slicer SNR [dB]:	16.09	16.09
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	-1.11	-1.11
Wire u-reflections [dB]:	-44.38	-44.38
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	31.73	31.73
Cable Insertion Loss @ Nyquist [dB]:	29.38	29.38



- The maximum average temperature is probably in the range 90-95°C, based on information in [wienckowski_3cy_01_01_12_21]
- This gives negative 1.11dB SNR-margin

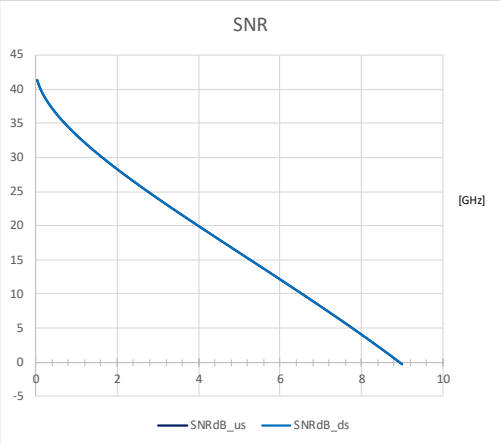




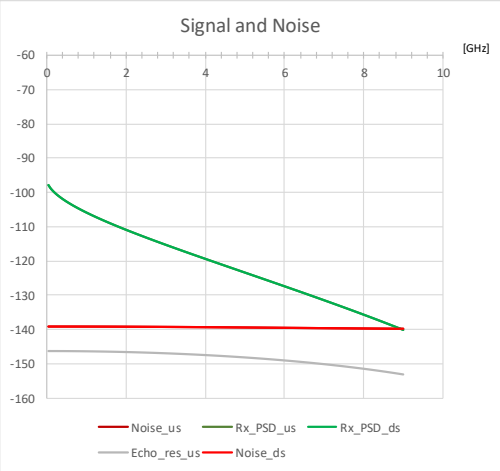
Performance of a good cable at T=95°C with 1.5dBm Tx-Power

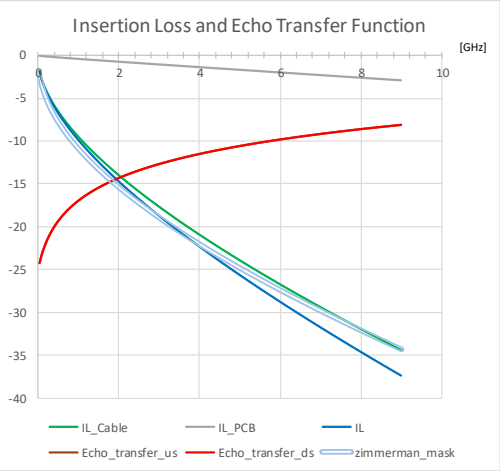
	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	ionsson*12_08_	onsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	1.5	1.5
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
EC cancelation [dB]:	6	6
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	95	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	22.39	22.39
Estimated Slicer SNR [dB]:	17.39	17.39
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	0.19	0.19
Wire u-reflections [dB]:	-44.38	-44.38
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	31.73	31.73
Cable Insertion Loss @ Nyquist [dB]:	29.38	29.38



- Same case as previous slide, but with transmit power raised to 1.5dBm
- This gives positive 0.19dB SNR-margin
- This is an example of an 11m cable with positive SNR-margin

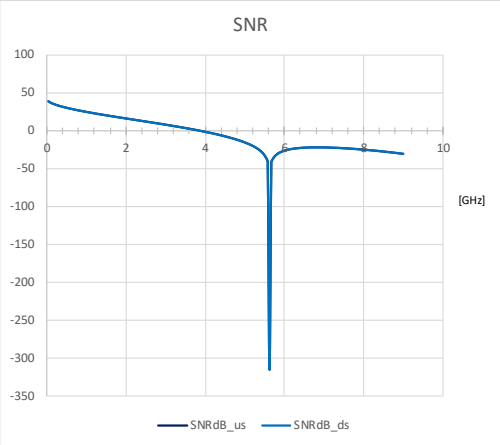




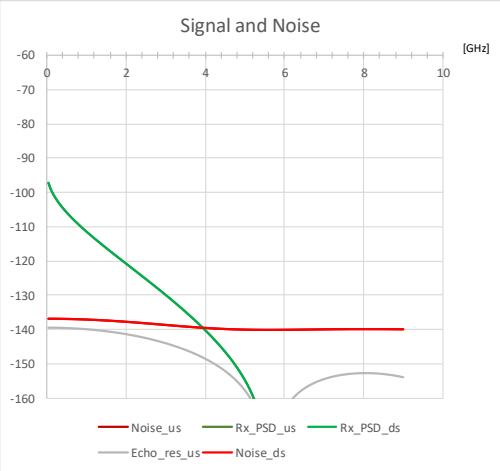
Simple Reality Check – IEEE 802.3ch Performance

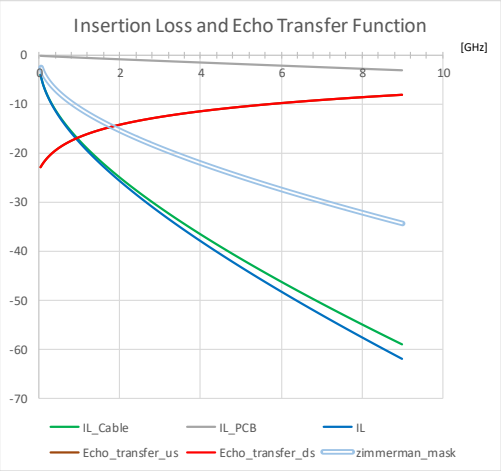
	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	10	10
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	15.000	15.000
Wire u-reflections limit:	-40	-40
Number of Connectors:	6	6
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
EC cancelation [dB]:	6	6
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	eq149-18	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	22.22	22.22
Estimated Slicer SNR [dB]:	17.22	17.22
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	0.02	0.02
Wire u-reflections [dB]:	-40.00	-40.00
Nyquist Frequency [GHz]:	2.81	2.81
Channel Insertion Loss @ Nyquist [dB]:	30.74	30.74
Cable Insertion Loss @ Nyquist [dB]:	29.74	29.74



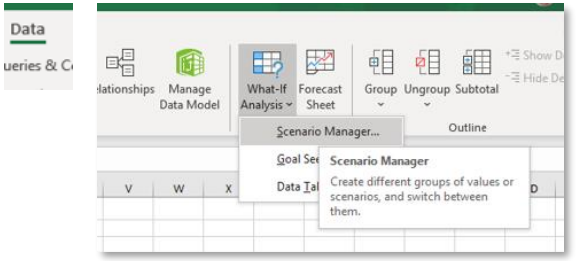
- Using configuration for 802.3ch at 10Gbps
- Same realistic implementation values as before
- This gives positive 0.02dB SNR-margin
- The simulation passes the simple reality check

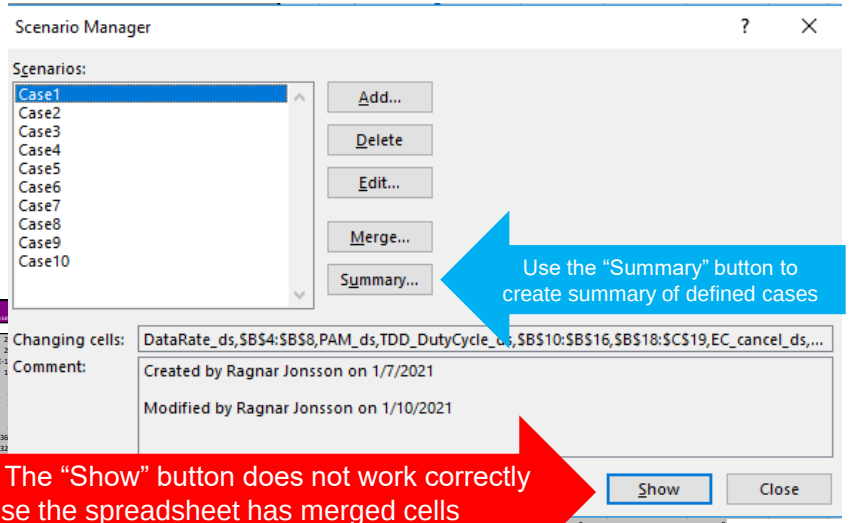




Scenario Manager

- The Excel Scenario Manager can be useful for comparing different cases and to save scenarios of interest
- There are 10 predefined cases in the Scenario Manager





Use the "Summary" button to create summary of defined cases

WARNING: The "Show" button does not work correctly because the spreadsheet has merged cells

Scenario Summary		Current Values:	Case1	Case2	Case3	Case4	Case
Changing Cells:							
DataRate_ds		25	25	25	25	25	2
DataRate_us		25	25	25	25	25	2
Target_BER		1.00E-12	1E-12	1E-12	1E-12	1E-12	1E-1
cable_length		11.000	11	10.5	10	8.75	1
micro_reflection_limit	jonsson*12_08_20		jonsson*12_08_20	jonsson*12_08_20	jonsson*12_08_20	jonsson*12_08_20	jonsson*12_08_20
number_of_connectors		4	4	4	4	4	
PAM_ds		4	4	4	4	4	
TDD_DutyCycle_ds		100%	1	1	1	1	
PAM_us		4	4	4	4	4	
fec_block_size		360	360	360	360	360	36
fec_data_size		326	326	326	326	326	32
fec_efficency		100%	1	1	1		
fec_bits_per_symbol		10	10	10	10		
TDD_DutyCycle_us		100%	1	1	1		
framing_overhead		1.875%	0.01875	0.01875	0.01875		
psd_mask_us	PSD_ZOH		PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH	
psd_mask_ds	PSD_ZOH		PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH	
Tx_power_us		0	0	0	0		
Tx_power_ds		0	0	0	0	0	0
EC_cancel_ds		6	6	6	6	6	6
impulse_error_rate		1.00E-04	0.0001	0.0001	0.0001	0.0001	0.0001
AFE_noise_us		-140	-140	-140	-140	-140	-140
EC_cancel_us		6	6	6	6	6	6
EC_conector_ratio_us		100%	1	1	1	1	1
implementation_loss_us		5	5	5	5	5	5
implementation_loss_ds		5	5	5	5	5	5
cable_model	mueller_3cy_01_12_01_20_sdp		mueller_3cy_01_12_01_20_sdp	neulinger_3cy_01_12_15_20	boyer_3cy_01_10_14_20_c1	patel_3cy_01_0920	diminico_3cy_01a_1_5_21_26awg
pcb_model	pcb_kadry_3cy_02_0820		pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820
PCB_trace_length		0.0762	0.0762	0.0762	0.0762	0.0762	0.0762
connector_echo_model	Hard		Hard	Hard	Hard	Hard	Hard
T		20	20	20	20	20	20
f_max		9.00E+09	9000000000	9000000000	9000000000	9000000000	9000000000
Result Cells:							
SNR_margin_us		0.31	0.31	0.00	-0.02	0.05	0.90
SNR_margin_ds		0.31	0.31	0.00	-0.02	0.05	0.90

Scenario Summary		mueller_3cy_01_12_01_20_stp	diminico_3cy_01a_1_5_21_28awg	koeppendoerfer_3cy_01_10_28_20_sdp3	eq149-18	zimmerman_3cy_01a_1120
Changing Cells:						
DataRate_ds		25	25	25	25	25
DataRate_us		25	25	25	25	25
Target_BER		1E-12	1E-12	1E-12	1E-12	1E-12
cable_length		10	10	10	10	10
micro_reflection_limit	jonsson*12_08_20	jonsson*12_08_20	jonsson*12_08_20	jonsson*12_08_20	jonsson*12_08_20	jonsson*12_08_20
number_of_connectors		4	4	4	4	4
PAM_ds		4	4	4	4	4
TDD_DutyCycle_ds		100%	100%	100%	100%	100%
PAM_us		4	4	4	4	4
fec_block_size		360	360	360	360	360
fec_data_size		326	326	326	326	326
fec_efficency		100%	100%	100%	100%	100%
fec_bits_per_symbol		10	10	10	10	10
TDD_DutyCycle_us		100%	100%	100%	100%	100%
framing_overhead		1.875%	1.875%	1.875%	1.875%	1.875%
psd_mask_us	PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH
psd_mask_ds	PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH	PSD_ZOH
Tx_power_us		0	0	0	0	0
Tx_power_ds		0	0	0	0	0
EC_cancel_ds		6	6	6	6	6
impulse_error_rate		0.0001	0.0001	0.0001	0.0001	0.0001
AFE_noise_us		-140	-140	-140	-140	-140
EC_cancel_us		6	6	6	6	6
EC_conector_ratio_us		1	1	1	1	1
implementation_loss_us		5	5	5	5	5
implementation_loss_ds		5	5	5	5	5
cable_model	mueller_3cy_01_12_01_20_stp	diminico_3cy_01a_1_5_21_28awg	koeppendoerfer_3cy_01_10_28_20_sdp3	eq149-18	zimmerman_3cy_01a_1120	
pcb_model	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820	pcb_kadry_3cy_02_0820
PCB_trace_length		0.0762	0.0762	0.0762	0.0762	0.0762
connector_echo_model	Hard	Hard	Hard	Hard	Hard	Hard
T		20	20	20	20	20
f_max		9000000000	9000000000	9000000000	9000000000	9000000000
Result Cells:						
SNR_margin_us		0.90	0.00	-0.01	0.07	-5.94
SNR_margin_ds		0.90	0.00	-0.01	0.07	-5.94

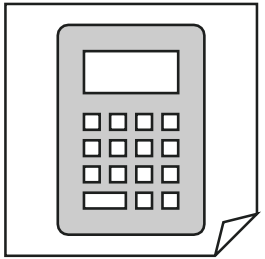
Some Observations

The Zimmerman strawman IL limit probably has too much insertion loss

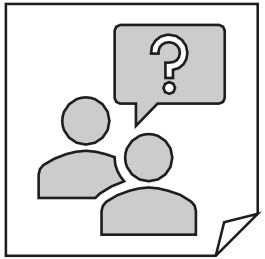
It may be possible to operate with 25Gbps over real 11m cables, but this requires more in-depth evaluation

The CCC passes the basic reality check of testing it against the IEEE 802.3ch requirements

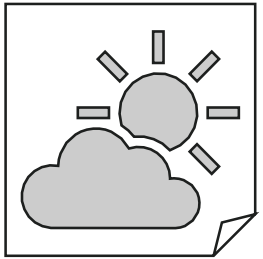
Summary



We described updates to the channel capacity calculator tool, including one bug fix



For typical model parameters, the IL limit introduced in zimmerman_3cy_01a_1120 has too much insertion loss



There exist simulation cases where 25Gbps can realistically operate over 11m

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