FEC and Interleaving Candidate

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Introduction

- In the Telephonic Interim Meeting on September 9, 2021, the text proposal in jonsson_etal_3cy_01a_09_21_21 was adopted
- FEC and Interleaving was further discussed in
  - jonsson_3cy_01_11_09_21
  - tingting_3cy_01a_11_16_21
  - tu_3cy_01_12_07_21
  - castrillon_3cy_01_12_07_21
- This contribution identifies good candidates for FEC and the interleaving depth

FEC and Interleaving Candidate

- Based on earlier presentations on FEC and interleaving, and on offline discussions between authors of these presentations, the following candidate is suggested
  - RS(936,846) with L=1,2,4,8

- We may also consider the possibility of using L=6 instead of L=8, but that needs more discussion

FEC and Interleaving Options

RS Code	Interleaver Depth	Required Slicer SNR [dB]			Intrinsic Latency [ns]	Relative Complexity*	
		50 ns burst	25 ns burst	0 ns burst		w.r.t RS(360,326), L=1	w.r.t RS(360,326), L=4
(360,326)	4	-	-	16.8	560	2.1	1.0
	8	-	18.2	16.8	1121	3.7	1.8
	10	20.9	18.0	16.8	1401	4.4	2.1
	12	19.1	17.6	16.8	1681	5.2	2.5
	16	18.2	17.5	16.8	2241	6.7	3.2
(936,846)	1	-	-	16.1	364	2.6	1.2
	2	-	18.6	16.1	728	3.6	1.7
	4	18.6	16.9	16.1	1456	5.6	2.7
	6	17.3	16.6	16.1	2185	7.6	3.6
	8	16.9	16.4	16.1	2913	9.5	4.5

* Relative complexity is expressed with respect to RS(360,326) with an interleaver depth (L) of 1 or 4 depending the column. It is a relative measure of silicon area