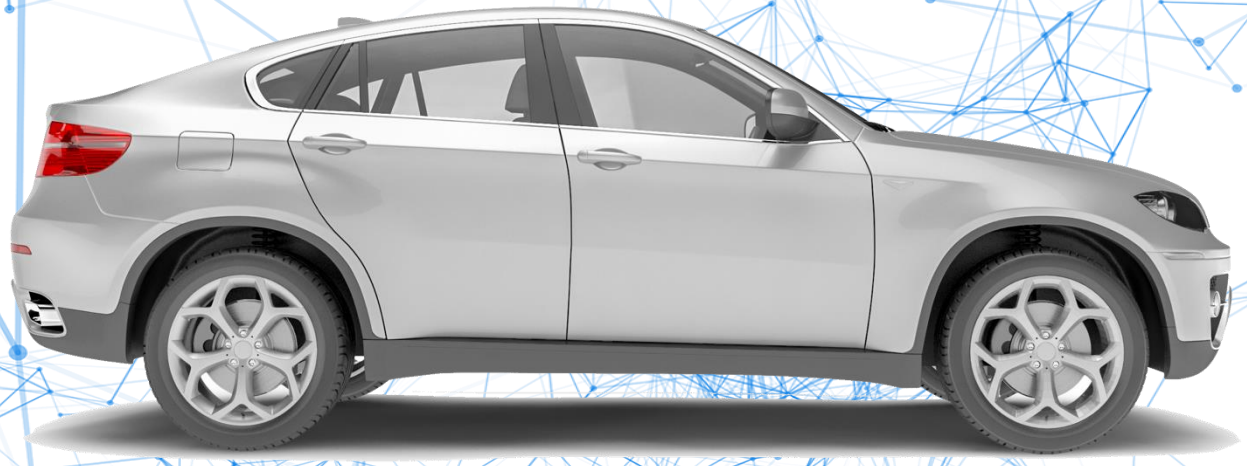


A Proposal for the Limit Line of Insertion Loss

Hossein Sedarat

IEEE 802.3cy

January 2021

Overview

- A limit line for insertion loss is the foundation to derive other specifications of the transceiver

- There have been considerable number of contributions analyzing from PHY-design perspective:
  - sedarat_101420: Preliminary PHY complexity analysis
  - jonsson_111820: Capacity estimation tool
  - sedarat_010521: Comprehensive analysis

Comprehensive Analysis

- The analysis in sedarat_010521 includes the following:
  - Reasonable transmit PSD and power
  - The loss of PCB, MDI connectors and other components
  - Reasonable implementation loss

- Concludes that a tolerated limit line for the insertion loss of the link-segment can be defined based on 802.3ch limit line profile extended to higher frequencies and scaled to 6.5 m
  - Roughly 22 dB loss at Nyquist frequency

Decision to Consider

- PROPOSED:

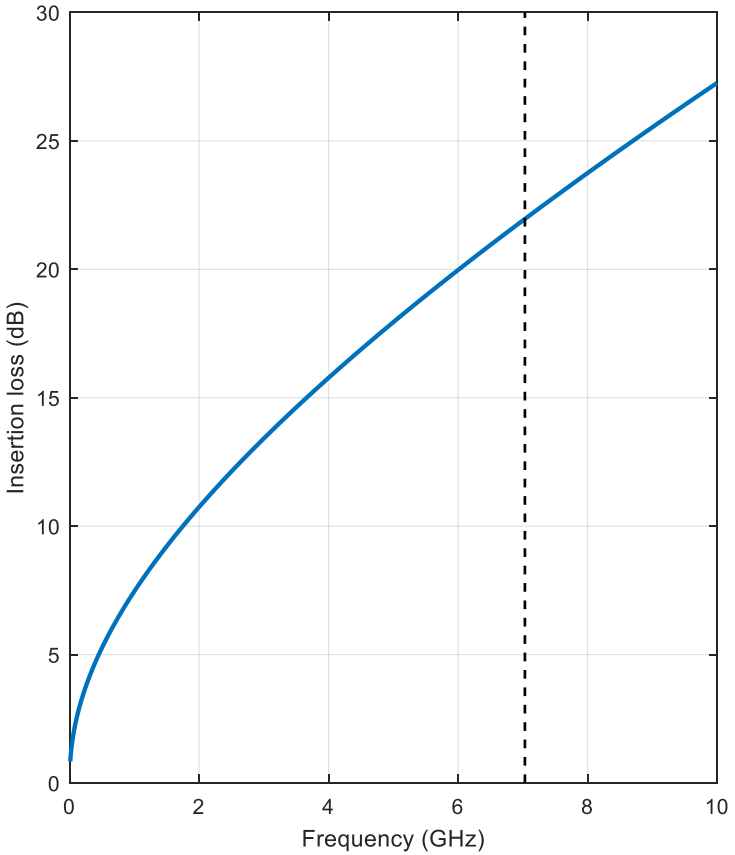
  Move that: 802.3cy consider the following limit-line for insertion loss

$$Insertion\ Loss(f) \leq \frac{6.5}{15}(0.002 \times f + 0.68 \times f^{0.45})$$

Where f is the frequency in MHz,

$1 \leq f \leq F_{max}, and\ F_{max}$=10 GHz

(F_{max} is chosen to be 2.5x the corresponding 802.3ch value)



THANK YOU

ETHERNOVIA | hossein.sedarat@ethernovia.com