## rfer\_timer

August 16, 2022

Mike Tu tum@broadcom.com

1 | IEEE 802.3cy Task Force

## Introduction

- In 165.3.7.2.2:
  - hi\_rfer
  - Boolean variable that is asserted TRUE when the rfer\_cnt reaches 16 errors in one rfer\_timer interval.
- In 802.3ch, rfer\_timer = 312500 bit times = 31.25/S us for 10G/5G/2.5G
- This translates to 97.65625 RS FEC frames
- In summary, hi\_rfer = TRUE if 16 out of 97.65625 RS FEC frames are in errors

## **802.3cy Considerations**

- A comment was submitted against D1.3 165.3.7.2.3:
  - rfer\_timer
  - Timer that is triggered every 125/(4 × S)12.5 µs +±1%, -25%. When the timer reaches its terminal count, rfer\_timer\_done = TRUE
- Upon further evaluation, the proposed 12.5 us only translates to 37.56 RS FEC frames for 802.3cy. This is obviously not a good choice.
- A better option is to keep the same RS FEC counter ratio as in 802.3ch:
  - hi\_rfer = TRUE if 16 out of 97.65625 RS FEC frames are in errors
  - 31.25 us \* (332.8 ns/FEC frame) / (320 ns/FEC frame) = 32.5 us
- It is proposed to set rfer\_timer = 32.5 us for 25GBASE-T1
- <sup>3</sup> | IEEE 802.3cy Task Force

## **Proposed Changes**

- On page 78, line 8, change "12.5 us" to "32.5 us".
- On page 27, line 44, add a new paragraph:
- 45.2.3.xx.2 PCS high RFER (3.2324.9)
- When read as a one, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS receiver is detecting 16 or more RS-FEC errored blocks within one rfer\_timer interval. When read as a zero, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS is detecting fewer than 16 RS-FEC errored blocks within one rfer\_timer interval. Bit 3.2324.9 is a reflection of the state of the hi\_rfer variable defined in 149.3.8.1 and 165.3.8.1.
- Note: this is 45.2.3.87.2 in IEEE Draft P802.3/D3.2.