Revised link budget assessment

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Introduction and objectives

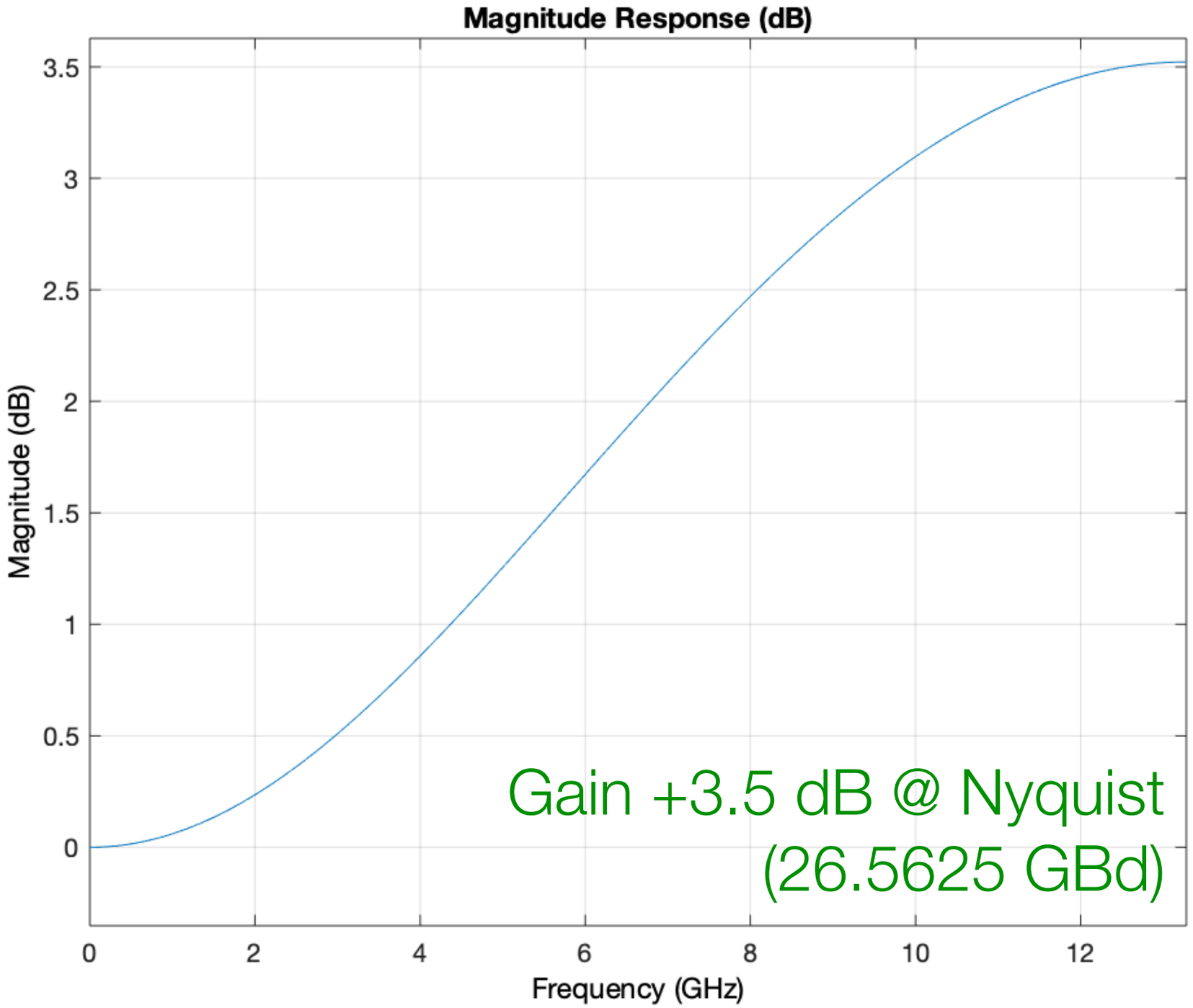
- Based on the characterization and experiments reported in [1] considering the reliability constraint of [2], a revised link budget assessment is provided for all the data-rates included in the 802.3cz objectives
- The main objective of this presentation is to demonstrate the 50 Gb/s PCS/PMA baseline proposal presented in [3] is even feasible with VCSELs just designed for 25 Gb/s NRZ
- Future experiments using longer wavelength VCSELs are expected
- These experiments will reinforce the feasibility of [3] further, because the use of these VCSELs will allow simpler and lower power consumption transceiver implementations (i.e. reduced DSP requirements like lower TX FFE gain and smaller RX equalizer computational complexity)

Link budget for 25, 10, 5 and 2.5 Gb/s

Baseline for simulations of 25 Gb/s and below

- Data-rate: 10·S Gb/s, where S = 2.5, 1.0, 0.5, 0.25
- Modulation: NRZ, PAM M = 2
- FEC: RS(544, 522) GF(2^{10})
  - Error correction capability: t = 11
  - Code-rate: CR = 0.96
  - Coding-gain: CG (for BER = 10^{-12} after FEC) = 5.55 dB
- BER before FEC (for BER = 10^{-12} after FEC) = 0.00017
- Fs = 10.625·S GBd, where S = 2.5, 1.0, 0.5, 0.25
- SNRd > 11.07 dB for BER < 10^{-12} after FEC
- RX equalization: DFE
- TIA: Optimized parameters for 25 Gb/s
- PD: GaAs PIN optimized for 850nm 0.6 A/W, 25 Gbaud
- RX conditions: worst production corner, T_J = 125 ºC
- TX & RX clock random jitter (RMS):
  - 25 Gb/s: t_J < 0.7 ps, 10 Gb/s: t_J < 1.8 ps
  - 5 Gb/s: t_J < 3.6 ps, 2.5 Gb/s: t_J < 7.0 ps
- RIL:
  - 0.5 dB @ 25 Gb/s (extracted from time-domain simulations of the complete system)
  - < 0.1 dB @ rates <= 10 Gb/s
- Fiber is OM3: 2.0 dB/km. BW_{eff} = 932 MHz·km @ 980nm
  - EMB = 950 MHz·km @ 980nm
  - BW_{CD} = 5498 MHz·km @ 980nm
- Fiber length = **40 meters**
- Number of inline connections: **N_{IC} = 4**
- 850 nm VCSEL simulation model
- VCSEL ER = 4 dB
- VCSEL driver:
  - Voltage driver with Z_o = 100 Ohm, differential
  - FFE fixed to [-0.125, 1.25, -0.125] for 25 Gb/s
  - No FFE for rates <= 10 Gb/s
- VCSEL RIN_{OMA}:
  - 25 Gb/s: -124 dB/Hz, BW_n = 20.7 GHz
  - 10 Gb/s and below: -120 dB/Hz, BW_n = 8.3 GHz
  - 5 Gb/s and below: -120 dB/Hz, BW_n = 4.1 GHz
  - 2.5 Gb/s and below: -120 dB/Hz, BW_n = 2.1 GHz
- VCSEL I_{BIAS} = 5 mA
- VCSEL temperatures (T_{BS}) = 125 ºC

3-tap FFE [-0.125, 1.25, -0.125] frequency response



Link budget assessment for 25 Gb/s (simulation)

25 Gb/s link budget assessment — simulation

Parameter	Value	
VCSEL SE variation in the same bin (dB)	0.50	A
VCSEL aging (dB)	1.00	B
VCSEL to TP2 max coupling loss (dB)	2.50	C
$IL_{TP1\text{-}to\text{-}TP2}$, max (dB)	4.00	D = A + B + C
$IL_{TP3\text{-}to\text{-}TP4}$, max (dB)	2.50	E
Insertion loss per inline connection, IL_{IC} max (dB)	2.00	F
Number of inline connections (N_{IC})	4	G
Macrobend insertion loss, max (dB)	0.20	H
Microbend insertion loss, max (dB)	0.00	I
Bending insertion loss, IL_{BEND} max (dB)	0.20	J = H + I
Fiber attenuation (dB/km)	2.00	K
Channel attenuation, $IL_{TP2\text{-}to\text{-}TP3}$, max (dB)	8.28	L = (F × G) + J + (40/1000 × K)
$IL_{TP1\text{-}to\text{-}TP4}$, max (dB)	14.78	M = D + E + L
OMA_{TP1} min (dBm)	0.30	N
OMA_{TP2} min (dBm)	-3.70	O = N - D
OMA_{TP4} max (dBm)	-17.50	P
OMA_{TP3} max (dBm)	-15.00	Q = P + E
Power budget (dB)	11.30	R = O - Q
Unallocated margin (dB)	3.02	S = R - L

Unallocated margin for additional implementation losses

Link budget assessment for 10 Gb/s (simulation)

10 Gb/s link budget assessment — simulation

Parameter	Value	
VCSEL SE variation in the same bin (dB)	0.50	A
VCSEL aging (dB)	1.00	B
VCSEL to TP2 max coupling loss (dB)	3.50	C
$IL_{TP1\text{-}to\text{-}TP2}$, max (dB)	5.00	D = A + B + C
$IL_{TP3\text{-}to\text{-}TP4}$, max (dB)	3.50	E
Insertion loss per inline connection, IL_{IC} max (dB)	2.50	F
Number of inline connections (N_{IC})	4	G
Macrobend insertion loss, max (dB)	0.20	H
Microbend insertion loss, max (dB)	0.00	I
Bending insertion loss, IL_{BEND} max (dB)	0.20	J = H + I
Fiber attenuation (dB/km)	2.00	K
Channel attenuation, $IL_{TP2\text{-}to\text{-}TP3}$, max (dB)	10.28	L = (F × G) + J + (40/1000 × K)
$IL_{TP1\text{-}to\text{-}TP4}$, max (dB)	18.78	M = D + E + L
OMA_{TP1} min (dBm)	0.30	N
OMA_{TP2} min (dBm)	-4.70	O = N - D
OMA_{TP4} max (dBm)	-21.80	P
OMA_{TP3} max (dBm)	-18.30	Q = P + E
Power budget (dB)	13.60	R = O - Q
Unallocated margin (dB)	3.32	S = R - L

Unallocated margin for additional implementation losses

Link budget assessment for 5 Gb/s (simulation)

5 Gb/s link budget assessment — simulation

Parameter	Value	
VCSEL SE variation in the same bin (dB)	0.50	A
VCSEL aging (dB)	1.00	B
VCSEL to TP2 max coupling loss (dB)	3.50	C
$IL_{TP1\text{-}to\text{-}TP2}$, max (dB)	5.00	D = A + B + C
$IL_{TP3\text{-}to\text{-}TP4}$, max (dB)	3.50	E
Insertion loss per inline connection, IL_{IC} max (dB)	2.50	F
Number of inline connections (N_{IC})	4	G
Macrobend insertion loss, max (dB)	0.20	H
Microbend insertion loss, max (dB)	0.00	I
Bending insertion loss, IL_{BEND} max (dB)	0.20	J = H + I
Fiber attenuation (dB/km)	2.00	K
Channel attenuation, $IL_{TP2\text{-}to\text{-}TP3}$, max (dB)	10.28	L = (F × G) + J + (40/1000 × K)
$IL_{TP1\text{-}to\text{-}TP4}$, max (dB)	18.78	M = D + E + L
OMA_{TP1} min (dBm)	0.30	N
OMA_{TP2} min (dBm)	-4.70	O = N - D
OMA_{TP4} max (dBm)	-25.10	P
OMA_{TP3} max (dBm)	-21.60	Q = P + E
Power budget (dB)	16.90	R = O - Q
Unallocated margin (dB)	6.62	S = R - L

Unallocated margin for additional implementation losses

Link budget assessment for 2.5 Gb/s (simulation)

2.5 Gb/s link budget assessment — simulation

Parameter	Value	
VCSEL SE variation in the same bin (dB)	0.50	A
VCSEL aging (dB)	1.00	B
VCSEL to TP2 max coupling loss (dB)	3.50	C
$IL_{TP1\text{-}to\text{-}TP2}$, max (dB)	5.00	D = A + B + C
$IL_{TP3\text{-}to\text{-}TP4}$, max (dB)	3.50	E
Insertion loss per inline connection, IL_{IC} max (dB)	2.50	F
Number of inline connections (N_{IC})	4	G
Macrobend insertion loss, max (dB)	0.20	H
Microbend insertion loss, max (dB)	0.00	I
Bending insertion loss, IL_{BEND} max (dB)	0.20	J = H + I
Fiber attenuation (dB/km)	2.00	K
Channel attenuation, $IL_{TP2\text{-}to\text{-}TP3}$, max (dB)	10.28	L = (F × G) + J + (40/1000 × K)
$IL_{TP1\text{-}to\text{-}TP4}$, max (dB)	18.78	M = D + E + L
OMA_{TP1} min (dBm)	0.30	N
OMA_{TP2} min (dBm)	-4.70	O = N - D
OMA_{TP4} max (dBm)	-27.90	P
OMA_{TP3} max (dBm)	-24.40	Q = P + E
Power budget (dB)	19.70	R = O - Q
Unallocated margin (dB)	9.42	S = R - L

Unallocated margin for additional implementation losses

Link budget analysis for 50 Gb/s

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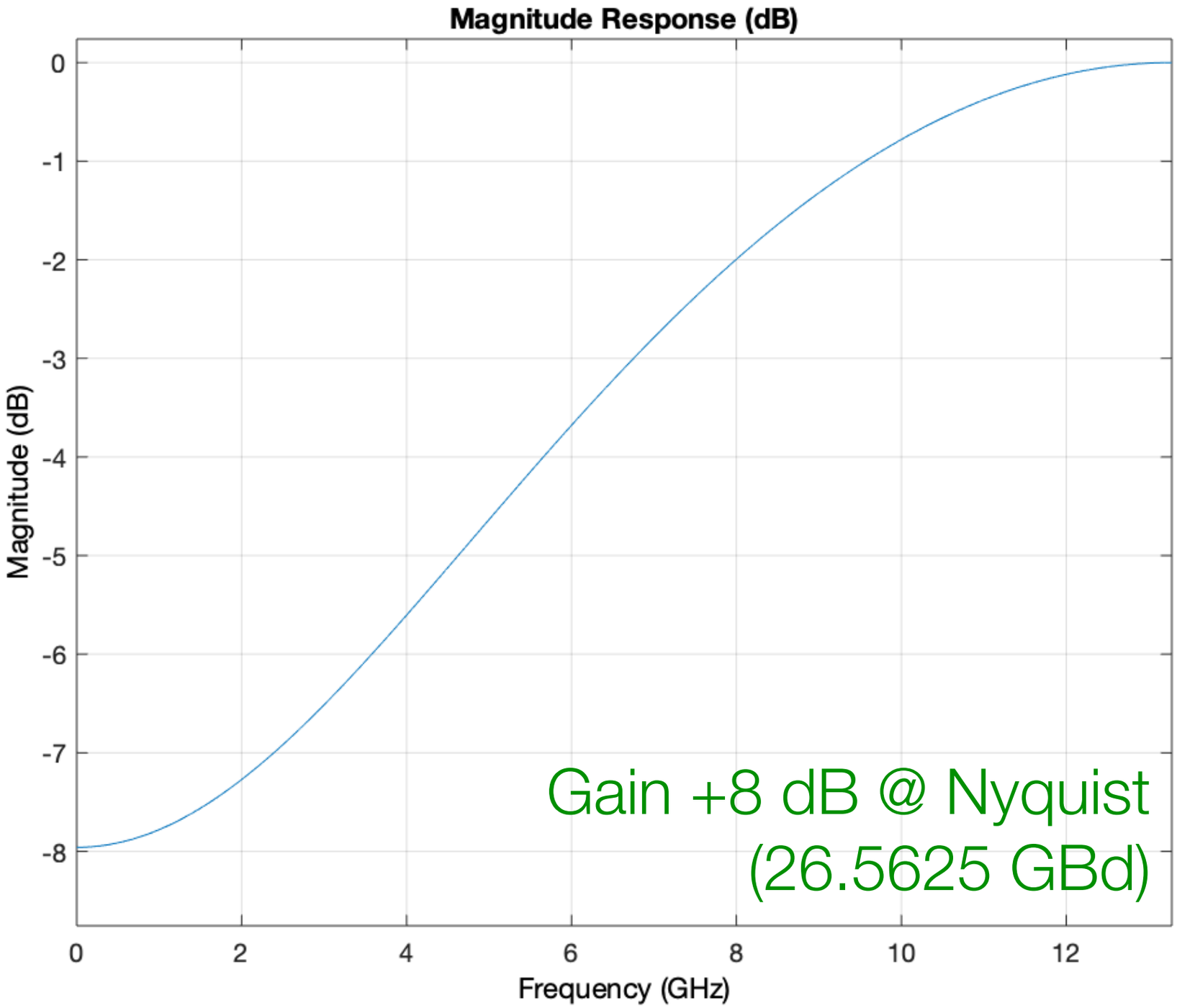
Baseline for simulations of 50 Gb/s

- Data-rate: 50 Gb/s
- Modulation: PAM M = 4, Gray mapping
- FEC: RS(544, 522) GF(2^{10})
  - Error correction capability: t = 11
  - Code-rate: CR = 0.96
  - Coding-gain: CG (for BER = 10^{-12} after FEC) = 5.49 dB
- BER before FEC (for BER = 10^{-12} after FEC) = 0.00017
- Fs = 26.5625 GBd
- SNRd > 17.88 dB for BER < 10^{-12} after FEC
- RX equalization: DFE
- TIA: Optimized parameters for 50 Gb/s
- PD: GaAs PIN optimized for 850nm 0.6 A/W, 25 Gbaud
- RX conditions: worst production corner, T_J = 125 ºC
- TX & RX clock random jitter (RMS): t_J < 0.3 ps
- RIL = 1.0 dB (extracted from time-domain simulations of the complete system)
- Fiber is OM3: 2.0 dB/km. BW_{eff} = 932 MHz·km @ 980nm
  - EMB = 950 MHz·km @ 980nm
  - BW_{CD} = 5498 MHz·km @ 980nm
- Fiber length = **40 meters**
- Number of inline connections: **N_{IC} = 2**
- 850 nm VCSEL simulation model
- VCSEL ER = 4 dB
- VCSEL driver:
  - Voltage driver with Z_o = 100 Ohm, differential
  - FFE fixed to [-0.15, 0.7, -0.15]
- VCSEL RIN_{OMA}: -128 dB/Hz, BW_n = 20.7 GHz
- VCSEL I_{BIAS} = 5 mA
- VCSEL temperatures (T_{BS}) = 125 ºC

3-tap FFE [-0.15, 0.7, -0.15] frequency response



Link budget assessment for 50 Gb/s (simulation)

50 Gb/s link budget assessment — Simulation

Parameter	Value	
VCSEL SE variation in the same bin (dB)	0.50	A
VCSEL aging (dB)	1.00	B
VCSEL to TP2 max coupling loss (dB)	2.50	C
$IL_{TP1\text{-}to\text{-}TP2}$, max (dB)	4.00	D = A + B + C
$IL_{TP3\text{-}to\text{-}TP4}$, max (dB)	2.50	E
Insertion loss per inline connection, IL_{IC} max (dB)	2.00	F
Number of inline connections (N_{IC})	2	G
Macrobend insertion loss, max (dB)	0.20	H
Microbend insertion loss, max (dB)	0.00	I
Bending insertion loss, IL_{BEND} max (dB)	0.20	J = H + I
Fiber attenuation (dB/km)	2.00	K
Channel attenuation, $IL_{TP2\text{-}to\text{-}TP3}$, max (dB)	4.28	L = (F × G) + J + (40/1000 × K)
$IL_{TP1\text{-}to\text{-}TP4}$, max (dB)	10.78	M = D + E + L
OMA_{TP1} min (dBm)	0.30	N
OMA_{TP2} min (dBm)	-3.70	O = N - D
OMA_{TP4} max (dBm)	-13.00	P
OMA_{TP3} max (dBm)	-10.50	Q = P + E
Power budget (dB)	6.80	R = O - Q
Unallocated margin (dB)	2.52	S = R - L

Unallocated margin for additional implementation losses

Conclusions

- A revised link budget assessment has been provided for all the data-rates included in the 802.3cz objectives based on recent VCSEL characterization
- The main objective of this presentation has been to demonstrate the 50 Gb/s PCS/PMA baseline proposal presented in [3] is even feasible with VCSELs just designed for 25 Gb/s NRZ
- **Nevertheless**, in the short term, characterization, reliability data, real-time transmission experiments, as well as link budget assessments will be provided for other VCSEL devices able to operate even faster and with better reliability in high temperatures, therefore allowing lower power consumption and lower complexity implementations (i.e. with reduced requirements of DSP like TX FFE and RX EQ)

References

- [1] R. Pérez-Aranda, “50 Gb/s demonstration in extreme temperatures using 850nm VCSELs,” May 2021, [Online], Available: https://www.ieee802.org/3/cz/public/…
- [2] R. Pérez-Aranda, “Reliability constrained link budget assessment for 25 and 10 Gb/s,” Dec 2020, [Online], Available: https://www.ieee802.org/3/cz/public/22_dec_2020/perezaranda_3cz_02a_221220_reliability_linkbdget.pdf
- [3] R. Pérez-Aranda, “50GBASE-AU baseline proposal,” May 2021, [Online], Available: https://www.ieee802.org/3/cz/public/…

Thank you!