50GBASE-AU baseline proposal

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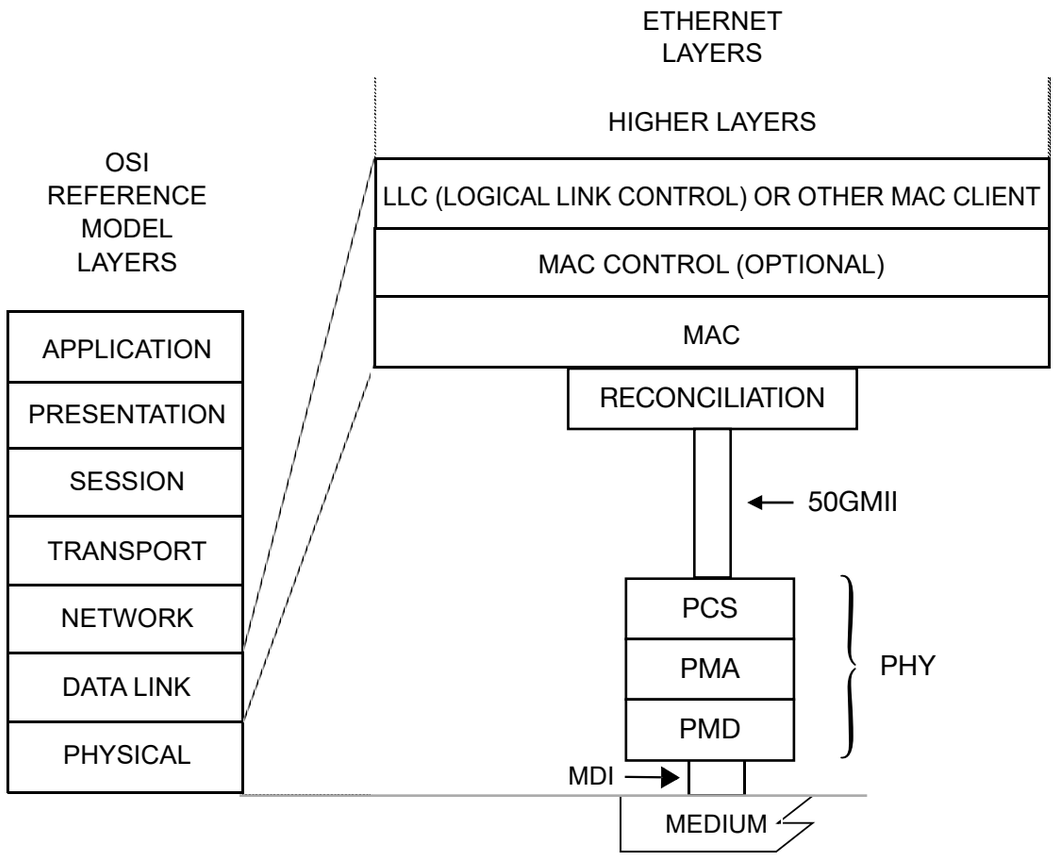
Introduction and objectives

- In [1] it was demonstrated that 50 Gb/s is feasible in extreme temperatures (-40ºC, 25ºC and 125ºC) using PAM4 modulation scheme, even using a VCSEL not designed for that aim, when the proper transmitter and receiver are used (i.e. TX FFE, RX timing-recovery & equalization, etc)
- In [2] a worst link budget assessment was presented for 50 Gb/s operation over 40 m OM3 fiber with 950 MHz·km EMB and 2 inline connections
- Both, [1] and [2] considered current densities below the limits reported in [3] to meet with the reliability and mission profile requirements

- This contribution is a **PCS** and **PMA** baseline proposal for **50 Gb/s** consistent with the presented link budget analysis and currently adopted PCS and PMA sublayers for 25, 10, 5 and 2.5 Gb/s
- This contribution does **NOT** include the needed extensions for optional **EEE**, however it does not preclude them. Baseline proposal for LPI is still pending
- This contribution does **NOT** include **PMD**, **MDI** and **medium** specifications

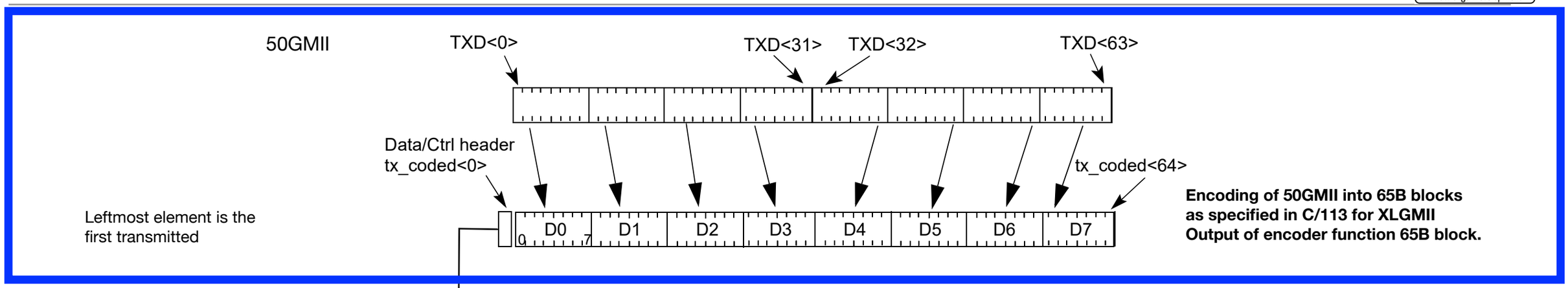
Reference models

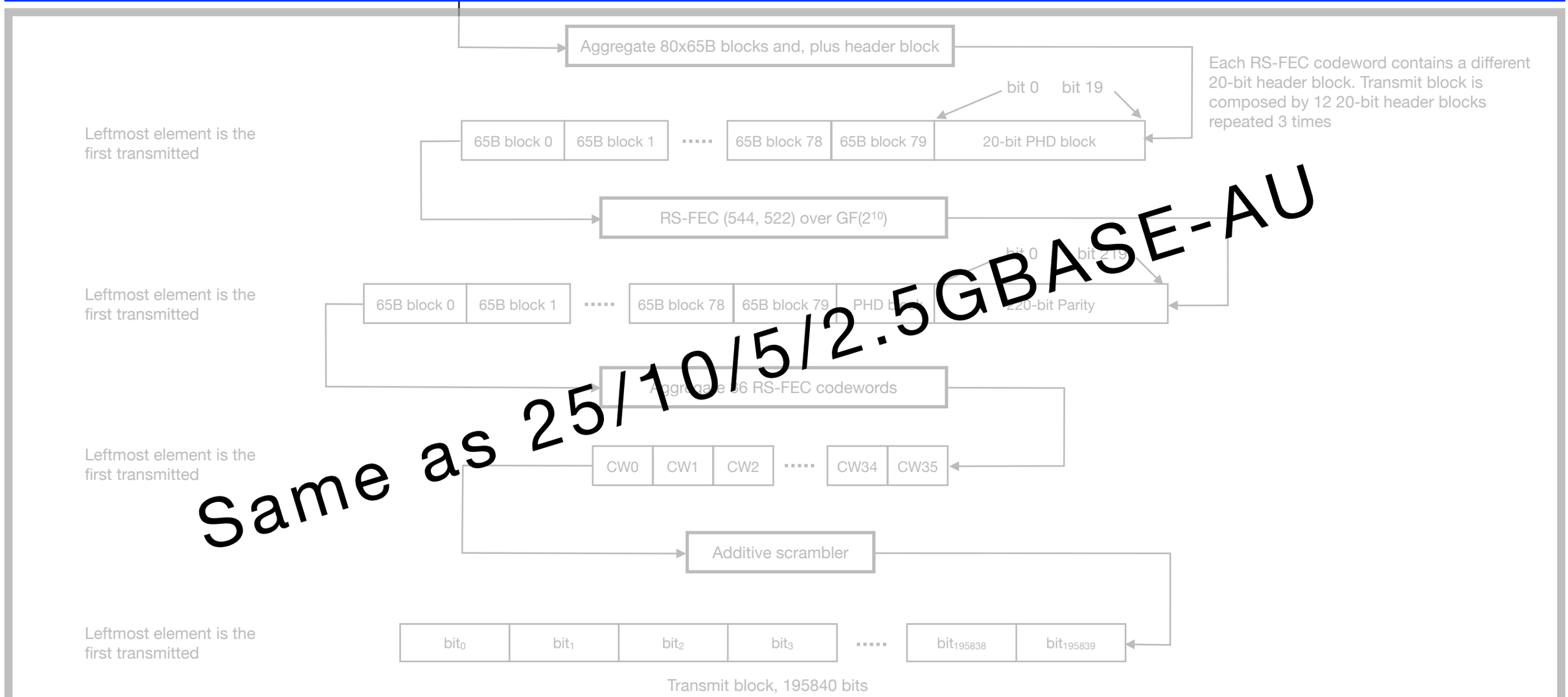


MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
50GMII = 50 GIGABIT MEDIA INDEPENDENT INTERFACE

Relationship of OMEGA PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

PCS transmit ordering





Same as 25/10/5/2.5GBASE-AU

PCS 64B/65B encoding (same as C/113)

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
D_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
C_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
S_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	1	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
O_0 D_1 D_2 D_3/Z_4 Z_5 Z_6 Z_7	1	0x4B	D_1	D_2	D_3	O_0	0x000_0000		
T_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
D_0 T_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
D_0 D_1 T_2 C_3/C_4 C_5 C_6 C_7	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
D_0 D_1 D_2 T_3/C_4 C_5 C_6 C_7	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
D_0 D_1 D_2 D_3/T_4 C_5 C_6 C_7	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
D_0 D_1 D_2 D_3/D_4 T_5 C_6 C_7	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
D_0 D_1 D_2 D_3/D_4 D_5 T_6 C_7	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
D_0 D_1 D_2 D_3/D_4 D_5 D_6 T_7	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 113–10—64B/65B block formats for 40GBASE-T

Table 113–2—Control codes for 40GBASE-T

Control character	Notation	XLGMII control codes	40GBASE-T control codes	40GBASE-T O code
idle	/I/	0x07	0x00	
LPI[a]	/LI/	0x06	0x06	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	

Table 113–2—Control codes for 40GBASE-T *(continued)*

Control character	Notation	XLGMII control codes	40GBASE-T control codes	40GBASE-T O code
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
Signal ordered set[b]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[a]Use of idle and LPI ordered sets per 81.3.
[b]Used by INCITS T11 Fibre Channel.

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a seven- bit control code or a four-bit O Code. Each control block contains eight characters.

The format of the blocks for 50GBASE-AU is as shown in Figure 113–10. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block.

The control characters and their mappings to 50GBASE-AU control codes and 50GMII control codes are specified in Table113–2 as for 40GBASE-T.

PCS binary scrambler

- Same binary scrambler as the one specified for 2.5, 5, 10 and 25GBASE-AU shall be used to scramble the 195840 bits composing the transmit block from the 36 RS codewords
- However, the shift register of the LFSR shall be initialized with a different value, searched to maximize the main correlation peak and to minimize the secondary correlation peaks, when Transmit Block synchronization is implemented by cross correlation functions (same criteria of [4])
  - Reset value needs to be re-calculated because both PAM4 modulation format with specific mapping is used and Local Fault sequential ordered sets are encoded in different way when 50GMII is encoded into 65-bit blocks
- The shift register shall be initialized with hexadecimal value 0x020492C for each transmit block, where the leftmost digit corresponds to the initial value of register element r[0]. The initial value of r[0] is xor-ed with the first bit from the first RS codeword to generate the first bit of the binary sequence that feeds the PAM4 mapper

PMA transmit function

- The PMA transmit function shall map the bits stream from PCS transmit function into PAM4 (Pulse Amplitude Modulation of 4 levels) symbols
- The PMA transmit function shall map pairs of consecutive bits into PAM4 symbols according to the following mapping function:
  - Bits $b_{2\cdot k}$ and $b_{2\cdot k+1}$ shall be mapped to symbol s_k, taking k values from 0 through 97919
  - For any k, the pair $\{b_{2\cdot k}, b_{2\cdot k+1}\}$ shall be mapped to s_k as follows
    - {0, 0} ➜ -1
    - {1, 0} ➜ -1/3
    - {1, 1} ➜ +1/3
    - {0, 1} ➜ +1
- The total number of symbols generated by the PMA transmit function shall be 97920 symbols per transmit block

PMD mapping

- The PMD transmit function shall convert the symbols stream from the PMA transmit function into optical symbols stream. The optical symbols stream shall then be delivered to the MDI, according to the transmit optical specifications (not included in this contribution).
- PAM4 symbols mapping into PMD optical intensity modulation levels
  - $s_k = -1$ ➜ Lowest optical power level (P_0), after transient
  - $s_k = -1/3$ ➜ $P_0 + 1/3 \cdot (P_1 - P_0) = 2/3 \cdot P_0 + 1/3 \cdot P_1$
  - $s_k = +1/3$ ➜ $P_0 + 2/3 \cdot (P_1 - P_0) = 1/3 \cdot P_0 + 2/3 \cdot P_1$
  - $s_k = +1$ ➜ Highest optical power level (P_1), after transient
  - $ER_{outer} = P_1/P_0$
  - $OMA_{outer} = P_1 - P_0$

Timing parameters

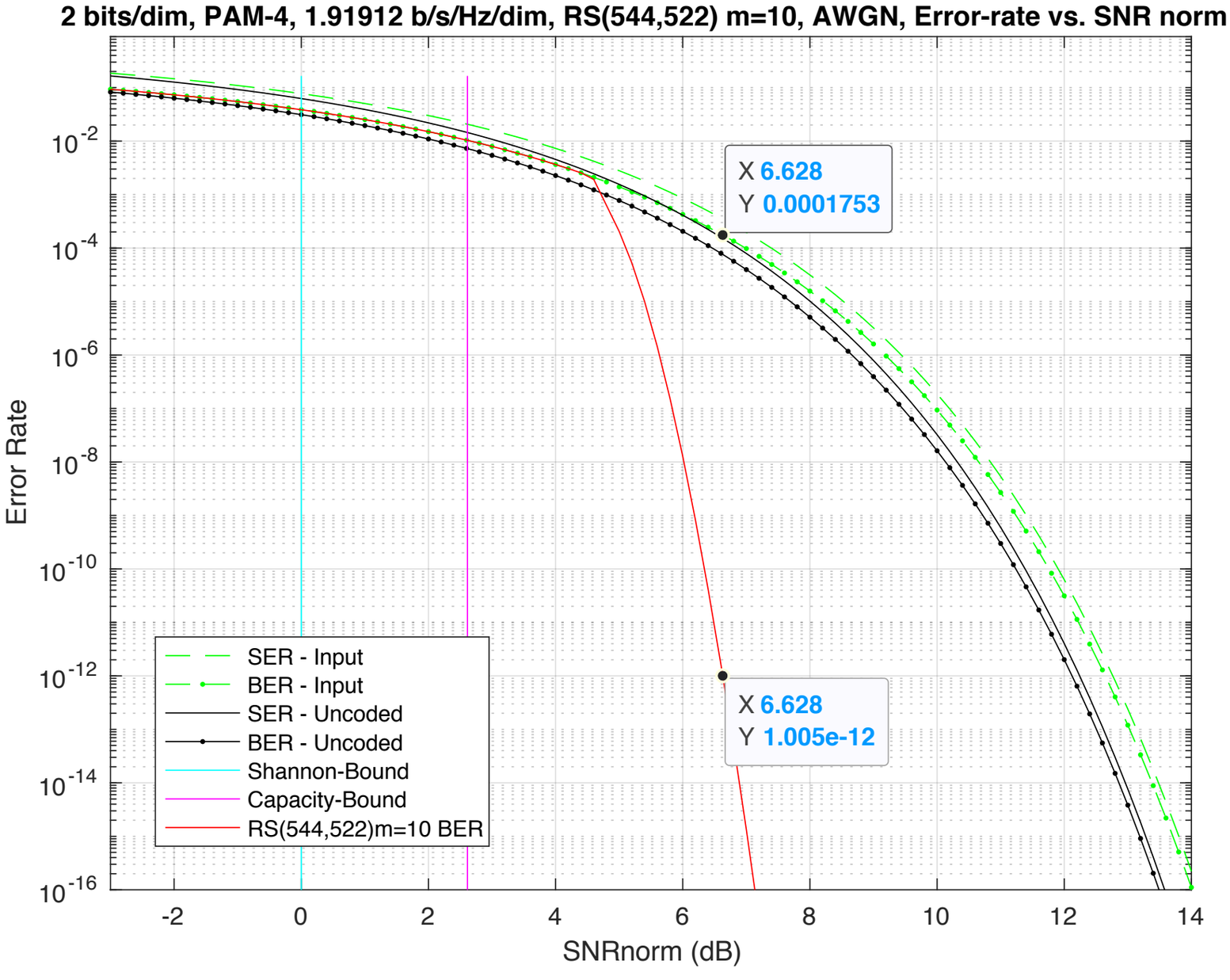
- The symbol transmission rate of the PHY shall be 26.5625 GBd +/- 100 ppm

Parameter	Value
xMII Data-rate (Mb/s)	**50000**
PAM m	**4**
RS m	10
RS t	11
RS n	544
RS k	522
RS cr	0.9596
PCS n	65
PCS k	64
PHD block per RS CW (bits)	20
BaudRate (MBd)	26562.5
Ref Clock (MHz)	156.25
Clock Factor	170
PHD info (bits)	224
PHD crc (bits)	16
PHD block (bits)	240
PHD repetition (times)	3
PHD TRC length (bits)	720
RS CWs/block	36
TX block length (bits)	195840
TX block length (symbols)	97920
TX block duration (us)	3.6864
FIFO latency (ns)	225.28
FIFO latency (bit-times)	11264
FIFO latency (pause-quantas)	22
PHD data-rate (Mb/s)	60.764
OAM net data-rate (Mb/s)	37.977

Common to all the BASE-AU PHYs

- Physical header data
- CRC16 calculation
- Reed-Solomon code
- PMA state variables
- PHY TX control state diagram
- PHY RX control state diagram
- Link monitor state diagram
- Local PHD reception monitor state diagram
- Remote PHD reception monitor state diagram
- PHD monitor state diagram
- PHY quality criterion
- PHY quality monitor state diagram
- OAM channel

Reed-Solomon code — performance with PAM4




```
Channel: AWGN
RS(544,522) m = 10
Spect. Eff.: 1.91912 b/s/Hz/dim
Shannon gap (BER = 1e-12):          6.63 dB
Capacity bound gap (BER = 1e-12): 4.01 dB
SNR (BER = 1e-12):                  17.88 dB
Coding gain (BER = 1e-12):          5.49 dB
Input SER (BER = 1e-12):            0.00034625
```

References

- [1] R. Pérez-Aranda, “50 Gb/s demonstration in extreme temperatures using 850nm VCSELs,” May 2021, [Online], Available: https://www.ieee802.org/3/cz/public/…
- [2] R. Pérez-Aranda, “Revised link budget assessment,” May 2021, [Online], Available: https://www.ieee802.org/3/cz/public/…
- [3] R. Pérez-Aranda, “Reliability constrained link budget assessment for 25 and 10 Gb/s,” Dec 2020, [Online], Available: https://www.ieee802.org/3/cz/public/22_dec_2020/perezaranda_3cz_02a_221220_reliability_linkbdget.pdf
- [4] R. Pérez-Aranda, “Scrambler initialization based on training sequence,” April 2021, [Online], Available: https://www.ieee802.org/3/cz/public/mar_2021/perezaranda_3cz_02_0321_scrambler.pdf

Thank you!