



PAM4 50 Gb/s PCS/PMA

Answers to unasked questions

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Motivation



- In [4] (May 11th) a PCS and PMA baseline was proposed for 50 Gb/s, which is consistent with [1], [2], [3] and the currently adopted PCS and PMA sublayers of 25, 10, 5 and 2.5 Gb/s
 - No questions were received for clarification and/or discussion
 - Straw poll, with potential motion, was announced for May 18th
- In [5] (May 18th) a straw poll was conducted to measure the support level of [4] by the Task Force
 - A summary of the PCS/PMA proposal was provided
 - No questions were received for clarification and/or discussion
- Straw poll passes with 92.6%, $25/(25 + 2)$
- Then the motion failed with 58.8%, $10/(10 + 7)$
- This contribution is intended to provide answers to unasked questions intended to give argumentation to support the baseline proposal of [4]
- The author of this contribution is open to answer and discuss any technical question about the proposal of [4]

Arguments supporting [4]

- Decision about modulation scheme for 50 Gb/s has taken more than one year in my side because we had to wait until testing VCSEL devices able to operate more linearly in very low and very high temperatures
 - One year ago the tested VCSELs in my side were not so linear in extreme temperatures to support 50Gb/s PAM4
 - Neither fast enough in extreme temperatures to support 50 Gb/s NRZ
- However, the last two reports using 850nm [1], and more clearly 980nm [3], demonstrated that PAM4 is very feasible in extreme temperatures for 50 Gb/s operation
- [6] demonstrated that there are no reliability constraints in 980nm VCSELs to use higher current densities in high temperature operation that makes the 50 Gb/s PAM4 PHY implementation easier

Arguments supporting [4]



- From the digital and analog mixed-signal circuits point of view PAM4 makes more sense than NRZ:
 - SNR after EQ for $BER < 10^{-12}$ after FEC : 17.28 dB required for PAM4 vs 11.07 dB, which would imply 1.1 bits ENOB extra in the ADC, assuming same level of ISI in the TIA output
 - Simulation model was used to validate that not more than 1.1 bits are needed in the ADC
 - Same ADC would be valid for 50Gb/s PAM4 and 25Gb/s NRZ
 - In case of NRZ, the precision demanded from ADC would be lower (1.1 bit), however, the sampling rate double
 - These kind of very high speed data converters follow time-interleaving architecture
 - Therefore doubling sampling rate means doubling silicon area
 - The same happen with the DSP digital path, which requires of parallel topologies
 - With PAM4, we would have 10% depth increase in the digital signal processing
 - However, with NRZ we will have double area
 - Same DSP would be valid for 50Gb/s PAM4 and 25Gb/s NRZ
 - Taking into account the bandwidth limitations of VCSEL and photodiodes as well as gain-bandwidth product limitations of the automotive grade technology processes in high temperatures, it is concluded the ISI to be compensated in NRZ will be much higher than in case of PAM4
 - This will impact in higher number of taps (>2x) and higher precision circuits (>25%) for NRZ
 - In summary: NRZ complexity > 2x PAM4 complexity, in terms of DSP and AMS blocks
 - In summary: NRZ power consumption > 2x PAM4 power consumption, in terms of DSP and AMS blocks

Arguments supporting [4]

- From the clock jitter point of view, the simulation indicates no big differences:
 - 50 Gb/s NRZ \rightarrow $t_j < 0.35$ psRMS @ 53.125 GHz
 - 50 Gb/s PAM4 \rightarrow $t_j < 0.3$ psRMS @ 26.5625 GHz
- From the RIN point of view, similar specification:
 - PAM4: RIN < 128 dB/Hz @ $BW_n = 20.7$ GHz
 - NRZ: RIN < 128 dB/Hz @ $BW_n = 41.3$ GHz
- From the data interfaces point of view: the electrical serial interfaces used today for 50 Gb/s are PAM4, therefore it is more natural to use PAM4, so similar baud-rate is used in the whole IC
- From PLL and TIA points of view:
 - Using PAM4 in 50 Gb/s makes the 50 Gb/s PHY development easier reusing same PLL and similar TIA topology, because same clock frequency and bandwidth are required

Arguments supporting [4]



- Extra advantages for PAM4:
 - No extra investment is necessary in laboratory equipment (development and acquisition)
 - Same bandwidth limitations for 50 Gb/s and 25 Gb/s
 - Easier to standardize
 - More synergies with photonics industry: e.g. 50GBASE-SR
 - The PAM4 PCS/PMA baseline proposal of [4] shares everything with the currently adopted 25G/10G/5G/2.5G NRZ baseline.
The delta is:
 - PCS 64B/65B → that needs to be different in any case due to 50GMII encoding is different of 25GMII
 - PAM4 mapping
 - Scrambler LFSR init value
 - All of them have little impact in the implementation
- **Therefore, the proposed 50G PCS/PMA baseline of [4] makes straightforward the implementation of an IC able to support all the data-rates allowing maximum reuse of all the HW blocks without multiplicities and extra cost and with optimal power consumption**

References



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- [2] R. Pérez-Aranda, “Revised link budget assessment,” May 2021, [Online], https://www.ieee802.org/3/cz/public/11_may_2021/perezaranda_3cz_02_110521_revised_link_budget.pdf
- [3] R. Pérez-Aranda, “980nm VCSEL Performance in extreme temperatures,” May 2021, [Online], Available: https://www.ieee802.org/3/cz/public/18_may_2021/perezaranda_3cz_01_180521_VCSEL_980nm.pdf
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- [5] R. Pérez-Aranda, “50GBASE-AU PCS and PMA baseline adoption,” May 2021, [Online], Available: https://www.ieee802.org/3/cz/public/18_may_2021/perezaranda_3cz_03a_180521_50G_strawpoll.pdf
- [6] R. King, “VCSEL design for automotive datacom Experimental results for 980 nm versus 850 nm,” https://www.ieee802.org/3/cz/public/18_may_2021/king_3cz_01a_180521.pdf



Thank you!