# Clause 45

Proposed Clause 45 text for 10BASE-T1M PHY.

This text modifies the 10BASE-T1S definitions to apply to both 10BASE-T1S and 10BASE-T1M and notes any exceptions.

**45.2.1 PMA/PMD registers**

***Modify the rows below to Table 45–3—PMA/PMD registers***

|  |  |  |
| --- | --- | --- |
| Register address | Register name | Subclause |
| 1.2297 | 10BASE-T1S/T1M PMA control | 45.2.1.234 |
| 1.2298 | 10BASE-T1S/T1M PMA status | 45.2.1.235 |
| 1.2299 | 10BASE-T1S/T1M test mode control | 45.2.1.236 |

**45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)**

***Add/modify the rows below to Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions***

|  |  |  |  |
| --- | --- | --- | --- |
| Bit(s) | Name | Description | R/W |
| 1.18.15:9 | Reserved | Value always 0 | RO |
| 1.18.8 | 10BASE-T1M ability | 1 = PMA/PMD is able to perform 10BASE-T1M | RO |
|  |  | 0 = PMA/PMD is not able to perform 10BASE-T1M | RO |

**45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)**

***Modify the rows below in Table 45–149—BASE-T1 PMA/PMD control register bit definitions***

|  |  |  |  |
| --- | --- | --- | --- |
| Bit(s) | Name | Description | R/W |
| 1.2100.3:0 | Type Selection | 3 2 1 0  Other values reserved.  1 0 0 0 = 10BASE-T1M  0 1 1 1 = 25GBASE-T1  0 1 1 0 = 10GBASE-T1  0 1 0 1 = 5GBASE-T1  0 1 0 0 = 2.5GBASE-T1  0 0 1 1 = 10BASE-T1S  0 0 1 0 = 10BASE-T1L  0 0 0 1 = 1000BASE-T1  0 0 0 0 = 100BASE-T1 | R/W |

**45.2.1.214.2 Type selection (1.2100.3:0)**

***Change as follows:***

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one. The mapping of bits is as follows:

* 0000 - 100BASE-T1
* 0001 - 1000BASE-T1
* 0010 - 10BASE-T1L
* 0011 - 10BASE-T1S
* 0100 - 2.5GBASE-T1
* 0101 - 5GBASE-T1
* 0110 - 10GBASE-T1
* 0111 - 25GBASE-T
* 1000 - 10BASE-T1M

**45.2.1.234 10BASE-T1S/T1M PMA control register (Register 1.2297)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The assignment of bits in the 10BASE-T1S/T1M PMA control register is shown in Table 45–150d.

**45.2.1.234.1 PMA reset (1.2297.15)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

Resetting the 10BASE-T1S/T1M PMAs is accomplished by setting bit 1.2297.15 to one. This action shall set all PMA registers to their default states. This action may change the internal state of the PMA and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the PMA shall return a value of one in bit 1.2297.15 when a reset is in progress; otherwise, it shall return a value of zero. The PMA is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2297.15.

During a reset, the PMA shall respond to reads from bits 1.2297.15, 1.8.15:14, and 1.0.15. All

other register bits should be ignored.

NOTE—This operation may interrupt communication.

Bit 1.2297.15 is a copy of 1.0.15, and setting or clearing either bit shall set or clear the other bit. Setting

either bit shall reset the PMA.

**45.2.1.234.3 Low-power (1.2297.11)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

When the low-power ability is supported, the 10BASE-T1S/T1M PMA may be placed into a low-power mode by

setting bit 1.2297.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PMA. The behavior of the PMA in transition to and from the low-power mode is implementation specific, and any interface signals should not be relied upon. While in the low-power mode, the device shall respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2297.11 is zero.

NOTE—The time from low-power mode to full operation is implementation specific.

Bit 1.2297.11 is a copy of bit 1.0.11, and setting or clearing either bit shall set or clear the other bit. Setting

either bit shall put the PMA in low-power mode.

**45.2.1.234.4 Multidrop mode (1.2297.10)**

***Add the following after the existing text:***

For 10BASE-T1M this bit is always set to 1 and writing to bit 1.2297.10 shall have no effect.

**45.2.1.234.5 Loopback (1.2297.0)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The 10BASE-T1S/T1M PMA shall be placed in loopback mode of operation when loopback bit 1.2297.0 is set to

one. When in loopback mode, the PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2297.0 is zero. Bit 1.2297.0 is a copy of 1.0.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

**45.2.1.235 10BASE-T1S/T1M PMA status register (Register 1.2298)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The assignment of bits in the 10BASE-T1S/ T1M PMA status register is shown in Table 45–197.

**Table 45–197 - 10BASE-T1S/T1M PMA status register bit definitions**

**45.2.1.235.1 10BASE-T1S/T1M loopback ability (1.2298.13)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

When read as a one, this bit indicates that the 10BASE-T1S/T1M PHY supports PMA loopback. When read as a zero, this bit indicates that the PHY does not support PMA loopback.

**45.2.1.235.2 Low-power ability (1.2298.11)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

When read as a one, bit 1.2298.11 indicates that the 10BASE-T1S/T1M PMA supports the low-power ability. When read as a zero, bit 1.2298.11 indicates that the PMA does not support the low- power feature. If the 10BASE- PMA supports the low-power feature, then it is controlled using either bit 1.2297.11 or bit .0.11.

**45.2.1.235.3 Multidrop ability (1.2298.10)**

***Add the following after existing text:***

For 10BASE-T1M this bit is always set to 1 and writing to bit 1.2297.10 shall have no effect.

**45.2.1.235.4 Receive fault ability (1.2298.9)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

When read as a one, bit 1.2298.9 indicates that the 10BASE-T1S/T1M PMA can detect a fault condition on the receive path. When read as a zero, bit 1.2298.9 indicates that the PMA does not have the ability to detect a fault condition on the receive path.

**45.2.1.235.5 Receive fault (1.2298.1)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

When read as a one, bit 1.2298.1 indicates that the 10BASE-T1S/T1M PMA has detected a fault condition on the

receive path. When read as a zero, bit 1.2298.1 indicates that the PMA has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional, and the ability to detect such a condition is advertised by bit 1.2298.9. The PMA that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. This bit shall be implemented with latching high behavior.

**45.2.1.236 10BASE-T1S/T1M test mode control register (Register 1.2299)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The assignment of bits in the 10BASE-T1S test mode control register is shown in Table 45–150 - 10BASE-T1S/T1M test mode control register bit definitions”. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**45.2.3 PCS registers**

***Change Table 45–233—PCS registers as follows (unchanged rows not shown):***

|  |  |  |
| --- | --- | --- |
| Register address | Register name | Subclause |
| 3.2291 | 10BASE-T1S/T1M PCS control | 45.2.3.72 |
| 3.2292 | 10BASE-T1S/T1M PCS status | 45.2.3.73 |
| 3.2293 | 10BASE-T1S/T1M PCS diagnostic 1 | 45.2.3.74 |
| 3.2294 | 10BASE-T1S/T1M PCS diagnostic 2 | 45.2.3.75 |

**45.2.3.72 10BASE-T1S/T1M PCS control register (Register 3.2291)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The assignment of bits in the 10BASE-T1S/T1M PCS control register is shown in Table 45–237c. The default

value for each bit of the PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**Table 45–298 —10BASE-T1S/T1M PCS control register bit definitions**

**45.2.3.72.1 PCS reset (3.2291.15)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

Resetting the 10BASE-T1S/T1M PCS is accomplished by setting bit 3.2291.15 to one. This action shall set all PCS registers to their default states. Consequently, this action may change the internal state of the PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the PCS shall return a value of one in bit 3.2291.15 when a reset is in progress; otherwise, it shall return a value of zero. The PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2291.15. During a reset, a PCS shall respond to reads from bits 3.0.15, 3.8.15:14, and 3.2291.15. Reads for all other bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2291.15 is a copy of 3.0.15, and setting or clearing either bit shall set or clear the other bit. Setting

either bit shall reset the PCS.

**45.2.3.72.2 Loopback (3.2291.14)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The 10BASE-T1S/T1M PCS shall be placed in a loopback mode of operation when bit 3.2291.14 is set to one.

When in loopback mode, the PCS shall accept data on the transmit path and return it on the receive path.

**45.2.3.72.3 Duplex mode (3.2291.8)**

***Add the following after the existing text:***

This bit shall be ignored for the 10BASE- T1M pcs.

**45.2.3.73 10BASE-T1S/T1M PCS status register (Register 3.2292)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The assignment of bits in the 10BASE-T1S/T1M PCS status register is shown in Table 45–237d. All the bits in

the PCS status register are read only; a write to the PCS status register shall

have no effect.

**45.2.3.73.1 Fault (3.2292.7)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

When read as a one, bit 3.2292.7 indicates that the 10BASE-T1S/T1M PCS has detected a fault condition on either the transmit or receive path. When read as a zero, bit 3.2292.7 indicates that the PCS has not detected a fault condition. This bit shall be implemented with latching high behavior.

**45.2.3.74 10BASE-T1S/T1M PCS diagnostic 1 (Register 3.2293)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The assignment of bits in the 10BASE-T1S/T1M PCS diagnostic 1 register is shown in Table 45–237e. All the bits in the PCS diagnostic 1 register are read only and self-clear on read; a write to the PCS diagnostic 1 register shall have no effect.

**45.2.3.75 10BASE-T1S PCS diagnostic 2 (Register 3.2294)**

***Change as follows so that it applies equally to 10BASE-T1S & T1M:***

The assignment of bits in the 10BASE-T1S/T1M PCS diagnostic 2 register is shown in Table 45–237f. All the bits in the PCS diagnostic 2 register are read only and self-clear on read; a write to the diagnostic 2 register shall have no effect.

Table 45–301—10BASE-T1S/T1M PCS diagnostic 2 register bit definitions

**45.2.3.1.2 Loopback (3.0.14)**

***Change as follows:***

Replace

When the 100BASE-T1, any MultiGBASE-T, or the 5/10GBASE-R mode of operation is selected for the

PCS using the PCS type selection field (3.7.3:0), the PCS shall be placed in a loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 100BASE-T1, 5/10GBASE-R, or any PCS in the MultiGBASE-T set shall accept data on the transmit path and return it on the receive path. The speed of the loopback is selected by the PCS control 1 (register 3.0) defined in 45.2.3.1. The specific behavior of the 100BASE-T1 PCS during loopback is specified in 96.3.5. The specific behavior of the 5/10GBASE-R PCS during loopback is specified in 49.2. The specific behavior for the 10GBASE-T PCS during loopback is specified in 55.3.7.3. The specific behavior for the 25GBASE-T and 40GBASE-T PCS during loopback is specified in 113.3.7.3. The specific behavior for the 2.5GBASE-T or 5GBASE-T PCS during loopback is specified in 126.3.7.3. For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

With

Setting bit 3.0.14 to one for 100BASE-T1, any MultiGBASE-T or 5/10GBASE-R places the PCS into loopback. The PCS accepts data on the transmit path and returns it on the receive path. The speed of the loopback is selected by the PCS control 1 (register 3.0) defined in 45.2.3.1.

PCS specific behavior during loopback is defined in:

* 96.3.5 for 100BASE-T1.
* 49.2 for 5/10GBASE-R.
* 55.3.7.3 for 10GBASE-T PCS.
* 113.3.7.3 for 25GBASE-T and 40GBASE-T.
* 126.3.7.3 for 2.5GBASE-T or 5GBASE-T.

For all other PCSs, this functionality is not applicable. Writes to this bit shall be ignored and reads from this bit shall return a value of zero.