FEC for 802.3da

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Why?

- To meet objective (8) “Support operation in the noise environments for building, industrial, and transportation applications” listed at https://www.ieee802.org/3/da/802d3da_objectives.pdf
- May also contribute to other objectives:
  - (1) “Define performance characteristics of a mixing segment for 10Mb/s multidrop single balanced pair networks supporting up to **at least 16 nodes, for up to at least 50m reach**.”
  - (8) “Support addition and removal of a node or set of nodes to a continuously operating powered mixing segment” and

The Problem

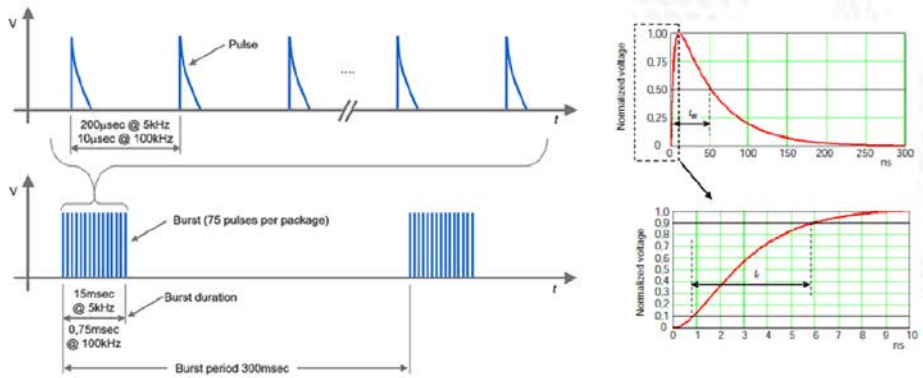
- Burst Noise from conducted interference
  - Tested in IEC 61000-4-4 & Seen in the Real World

Koczwara_Zimmerman_3SPMD_01_0120.pdf

Background: IEC 61000-4-4 test

Electrical Fast Transients (burst transients) are common mode disturbances coming from an arc when mechanical contact is open due to a switching process.

Similar disturbances could be observed from motor drivers and other load switching signals, if their cables bundled together with SPE cables.



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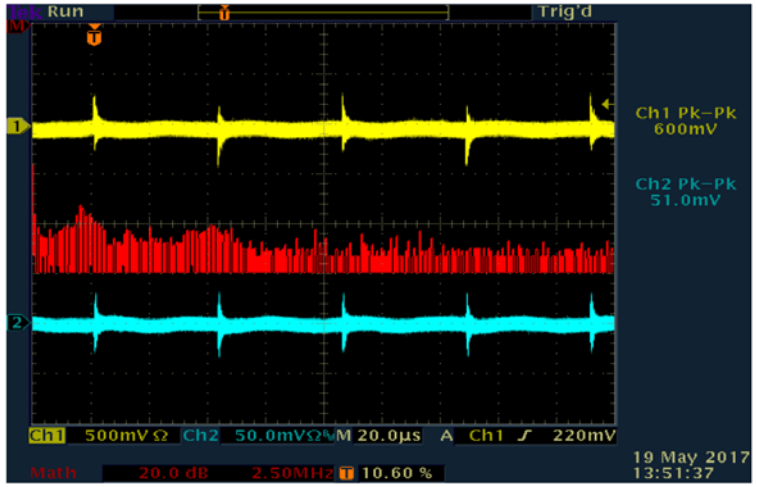
Setup: 20 cm cable separation, GND BALUN at Drive, 0 Hz
Measurements: Motor end



- ~10x voltage reduction
- Cable separation reduces Pk noise
- Visually appears to be 60 mV Pk-Pk

Potential Solutions & Challenges

- Allocating margin in the eye opening
  - Eats into reach/PHY/mixing segment complexity
- Cabling/front-end interference suppression
  - Shielding, common-mode rejection only work so far
- Burst-error (optional erasure) correcting FEC
  - Channel is a Binary Burst Error Channel with Optional Erasure Detection
  - Must be backward compatible with 10BASE-T1S without new overhead
  - May include per-frame configurable error/erasure resilience

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- All can be used in CONJUCTION

Reduced Reach & Installation complexity!

Installation & Analog Implementation Complexity!

Backward Compatibility & Digital Implementation

Requirements for FEC are well known

- Low complexity
  - Well-known codes
- Correct small bursts
  - 5 to 6 bits from IEC 61000-4-4 impulses
- Small block size
  - Needs to vanish in the packet size
- But backwards compatibility is the hard part…. Old nodes won't understand the code..

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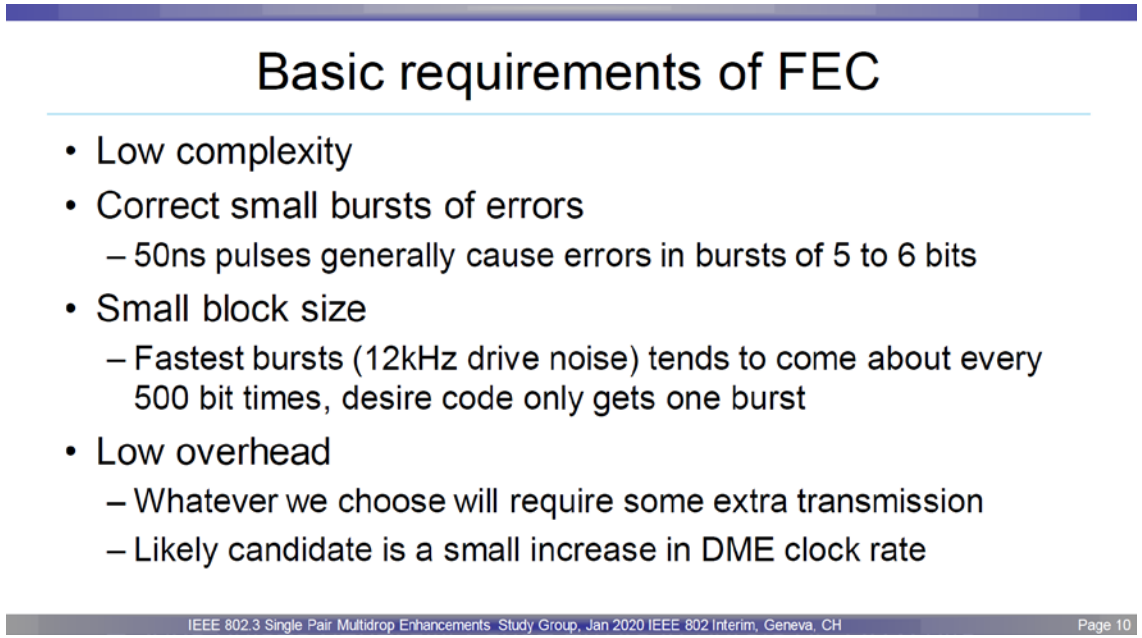


Basic requirements of FEC

- Low complexity
- Correct small bursts of errors
  - 50ns pulses generally cause errors in bursts of 5 to 6 bits
- Small block size
  - Fastest bursts (12kHz drive noise) tends to come about every 500 bit times, desire code only gets one burst
- Low overhead
  - Whatever we choose will require some extra transmission
  - Likely candidate is a small increase in DME clock rate

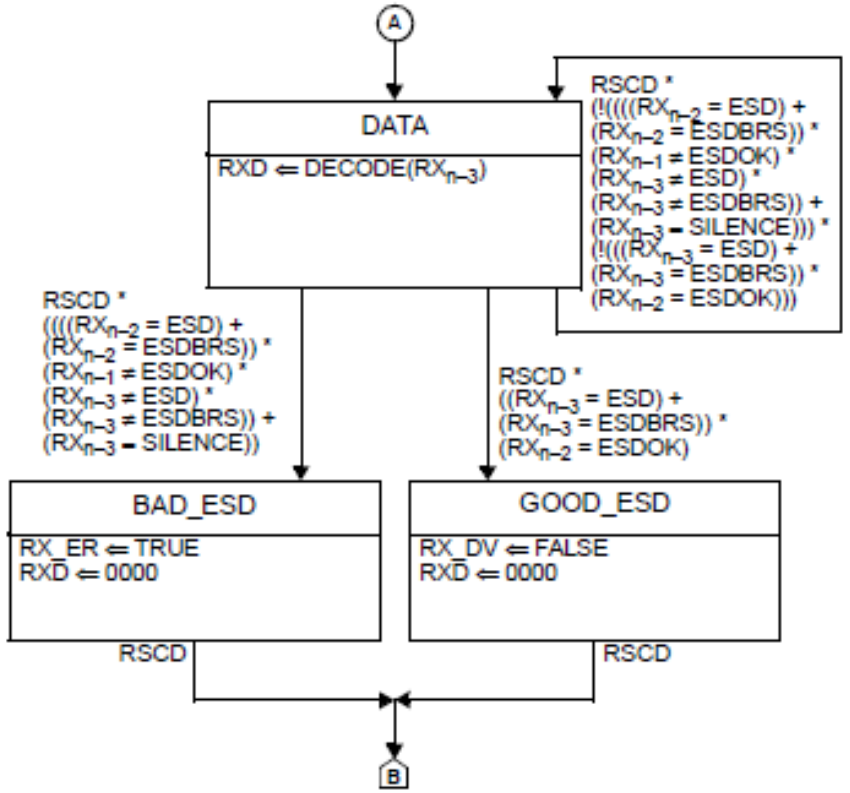
IEEE 802.3 Single Pair Multidrop Enhancements Study Group, Jan 2020 IEEE 802 Interim, Geneva, CH Page 10

Backward compatibility with Clauses 147-8

- Backwards compatibility with Clause 147:
  - DME modulation, 80 nsec bit time
  - Clause 147 encoding is used when talking to a Cl 147 PHY
  - Code is used only when talking to a “New” PHY (NPHY)
    - 4B/5B encoding overhead can be reused
    - Cl 147 PHY/MAC must predictably ‘discard with error’ so no junk packets are forwarded
- It should integrate with PLCA seamlessly

Ensuring Rejected Frames

- Lock Clause 147 PHYs PCS_RX/DATA state
  - Requires avoiding 3 5B symbols within a frame
    - “T” (ESD) = 01101
    - “R” (ESDOK/ESDBRS) = 00111
    - “I” (SILENCE) = 11111
  - Protected FEC_ESD requires a 4th symbol to be reserved
    - Only applicable for new PHYs
  - Remap these symbols



IEEE Std. 802.3cg-2019, Figure 147-8 (10BASE-T1S) PCS Rx State Diagram

Remapping the Symbols

- “Forbidden Symbols” are transcoded in the PCS
  - Details to be published shortly in an open paper
- Remapping must add no more latency than codeword
- Remapping must cover codeword parity symbols as well as message data
- Maintaining 80nsec DME time sets code

Proposed FEC: existence

- There exists a coding scheme that would map 19 4B data nibbles to 19 5B symbols, so that:
  - A single 5B symbol error (1-5 bits of error) may be corrected anywhere in the codeword
  - 1 or 2 5B symbol erasures (2-10 bits of erasure) may be corrected anywhere in the codeword
- The underlying code is a (19,17) MDS linear block code
  - (a shortened Reed-Solomon GF 32 code)
- Rate constraint (incl transcoding) precludes greater correction
- With interleaving, the burst error correcting capabilities may be increased arbitrarily

Proposed FEC: Encoding process

- Collect 19 4B symbols from MAC/PLS. For terminal symbols, pad those to 19 4B symbols
- Do a special remapping* that would map these to a FEC codeword with 19 5B symbols while maintaining backward compatibility with 10BASE-T1S
- Apply interleaving
- Transmit superblock
- Terminate the FEC stream by FEC_ESD
- Terminate the frame by T (ESD) then K (ESDERR)

* Expected to be available shortly via an open paper

Proposed FEC: Decoding process

- Collect a superblock of 5B symbols
- Deinterleave
- Apply the FEC decoder
- Reverse the encoding process

Proposed FEC: encoding delays

- Encoding delay is approximately the superblock size
- Encoding delay may be eliminated by systems where PHY and MAC are merged

Proposed FEC: interleaving

		Minimum error correcting capability, in bits	
Interleaving depth	Superblock size, in bits	For errors	For erasures
1 (no interleaving)	95	1	2
2	190	6	12
3	285	11	22
4	380	16	32

Next Steps

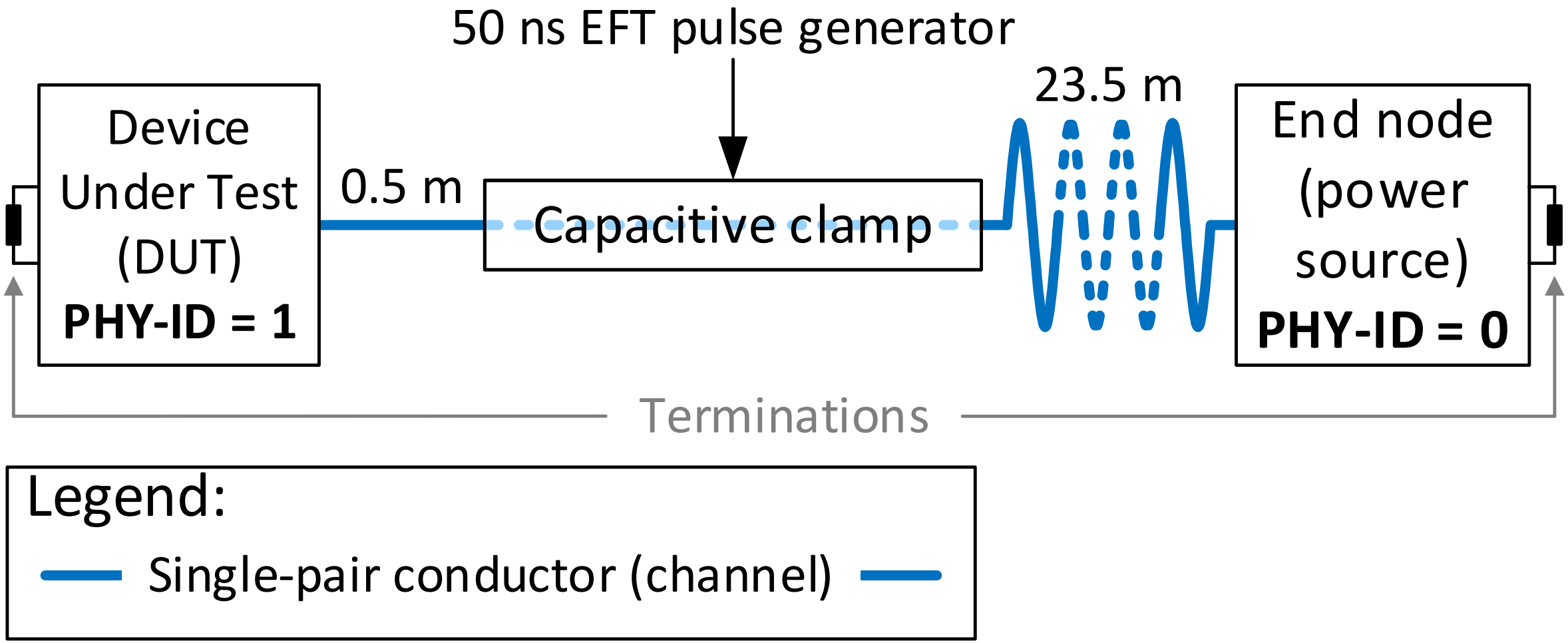
- Assuming this is an attractive way forward:
  - Continue disclosure of Remapping and Code
  - Discuss desired interleave parameters & control
  - Propose baseline for new PCS w/FEC
  - Consider other related enhancements
    - Preamble protection
    - Enabling future enhancements

Thanks for your kind attention

Any Questions?

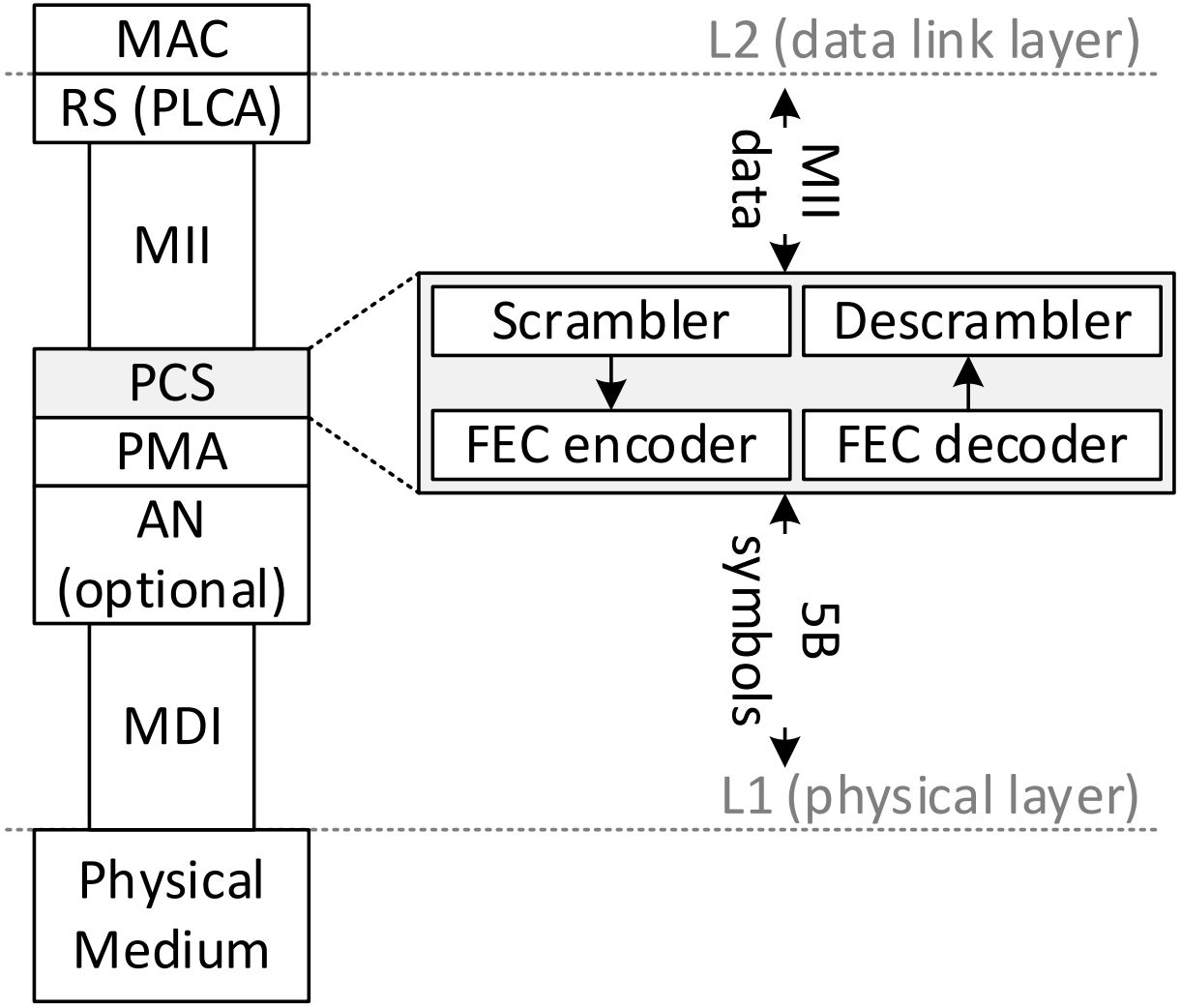
Backup Slides

IEC 61000-4-4 Electrical Fast Transient (EFT) tests



http://www.ieee802.org/3/SPMD/public/jan20/Koczwara_Zimmerman_3SPMD_01_0120.pdf

Location of FEC in a typical PHY with scrambler



Optimal bandwidth use

- If the rate of the code exceeds that of the 4B/5B encoding (namely r=0.8), then:
  - PHY needs buffers, as data is conveyed at 10Mbps at the MAC/PLS
  - The PHY cannot offer 10Mbps throughput
- If the preamble is inflated (beyond 16 nibbles), the PHY needs a delay line
- Extension of the ESD mechanism slightly decreases channel throughputs but the effect of this is calculable and is limited