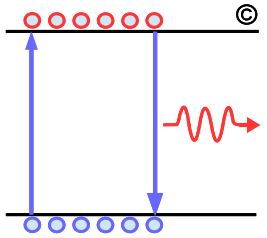


# Background on TDECQ Equalizer and Equalizer Options for 50 m PMDs

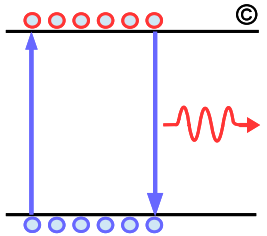
**Ali Ghiasi**

**Ghiasi Quantum LLC**

**IEEE 802.3db Task Force Meeting**

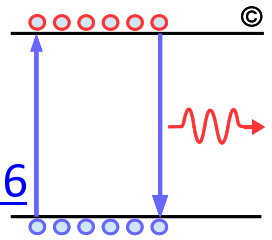
**July 19, 2021**

# Overview



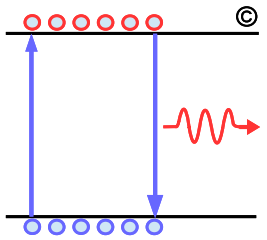
- **Background on TDECQ reference equalizer**
  - 5T vs 9T equalizer
  - Addressing comment 71 on D1.1
- **Background on threshold adjust**
  - Benefit of increasing threshold adjust from 1% to 2%
  - Addressing comment 72 on D1.1.

# Background on TDECQ



- **802.3bs reference equalizer and TDECQ initially defined based on 5 T/2 FFE**
  - Based on the view that 5 taps FFE will allow analog lower power CDRs, see king_3bs_01a_0516
    - king_3bs_03a_0916 contribution corrected TDECQ equation
  - 5 T/2 was chosen for CDR simplicity based on assumed up to 7 taps FFEs are feasible with analog implementations
- **Follow on contributions in 802.3bs indicated that 5 T/2 FFE with span of just 2.5 UI not sufficient to equalize 53 GBd PAM4**
  - Traverso contributions shows both error floor and substantial penalty with just 5 T/2 FFE
  - In D3.1 the reference equalizer was changed to 5T FFE
  - The reference equalizer BW was also reduced from 38.68 GHz to 26.55 GHz based on Mr. King view regarding T-spaced FFE potential aliasing issue
- **The thinking was that 5T FFE would be overall simpler than 10 taps T/2**
  - Another concern with 10 taps T/2 was that such equalizer can be setup for Nyquist shaping which is not possible with T-sampled DSP implementations
  - Existing DSP based on 10+ T-spaced FFE will enable the market but future simpler analog 5-7 T-spaced FFE are not ruled out
- **Our initial assumption regarding emergence of lower power 5-7 taps analog FFEs have not materialized**
  - Over the last 5 years CMOS nodes reduction has closed the gap between analog and DSP implementation.

# From 802.3ck Task Force

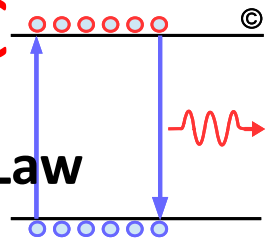


- **From sun_3ck_01a_0918 and ghiasi_3ck_02_1118 show comparisons of several receiver architecture including ADC and analog FFE**
  - Assumes 16 nm CMOS.

| Architecture | Balanced EQ (1. Asymmetric, 2. symmetric) | 3. Analog DFE ** | 4. ADC Based | 5. Analog FFE |
|---|---|---|---|---|
| Equalization | TX: FIR (2/4 taps for asymmetric structure, 2/11 taps for symmetric structure)<br>RX: CTLE | TX: FIR (2/4)<br>RX: CTLE, with DFE taps | TX: FIR (2/4)<br>RX: CTLE, 6-bit ADC, 8 postcursor digital FFE | TX: FIR(2/4)<br>RX:CTLE, Analog 5-7 tap FFE |
| TX Power*(mW) | 196<br>224 (symmetric structure) | ~~196~~ *157mW | ~~196~~ *157mW | 157 mW<br>(by scaling TX of [5] from 64 Gb/s to 112 Gb/s) |
| RX Power (mW) | 239<br>(by scaling [6]) | 436<br>(by scaling [3], 2 DFE tail tap power is very low) | 498<br>(310 by scaling [5] front end for 13.6dB channel; 108 for FFE by scaling FIR of [7] for 6b input; 80 for PLL, deserializer and CDR) | 220 mW<br>(by scaling [6] to 112G)<br>+60 mW for 7 T FFE<br>Total RX Power=280 mW |
| Relative total Power (mW) | **0** (435 as Baseline for asymmetric)<br>**28** (463 for symmetric) | **197**<br>(total 632) | **259**<br>(total 694) | +2 mW<br>(total power 437 mW) |
| Power Difference for 2x400G Module C2M at 106.25G (mW) | **0** for asymmetric (Total 3480)<br>**224** for symmetric (Total 3704) | ~~**1,576**~~ 1269 mW<br>(Total ~~**5056**~~ 4744 mW) | ~~**2,072**~~ 1760 mW<br>(Total ~~**5552**~~ 5240 mW) | +16 mW<br>(total 3480) |
| Projection with 30% reduction (mw)*** | **0** for asymmetric (Total 305)<br>19 for symmetric (Total 324) | ~~137~~ (total 442)<br>110 (total 415) | ~~181~~ (total 486)<br>154 (total 459) mW | 0 Analog FFE (Total 305 mW) |

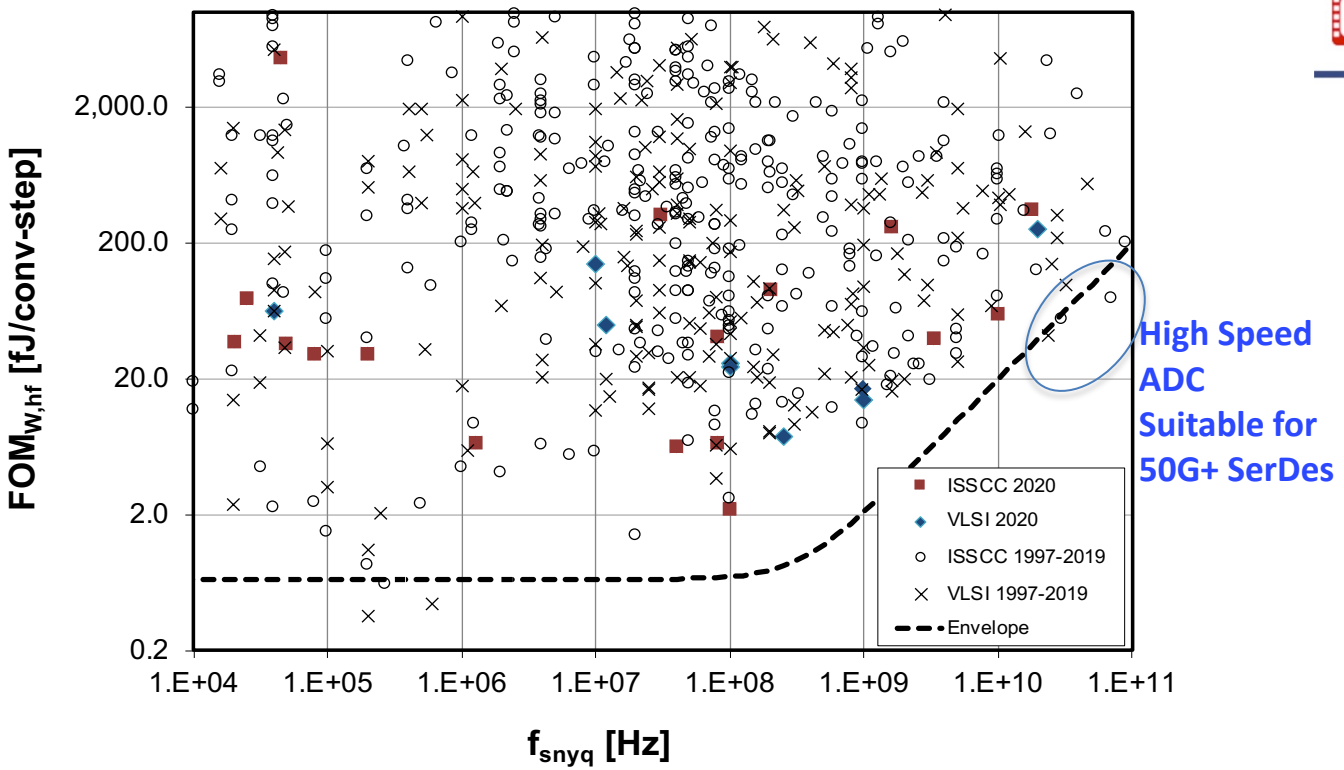
*** Expected reduction for 7 nm CMOS

# DSP SerDes Power Have Been Dominated by ADC



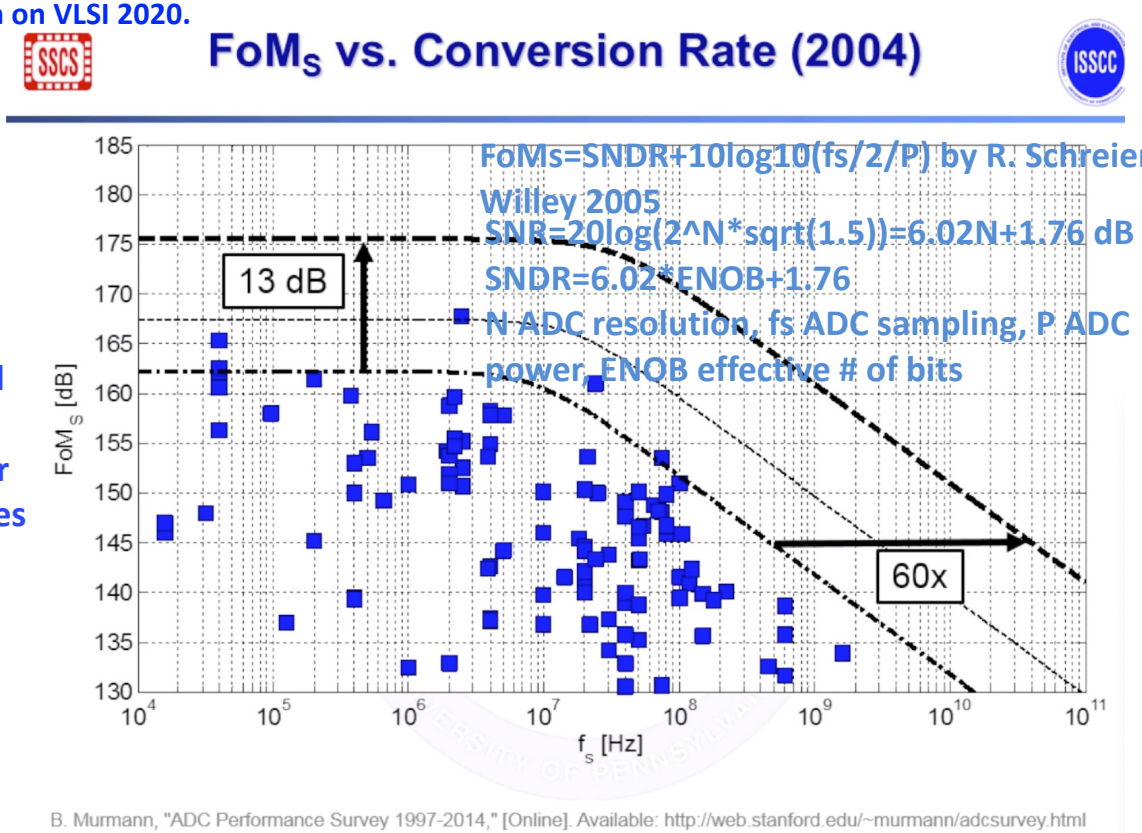
- **ADC have been improving at at rate of 2x/14 months which is faster than Moore's Law**
  - The drawback of DSP SerDes has been ADC power dissipation
  - 112 Gb/s 7 bits SAR ADC capable of 36 dB Cu reported PD is <200* mW 7 nm CMOS (include clocking power).

* H. Lin, et. al., A 4×112 Gb/s ADC-DSP Based Multi-standard Receiver in 7nm FinFET, Symposium on VLSI 2020.



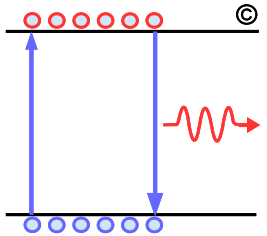

ADC Performance Survey 1997-2021," [Online]

See https://web.stanford.edu/~murmann/adcsurvey.html

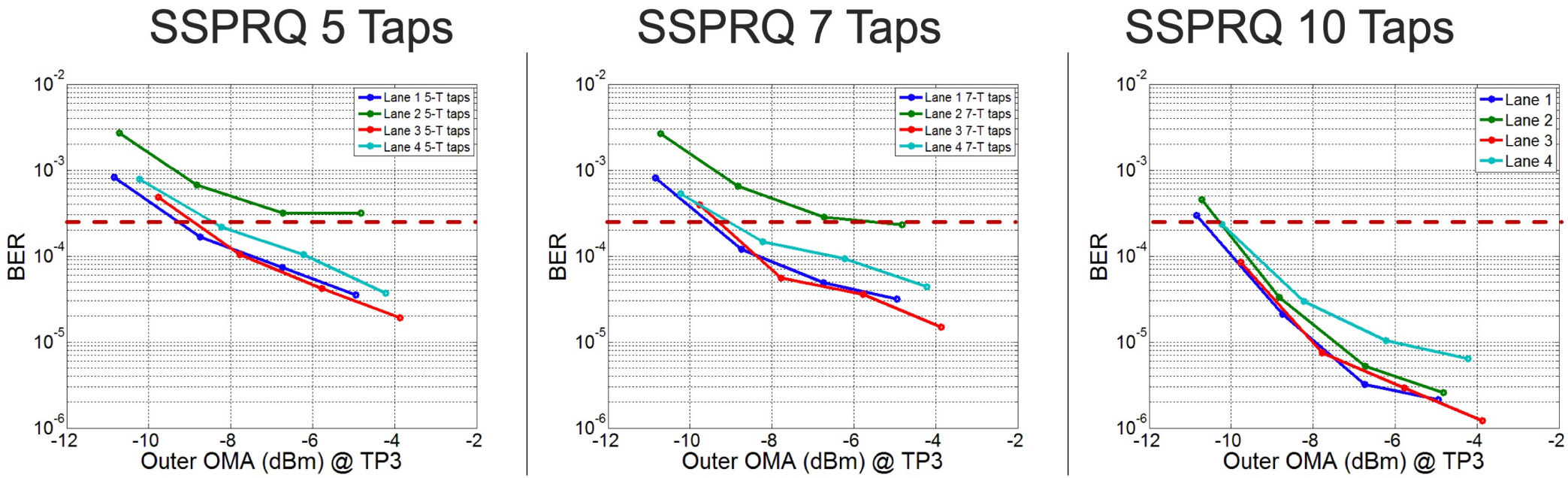



B. Murmann, "ADC Performance Survey 1997-2014," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

# Even for SMF 7T/9T FFE Showed Performance Benefit

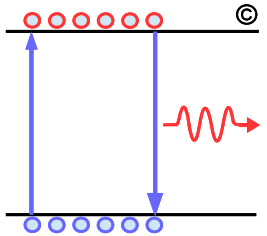


- **Toward the end of 802.3bs project [way_3bs_01a_0717]() brought forward proposal to increase 5T FFE to 7 or 9 T FFE but it was too late to make the change!**




> 7 T-taps make a significant difference in BER

# Way Results Showed Unallocated Margin in the Receiver

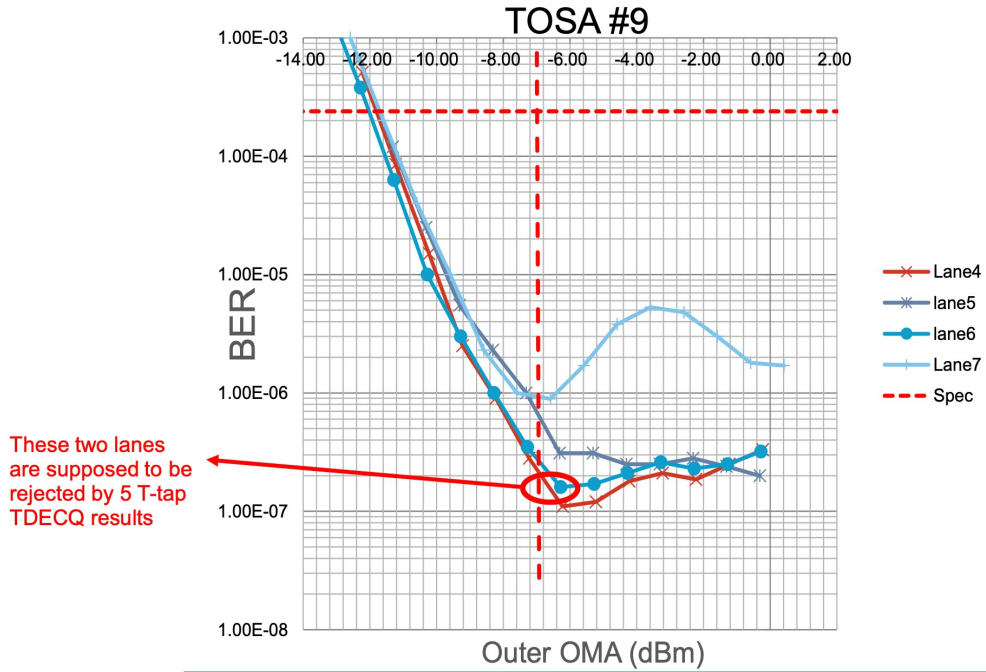


- **Unallocated margin way_3bs_01a_0717 is seeing is due to digital receiver having 5+ T FFE+ architecture**
  - Given the availability of this unallocated margin and VR cost objective the 9T TDECQ equalizer may offer better cost optimization

**All lanes ON and modulated**

| Lane | 5T | 7T | 9T |
|---|---|---|---|
| 4 | 3.32 | 2.88 | 2.86 |
| 5 | 2.72 | 2.65 | 2.4 |
| 6 | 3.68 | 3.01 | 2.36 |
| 7 | 2.51 | 1.98 | 2.04 |

5 T-taps would reject two lanes
7 T-taps would pass all lanes

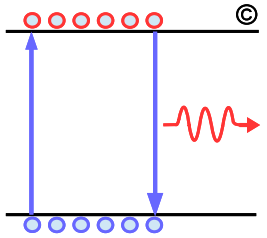



**Used digital PAM4 chip on CFP8 PCB**

All lanes pass with sufficient margin

NeoPhotonics

# What Initiated Threshold Adjust



- **BER contour eye from [mazzini_120617_3cd_adhoc-v2] showed not only vertical offsets but also some having tilts**
  - Mazzini opinion was that real receiver will have threshold adjust
- **For DMLs specially VCSELs additional slicing error gets introduced due to asymmetrical DML waveform which is used to set the slicing levels**
  - A real receiver will use MMSE with additional threshold adjust.

## PAM4 signals: average versus optimum thresholds (1).

Into TDECQ method (802.3bs, 121.8.5.3), sub-eye threshold levels Pth1, Pth2, and Pth3, are determined from the $OMA_{outer}$ and so are average thresholds for each of the three PAM4 eyes diagram (Pave) as defined in Equation (121–1), Equation (121–2), and Equation (121–3).

But in real implementations the optimum thresholds at lower BER are different from the average ones.

This is true even for a very clean eye, with lot of available bandwidth.

$$P_{th1} = P_{ave} - \frac{OMA_{outer}}{3} \quad (121\text{–}1)$$

$$P_{th2} = P_{ave} \quad (121\text{–}2)$$

$$P_{th3} = P_{ave} + \frac{OMA_{outer}}{3} \quad (121\text{–}3)$$

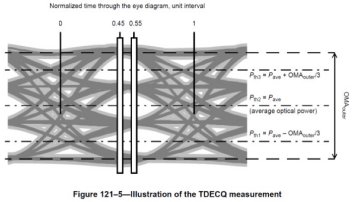
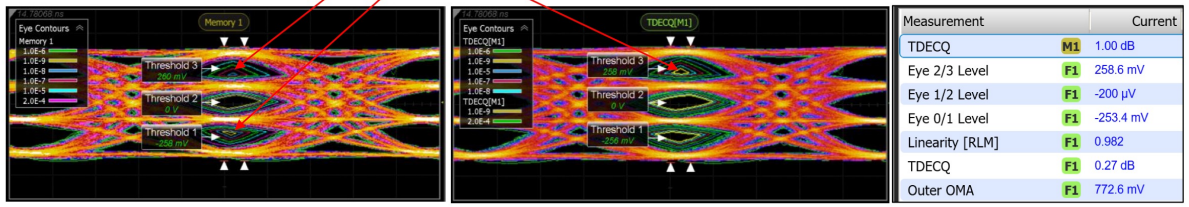


Figure 121–5—Illustration of the TDECQ measurement

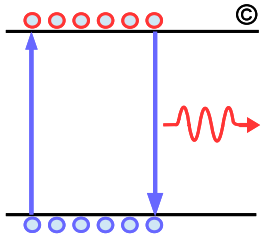
0/1 & 2/3 optimum thresholds are closer to levels 1 and 2 respectively




Above example: clean electrical eye, 773mV VMAouter, @53GBaud, lab-grade equipment, observed BW = 60GHz.

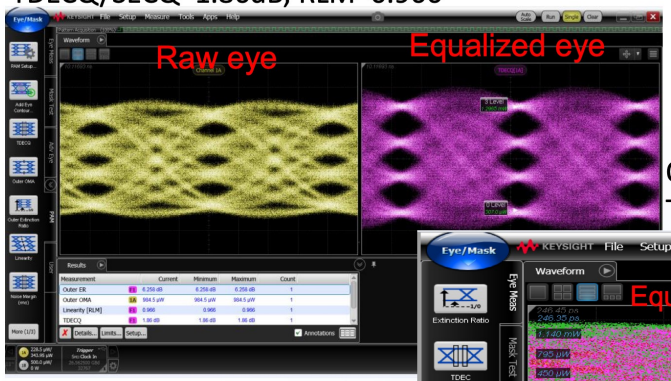
Real receivers will implement threshold optimization to get the lowest BER.

# Proposal to Add Threshold Adjust

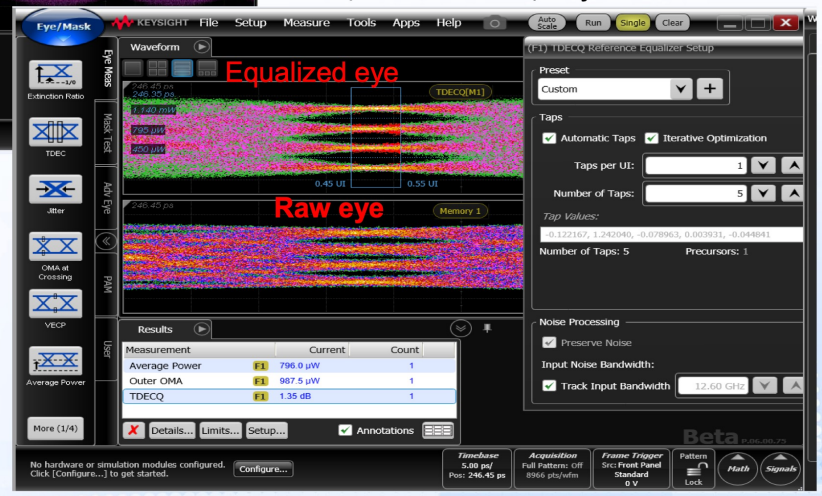


- **Original contribution from [chang_3cd_01b_0318] recommended 2% adjustment given the DML data, but 802.3cd task force only adopted 1% OMA adjustment.**

Off-optimized case (D3.1) ER=6.2dB
TDECQ/SECQ=1.86dB, RLM=0.966




Off-optimized case D3.1 with threshold Adj
TDECQ/SECQ=1.35dB, Adj~1.% of OMAouter




| | | Adj | % |
|---|---|---|---|
| Pth3 | 1130.167 | -9.83333 | -0.99% |
| Pavg | 796 | -1 | -0.13% |
| Pth1 | 466.8333 | -6.83333 | -0.69% |

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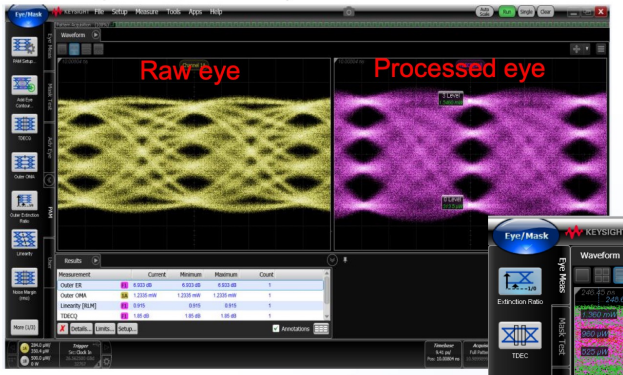
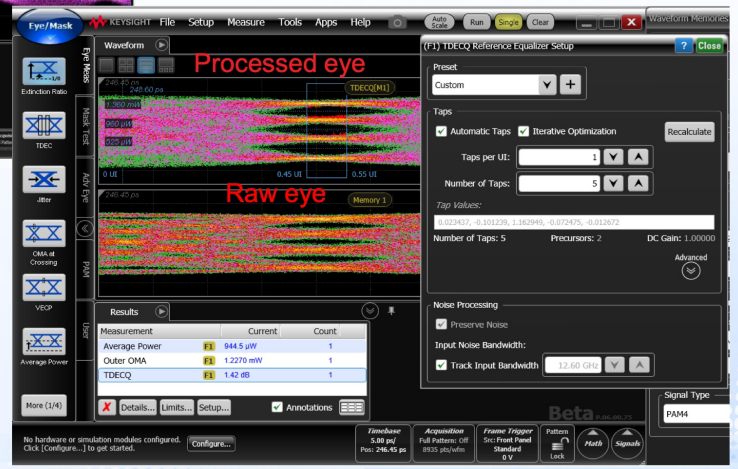
Unoptimized Case1: ER=6.9dB
TDECQ/SECQ=1.85dB, RLM =0.915




Case1(D3.1 with threshold Adj)
TDECQ/SECQ=1.42dB Adj within +1.95%




| | | Adj | % |
|---|---|---|---|
| Pth3 | 1353.5 | 6.5 | 0.53% |
| Pavg | 944.5 | 15.5 | 1.95% |
| Pth1 | 535.5 | -10.5 | -0.86% |

Inphi

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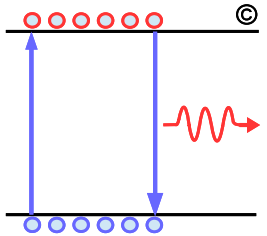
# Summary



- **Existing 100G DSP PHYs in 7 nm are achieving power numbers better than our estimate of 459 mW from 2018 projection**
  - The gap between advance CMOS 5-7 taps analog FFE vs 10+ taps FFE+ receiver that typically achieve 1-2 dB better sensitivity as shown by Way is ~100 mW in 7 nm
  - This gap will further close with 5 nm CMOS to the point where there is little or no power advantage
- **To achieve power in the 300's mW the CDR require costly 5 nm CMOS for DSP and analog implementations**
  - Given the receiver sensitivity challenges with MMF a DSP CDR the offer 1-2 dB sensitivity advantage is a major advantage
  - The DSP CDR with 9T FFE will provide relief to the VR transmitters and likely to be more beneficial than Way's SMF results
- **Given the power dissipation gap is closing between DSP and analog receiver the 802.3db task force should standardize a common 9 taps FFE for both SR and VR PMDs**
  - The 9 tap FFE allow reduced VCSEL BW with improve sensitivity with better economy of scale that will offer better cost advantage than reducing FFE taps to 5
- **Given that VCSELs will have more waveform asymmetry recommend 2% threshold adjust**
  - Original chang_3cd_01b_0318 also recommended 2% threshold adjust but it was viewed adding threshold adjust and 2% might be too big a change during 802.3cd D3.1 recirculation!