

# End to End COM Estimates for 100G Linear Interface with 30 Meters of OM3

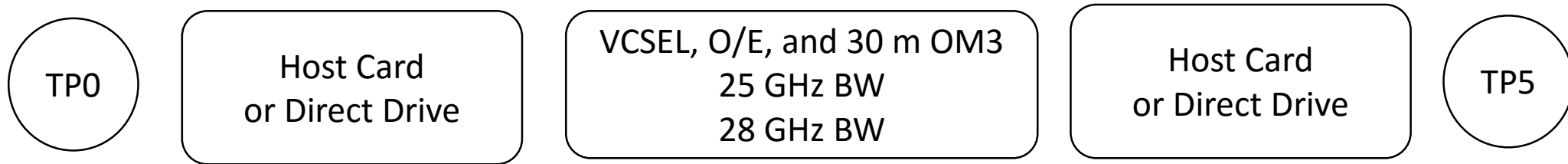
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# Follow up to “In Support of Linear Interface: Updated Measurements / Simulations”

- ❑ Ryan Latchman, Macom
- ❑ [http://www.ieee802.org/3/db/public/adhoc/presentations/latchman\\_3db\\_adhoc\\_01\\_101520.pdf](http://www.ieee802.org/3/db/public/adhoc/presentations/latchman_3db_adhoc_01_101520.pdf)
- ❑ Illustrate how much working margin that .3ck 100G KR devices could have using a COM end to end analysis.

# COM End to End Topology



## ❑ Electricals channels

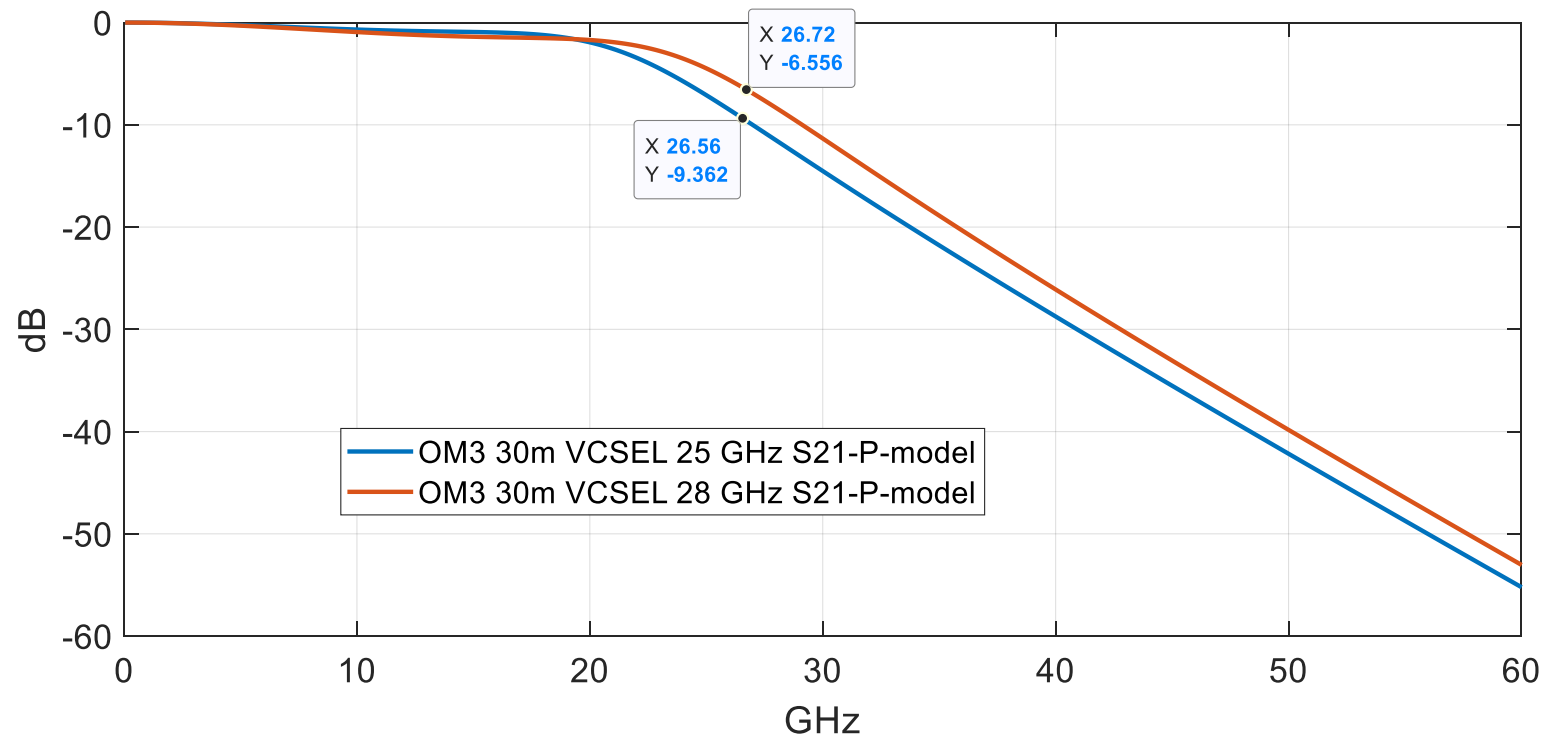
- 3 short channels from Jane Lim (2", 3" and 4")
- 400 mm cabled host
- 85 mm direct drive die to die

## ❑ Optics

- 30 m OM3
- 25 GHz and 28 GHz VCSEL bandwidths

# VCSEL 25 GHz and 28 GHz Contribution

- ❑ Contribution from Jose Castro, Panduit
- ❑ VCSEL, O/E, and 30 meter of OM3 converted to S-parameters



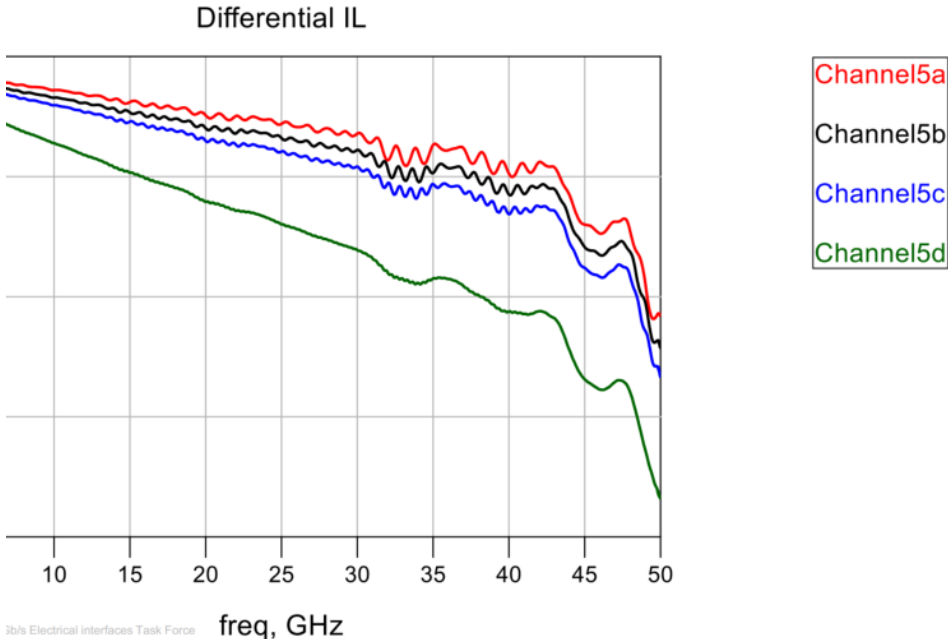
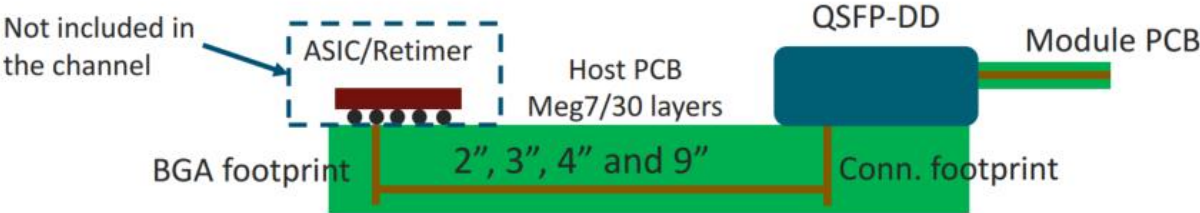
# Electrical Channels: Short Host Channels

□ [http://www.ieee802.org/3/ck/public/adhoc/aug14\\_19/lim\\_3ck\\_adhoc\\_01\\_073119.pdf](http://www.ieee802.org/3/ck/public/adhoc/aug14_19/lim_3ck_adhoc_01_073119.pdf)

## Differential Insertion Loss

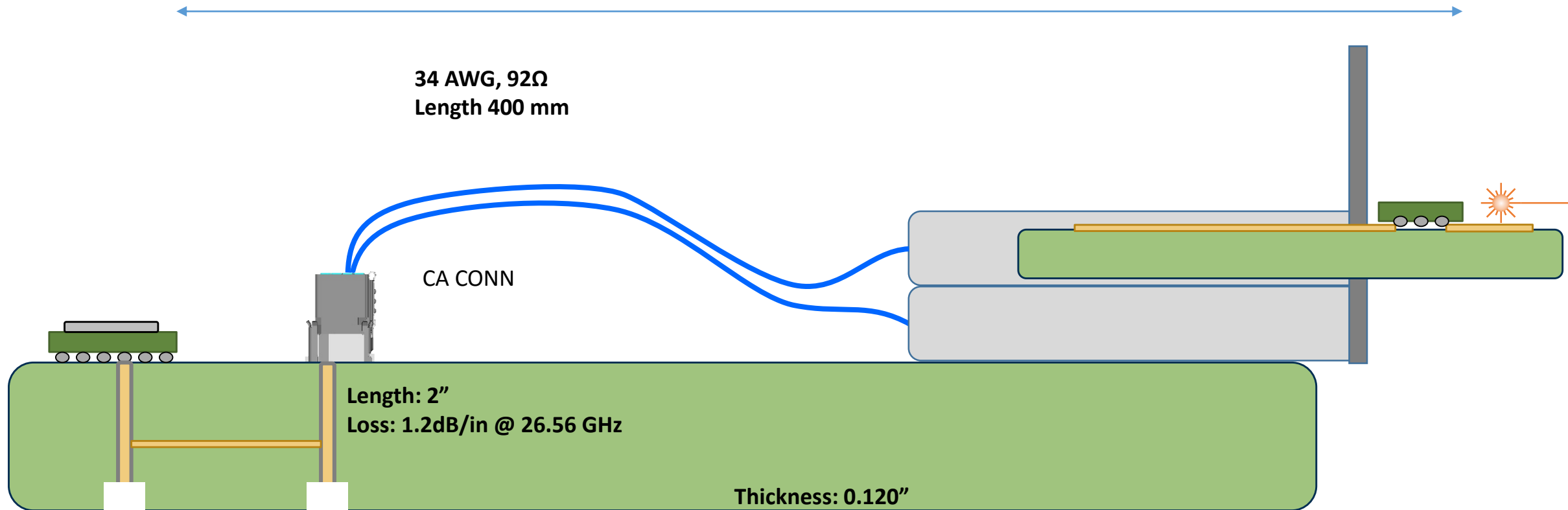
### Model Overview

- 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector and host PCB footprint are solved as one piece in HFSS
- QSFP-DD is the latest updated 112G simulation model
- PCB stackup is 30 layers, 150mil thick, with Meg7 material
- PCB via stub length is modelled as 10mil
- Diff pair trace width/spacing is 4.5mil/8.5mil
- ASIC and retimer footprint are simulated with actual BGA ball-out using the same PCB stackup

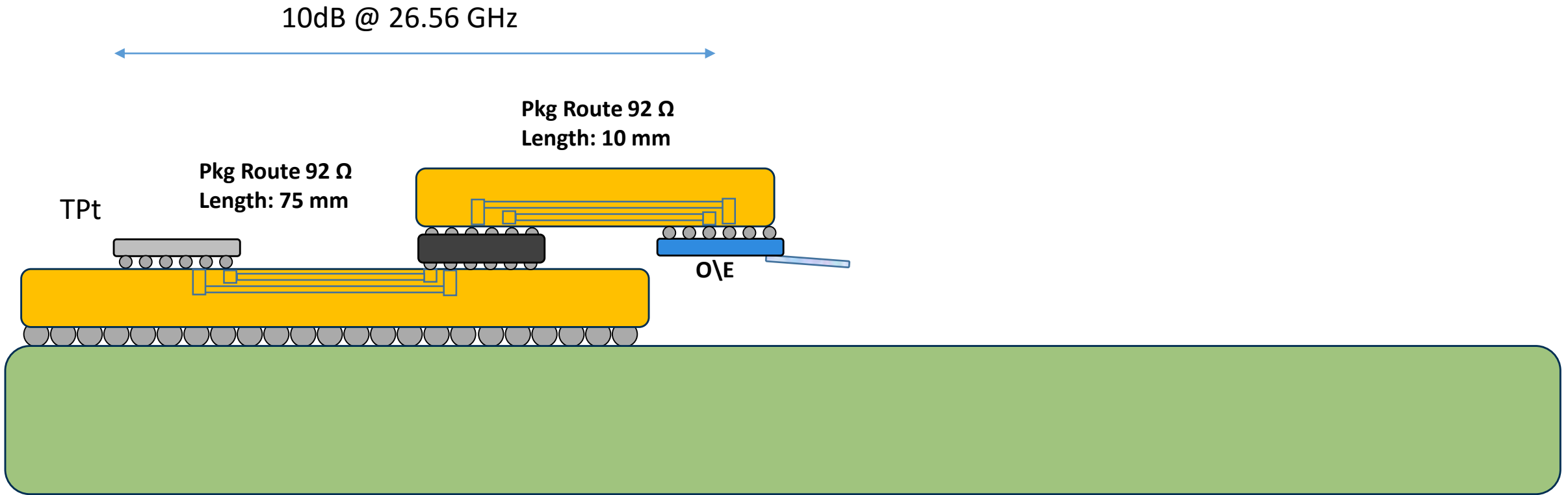


# FQSFPDD NVAC--DD800Host 400mm Electrical Channel

10dB @ 26.56 GHz

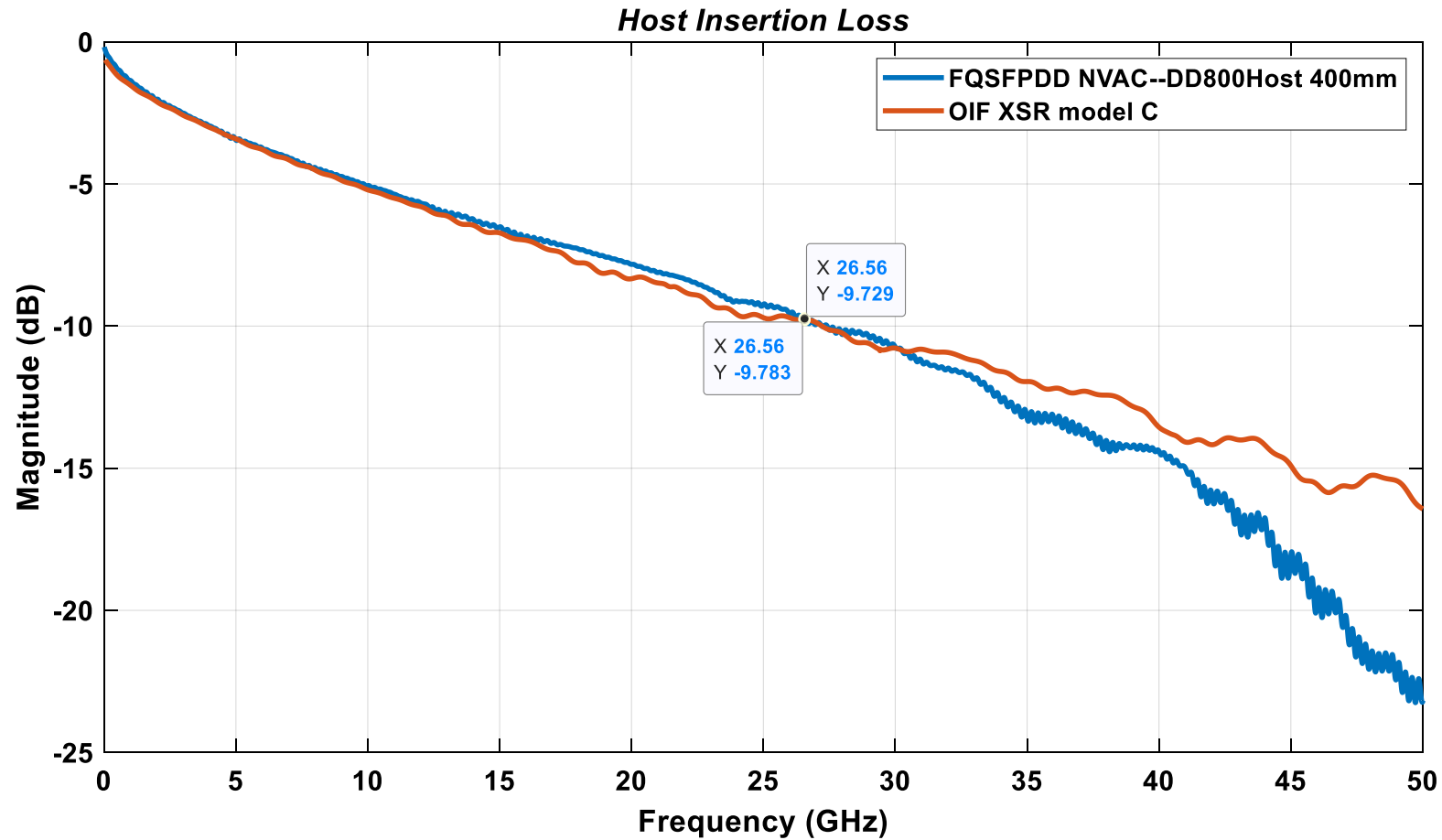


# OIF XSR Model C Electrical Channel



OIF (XSR die to die use model C)

# FQSPDD 800 and XSR Insertion Loss





# COM Computation Example

- ❑ COM KR table for P802.3ck D1.3
- ❑ COM version 2.95
- ❑ No crosstalk
- ❑ TP0 to TP5 used
  - Synthesized optic and electrical
- ❑ 3 dB is normally required for COM
- ❑ Consider
  - This is a first feasibility step in COM modeling
  - Additional feasibility results has been shared in earlier P802.3dB presentations
  - Figure that 4 dB COM would be required to account for extra noise and crosstalk

# COM Results

Channel	Host type	COM (dB) 25 GHz VCSEL	COM (dB) 28 GHz VCSEL	HOST IL (dB) @ 25.56 GHz
Lim--Channel5_thru_small_pad_2inch_w_OM3_Length_30m	Front Panel	4.1	4.7	5.7
Lim--Channel5_thru_small_pad_3inch_w_OM3_Length_30m	Front Panel	4.5	4.9	6.9
Lim--Channel5_thru_small_pad_4inch_w_OM3_Length_30m	Front Panel	4.3	4.9	8.2
FQSFPDD_NVAC--DD800Host_400mm_OM3_Length_30m	Front Panel	5.2	5.5	9.8
XSR_Model_C_OM3_Length_30m	XSR - OIF	6.2	6.5	9.8

□ Plenty of margin for crosstalk and additional noise

# Summary

- ❑ End to end channels with 30 meter of OM3 fiber pass COM with wide margin
- ❑ There may be more details to consider:
  - Additional noise, linearity, etc.
  - Including these factors not expected to delay SR standardization
- ❑ COM margin suggests we are within striking distance
  - Good enough for an objective

# Thank You!

# BACKUP

# COM table for 0.3ck D1.3 (COM 2.95)

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information				Parameter	Setting	Units
f_b	53.125	GBd		DIAGNOSTICS	1	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz		DISPLAY_WINDOW	1	logical	package_tl_tau	0.006141	ns/mm
Delta_f	0.01	GHz		CSV_REPORT	1	logical	package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	Ohm
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]	RESULT_DIR	.\results\100GEL_KR_{date}\				
L_s	[0.12, 0.12]	nH	[TX RX]	SAVE_FIGURES	0	logical			
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	Port Order	[1 3 2 4]				
z_p select	[1 2]		[test cases to run]	RUNTAG	KR_eval_				
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]	COM_CONTRIBUTION	0	logical			
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]	Operational					
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB	board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	8	dB	board_tl_tau	5.790E-03	ns/mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	DER_0	0.0001		board_Z_c	100	Ohm
R_0	50	Ohm		T_r	0.0075	ns	z_bp (TX)	110.3	mm
R_d	[50 50]	Ohm	[TX RX]	FORCE_TR	1	logical	z_bp (NEXT)	110.3	mm
A_v	0.413	V		Local Search	2		z_bp (FEXT)	110.3	mm
A_fe	0.413	V		BREAD_CRUMBS	1	logical	z_bp (RX)	110.3	mm
A_ne	0.608	V		SAVE_CONFIG2MAT	1	logical	C_0	[0.29e-4]	nF
L	4			TDR and ERL options			C_1	[0.19e-4]	nF
M	32			TDR	1	logical	Include PCB	0	logical
filter and Eq				ERL	1	logical	Floating Tap Control		
f_r	0.75	*fb		ERL_ONLY	0	logical	N_bg	3	0 1 2 or 3 groups
c(0)	0.54		min	TR_TDR	0.01	ns	N_bf	3	taps per group
c(-1)	[-0.34:0.02:0]		[min:step:max]	N	3500		N_f	40	UI span for floating taps
c(-2)	[0:0.02:0.12]		[min:step:max]	beta_x	0		bmaxg	0.05	max DFE value for floating taps
c(-3)	[-0.06:0.02: 0]		[min:step:max]	rho_x	0.618		B_float_RSS_MAX	0.02	rss tail tap limit
c(1)	[-0.2:0.05:0]		[min:step:max]	fixture delay time	[0 0]	[port1 port2]	N_tail_start	25	(UI) start of tail taps limit
N_b	12	UI		TDR_W_TXPKG	0		ICN parameters		
b_max(1)	0.85			N_bx	21	UI	f_v	0.594	*Fb
b_max(2..N_b)	[0.3 0.2*ones(1,10)]			Tukey_Window	1	logical	f_f	0.594	*Fb
b_min(1)	0.3			Noise, jitter			f_n	0.594	*Fb
b_min(2..N_b)	[0.05 -0.03*ones(1,10)]			sigma_RJ	0.01	UI	f_2	40.000	GHz
g_DC	[-20:1:0]	dB	[min:step:max]	A_DD	0.02	UI	A_ft	0.600	V
f_z	21.25	GHz		eta_0	8.20E-09	V^2/GHz	A_nt	0.600	V
f_p1	21.25	GHz		SNR_TX	33	dB			
f_p2	53.125	GHz		R_LM	0.95				
g_DC_HP	[-6:1:0]		[min:step:max]				Receiver testing		
f_HP_PZ	0.6640625	GHz					RX_CALIBRATION	0	logical
							Sigma BBN step	5.00E-03	V