In Support of Low Cost/Power 100G SR: Linear Architecture Review

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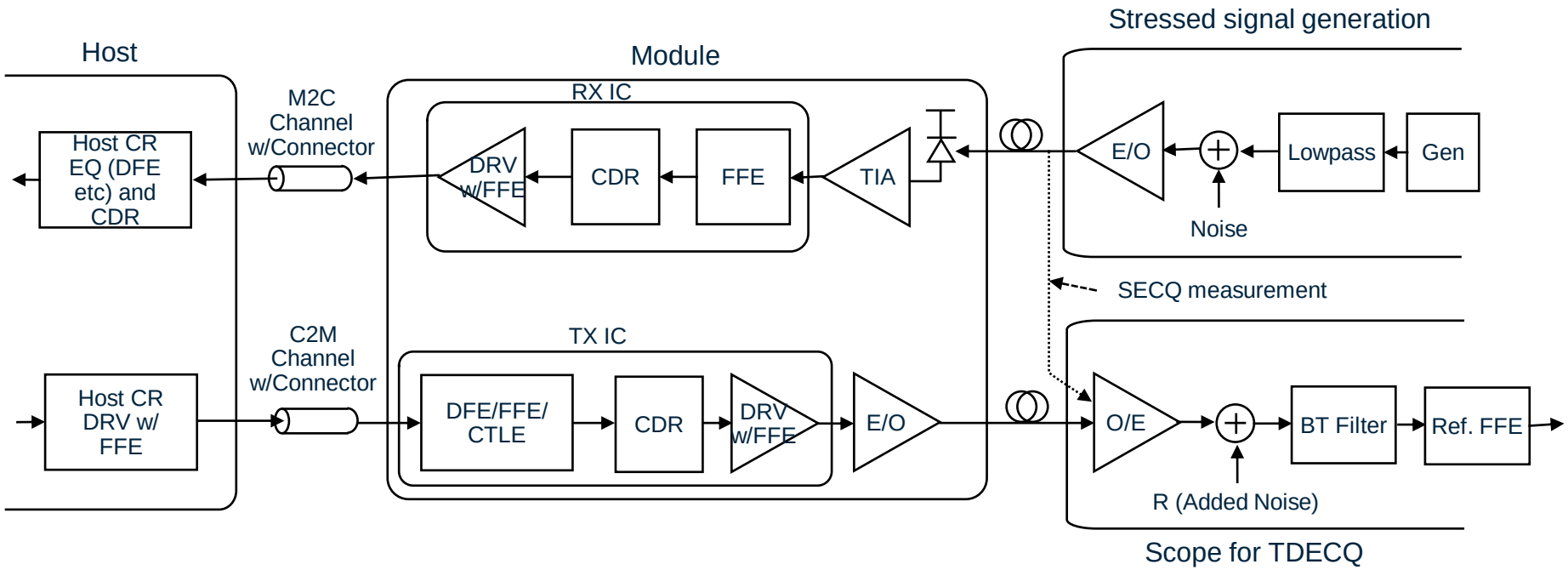
Supporters

- Vipul Bhatt (II-VI)
- Jose Castro (Panduit Corp)
- Greg D Le Cheminant (Keysight)
- Richard Mellitz (Samtec)
- Tom Palkert (Samtec)
- Rob Stone (Facebook)
- Prasad Venugopal (Arista)
- Chongjin Xie (Alibaba)

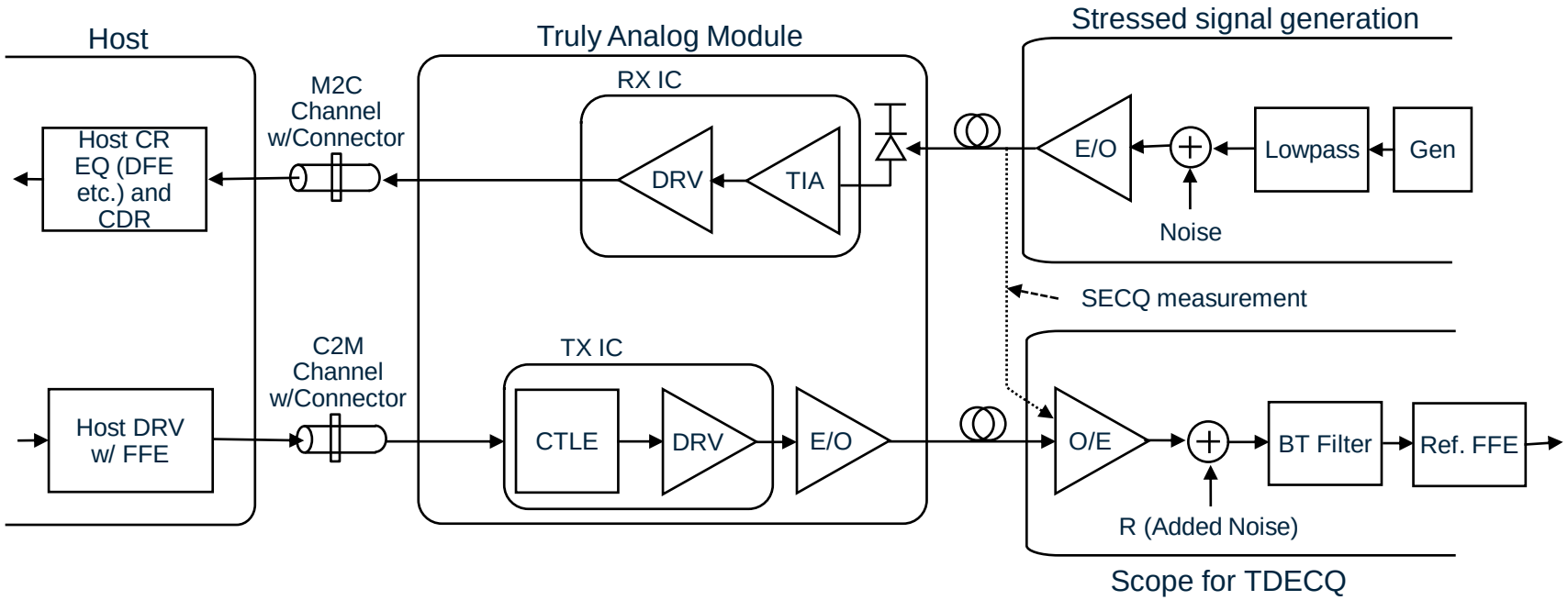
Traditional Approach With Retiming / DSP



Host ASICs have very capable equalizers to compensate for copper interfaces (CR/KR etc)

Non-linear retimed interface (DSP/CDR) limit the ability to leverage this equalization capability to Chip-Module interface (making the host I/O highly underutilized)

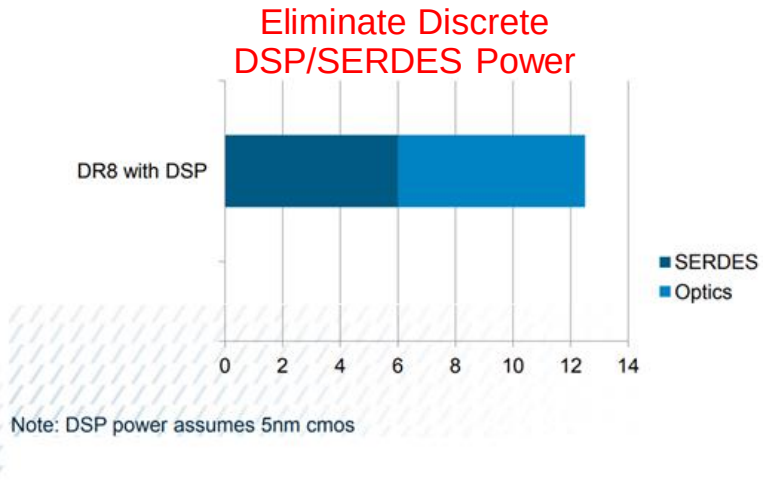
New Architecture: Linear and Non-Retimed



Architecting Module with a linear interface (No DSP/CDR) allows for host equalizer leverage and dramatically reduces power and cost. TDECQ FFE can also be used for recovering residual impairments from the combined host / E to O channel

Benefits to Linear Architecture

- Per Port Power consumption dramatically lower without DSP
  - 6W-8W savings on 800G port
- Cost dramatically lower without DSP or CDR
- Leverage system (ASIC) capability to the fullest
  - Potentially makes end-end link negotiation possible
- Brings module budgeting in line with historical trends
  - QSFP28 / SFP28 SERDES power content: 0W
  - Signal Integrity <10% of module power consumption
- Protocol, data rate, FEC scheme independent PMD interface
  - Methodology scalable to next generation bit rates
- Faster link bring up

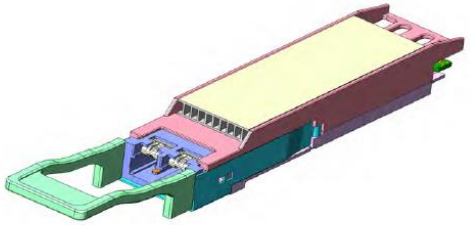


Reference: palkert_3ck_03a_1119.pdf

Quantifying Power Consumption at 100G/lane

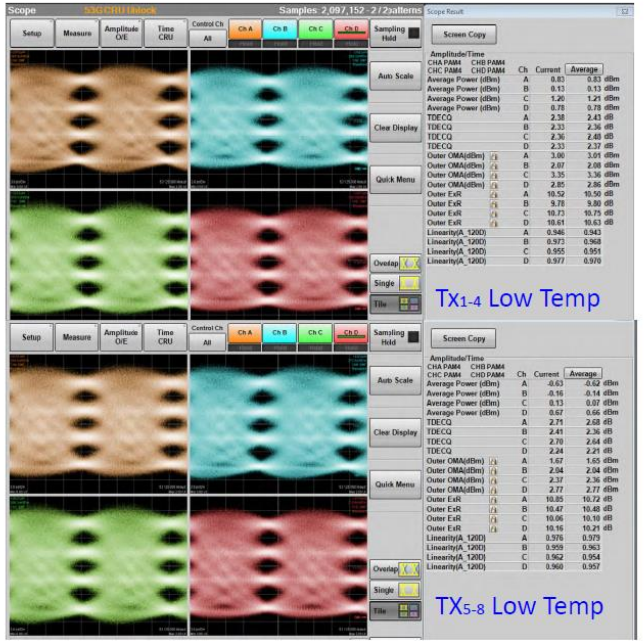
- 8 x 100G/lane SMF module with DSP inside: **17W-18W**
- 8 x 25G/lane (e.g. two QSFP28) SMF Module: **7W max**
  - QSFP28: Low power, low cost
  - 40G QSFP (4x10G): similar power consumption to QSFP28

Example: 800 Gb/s OSFP Capacity Module



- OSFP Form Factor
- 8x100G DR8+ 2km with MPO-16 and 2x400G FR4 with CS connector
- OIF CEI-112G-VSR interface
- PMD spec follows 400G DR4+ and FR4. interoperable with 400G
- 0~70degC 18W, 10~60C 17W
- 7nm DSP inside

Source – Tedros Tsegaye, Innolight



24 Aug 2020 IEEE 802.3 NEA Ad hoc - Draft Development - 400 GbE CFI Consensus Presentation Page 35

Reference: dambrosia_nea_01b_200824.pdf

50G Feasibility Demonstration: Innovium Switch Electrical Loopback Performance

- Electrical interface has potential to have minimal contribution to BER
  - ASIC capable of passive copper operation ensure margin relative to C2M

```
+-------------------------------------------------------------------------+
| Devport : Lane :   ISG :     Rate : Polynomial : Err Diff :      BER |
|-------------------------------------------------------------------------|
|    15 :    0 : ISG17 : 53_125GBS :    PRBS31 :     324 : 1.956e-9 |
|    15 :    1 : ISG17 : 53_125GBS :    PRBS31 :  Unknown :      N/A |
|    15 :    2 : ISG17 : 53_125GBS :    PRBS31 :  Unknown :      N/A |
|    15 :    3 : ISG17 : 53_125GBS :    PRBS31 :  Unknown :      N/A |
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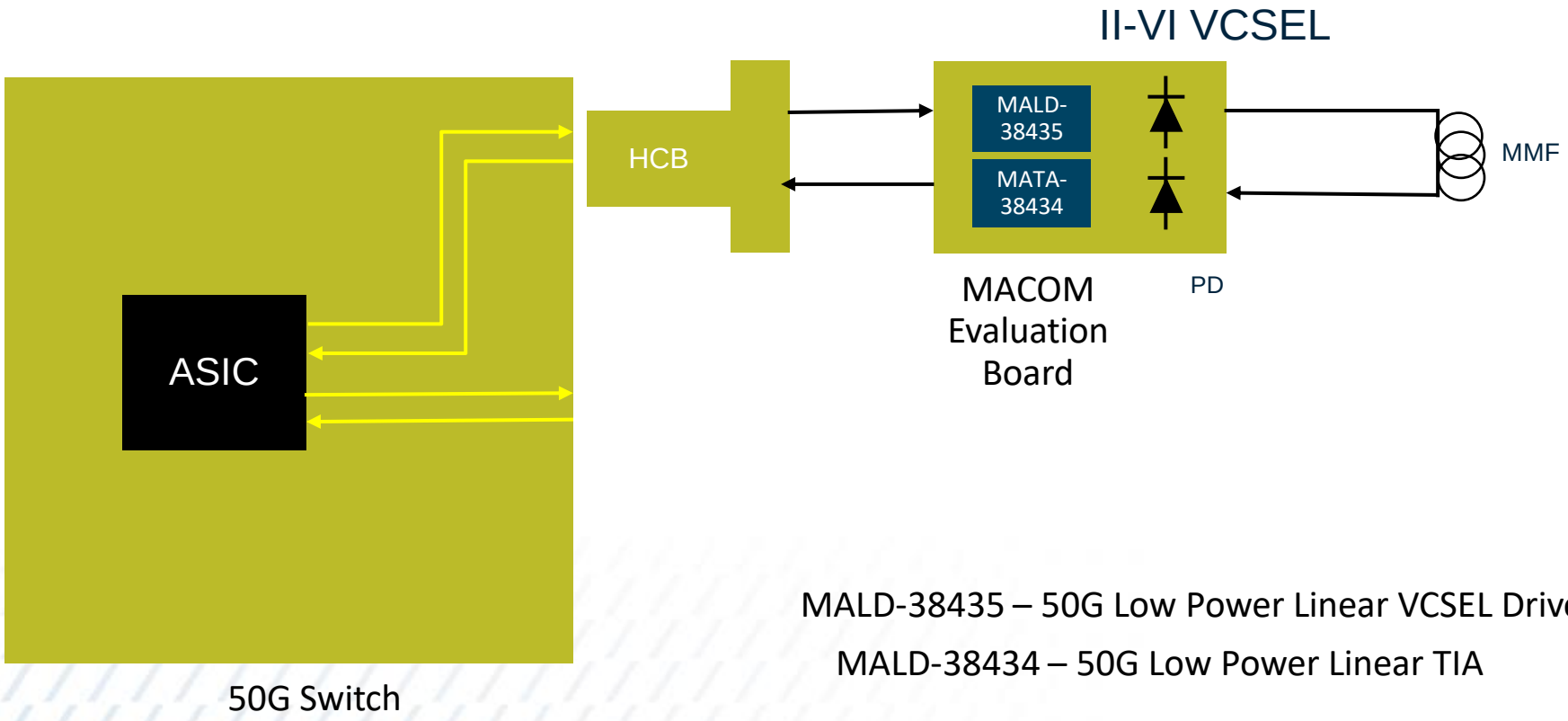
Electrical Loopback

Optical Linear Interface Demonstration



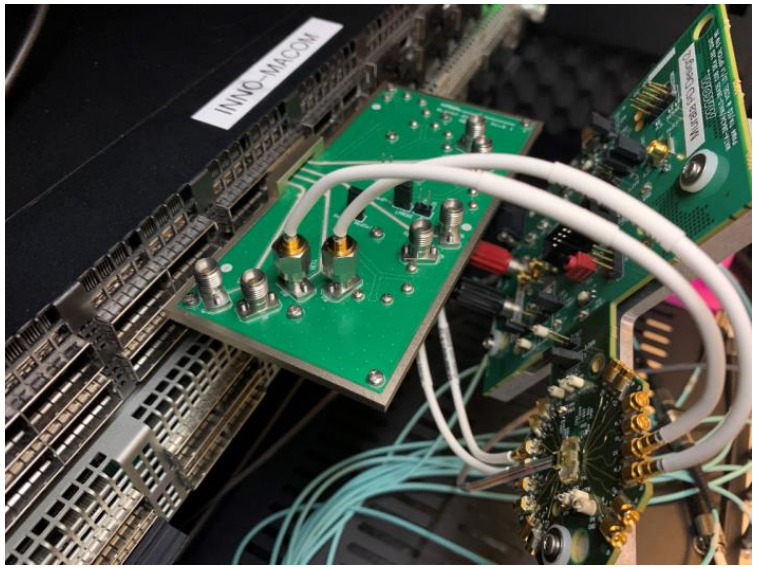
MALD-38435 – 50G Low Power Linear VCSEL Driver

MALD-38434 – 50G Low Power Linear TIA

Feasibility Demonstration: Linear Interface w/ Optical EVB (Port 15 – Closest to ASIC)

- Innovium switch -> HCB -> Optical EVB TX with linear VCSEL driver (MALD-38435)-> MMF Loopback -> Optical RX with linear TIA (MALD-38434) -> HCB-> Switch

- VCSEL Driver and TIA can be further optimized to directly interface with host

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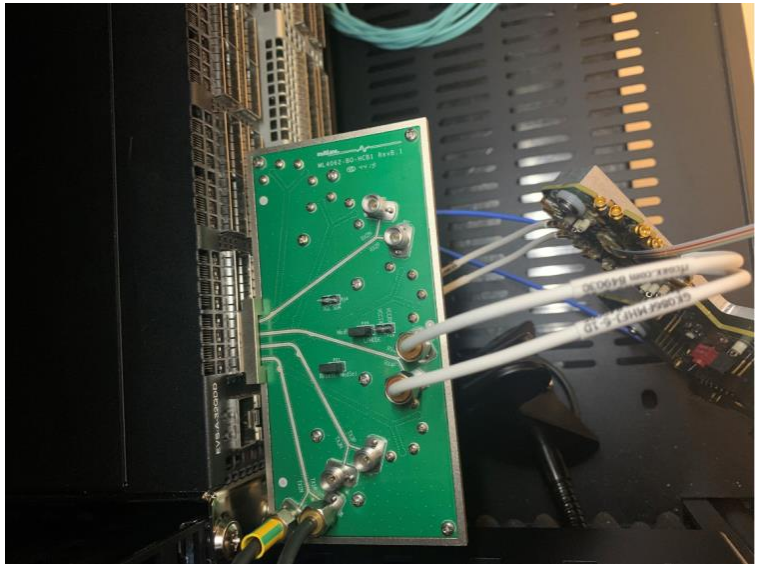
+-------------------------------------------------------------------------+
| Devport : Lane :   ISG :     Rate : Polynomial : Err Diff :      BER |
|-------------------------------------------------------------------------|
|    15 :    0 : ISG17 : 53_125GBS :    PRBS31 :     324 : 1.956e-9    |
|    15 :    1 : ISG17 : 53_125GBS :    PRBS31 :  Unknown :      N/A |
|    15 :    2 : ISG17 : 53_125GBS :    PRBS31 :  Unknown :      N/A |
|    15 :    3 : ISG17 : 53_125GBS :    PRBS31 :  378882 : 2.287e-6  |
+-------------------------------------------------------------------------+
```

Electrical Loopback

Optical Link

Feasibility Demonstration: Linear Interface w/ Optical EVB (Port 1 – Farthest from ASIC)

- This includes some pre-emphasis adjustment in the ASIC
  - tx_eq_pre1 [-2,-2,-2,-2]
  - tx_eq_pre2 [-2,-2,-2,-2]
  - tx_eq_pre3 [0,0,0,0]
  - tx_eq_attn [0,0,0,0]
  - tx_eq_post [0,0,0,0]
- VCSEL Driver and TIA can be further optimized to directly interface with host



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+-------------------------------------------------------------------+
| Devport : Lane :  ISG :     Rate : Polynomial : Err Diff :     BER |
|-------------------------------------------------------------------|
|     1 :   0 : ISG31 : 53_125GBS :    PRBS31 :    1450 :   8.797e-09 |
|     1 :   1 : ISG31 : 53_125GBS :    PRBS31 :  Unknown :       N/A |
|     1 :   2 : ISG31 : 53_125GBS :    PRBS31 :  Unknown :       N/A |
|     1 :   3 : ISG31 : 53_125GBS :    PRBS31 :   311501 : 1.898e-06 |
```

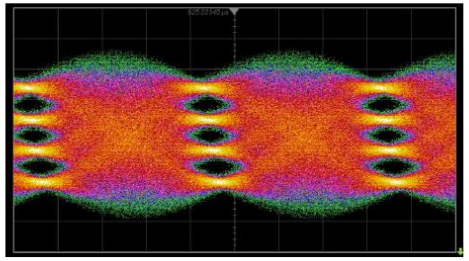
Electrical Loopback

Optical Link

100G Linear Interface Tx Considerations

- Reference receiver assumptions can be stronger without adding power / cost to module with linear interface
  - Leverage stronger equalizer on hosts
  - 9+ FFE taps, potential to introduce DFE Taps to maximize reach
- Leverage 30m reach to make additional budget available for host and optics
  - 2m vs 30m TDECQ penalty small
    - 30m vs 100m difference greater than 1dB
- 9-tap needed to support 100m
    - Host equalizers integrated in ASICs can be quite capable beyond 9-tap

Eye diagram after 100 m OM4



TDECQ: 3.5 dB

Modulation format	PAM4
Symbol rate	53.125 GBd
Pattern	PRBS15Q
Tx FFE	3-tap T-spaced
SER target for TDECQ	4.8×10^{-4}
DCA optical plug-in bandwidth	34 GHz
DCA SIRC bandwidth	38.3 GHz
DCA BT filter bandwidth	26.6 GHz
DCA FFE	9-tap T-spaced
Temperature	75 °C
Center wavelength	863 nm
RMS spectral width	0.42 nm
Outer ER	3 dB

- 100 m OM4 link: TDECQ within 4.5 dB with a 9-tap Rx FFE

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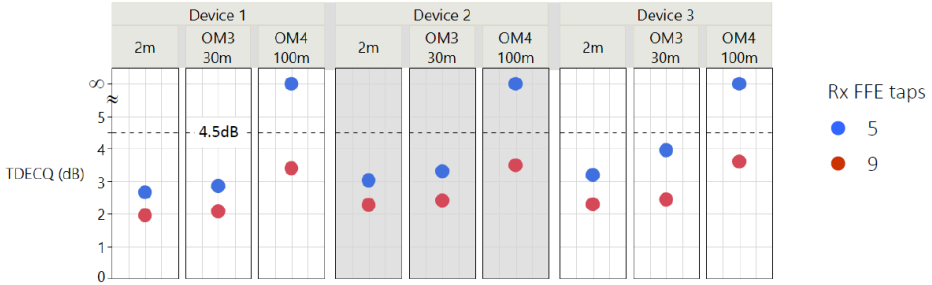
TDECQ vs Rx FFE taps



- 30 m OM3 link: 5-tap Rx FFE is sufficient for TDECQ within 4.5 dB
- 100 m OM4 link: TDECQ within 4.5 dB with a 9-tap Rx FFE, but not measurable with a 5-tap Rx FFE

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Reference: ingham_3db_adhoc_01a_062520

Example Optical Tx Interface Considerations

SR(30) = 30m SR(100) = 100m

Table 140–6—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 transmit characteristics

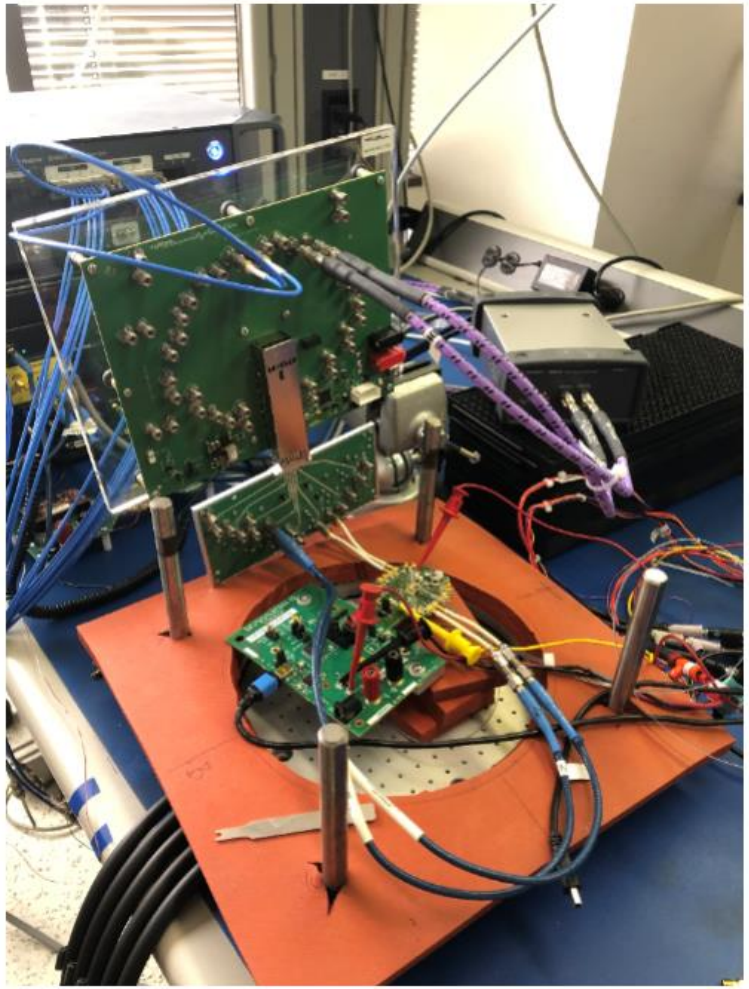
Description	Value (SR(30)) 100GBASE-DR	(SR(100)) 100GBASE-FR1	Unit
Signaling rate (range)	53.125 ± 100 ppm		GBd
Modulation format	PAM4		—
Wavelength (range)	850		nm
RMS Spectral Width (max)	0.6		nm
Average launch power (max)	4	4	dBm
Average launch power[a] (min)	-6.5	-6.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	3	3	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]	X (-4.5)	X (-4.5)	dBm dBm dBm
Launch power in OMA_{outer} minus TDECQ (min):	Y-1 (-5.9)	Y (-4.9)	dBm dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	Z + 1 (4.5dB)	Z (3.5dB)	dB

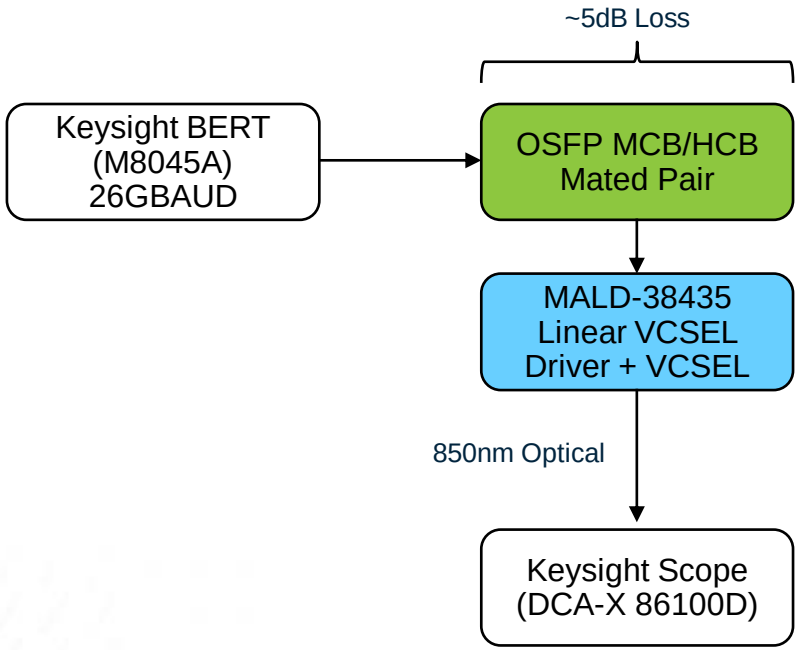
Consider raising min Tx OMA

Shorter Channel allows for relaxed Tx Budget

Shorter Link allows for higher TDECQ assuming no test fiber. Measure with 9-tap + FFE

Linear Tx Interface Demonstration – 26GBAUD VCSEL Result

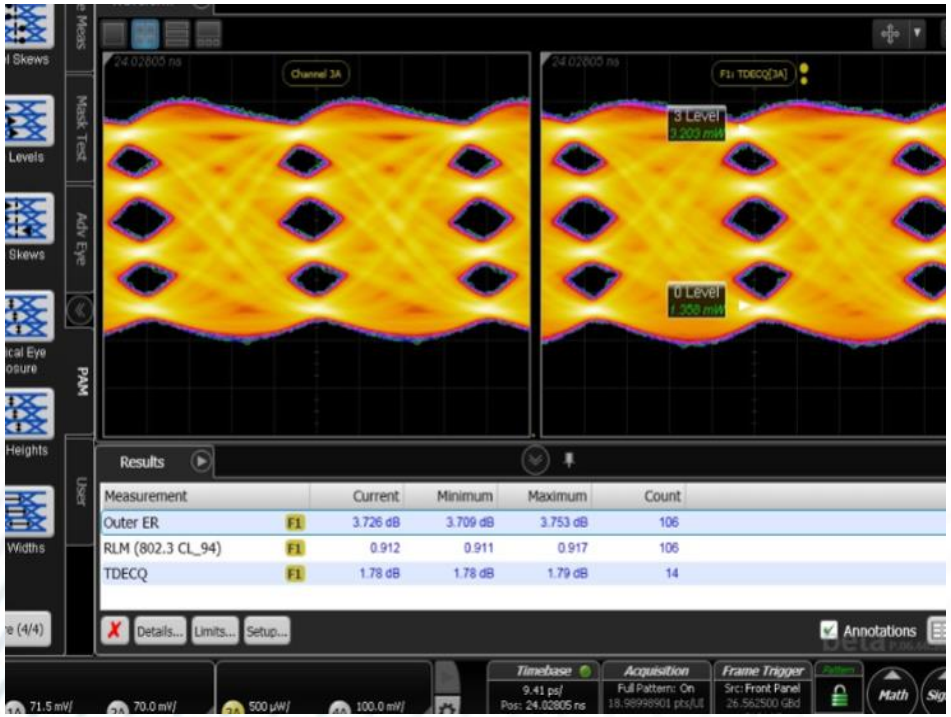




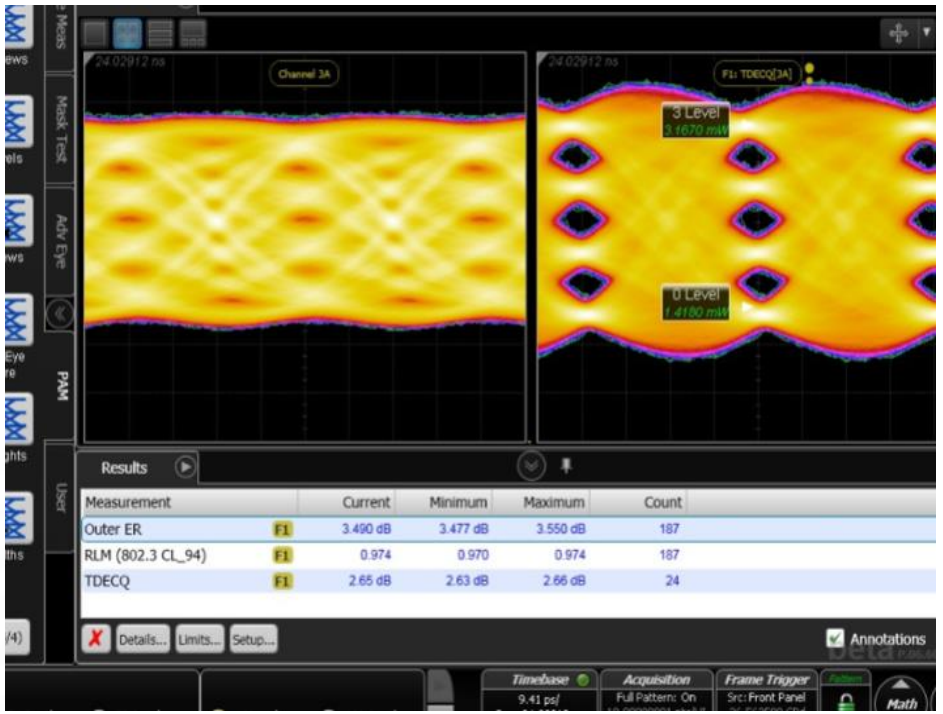
850nm II-VI Laser

Tx Path – Optical Output Comparison

- TDECQ: FFE able to improve optical output from MACOM Optical Evaluation Board
  - TDECQ 1.78dB (without MCB/HCB pair) vs 2.65dB (with MCB/HCB)
  - MALD-38435 can be further optimized to interface directly to hosts

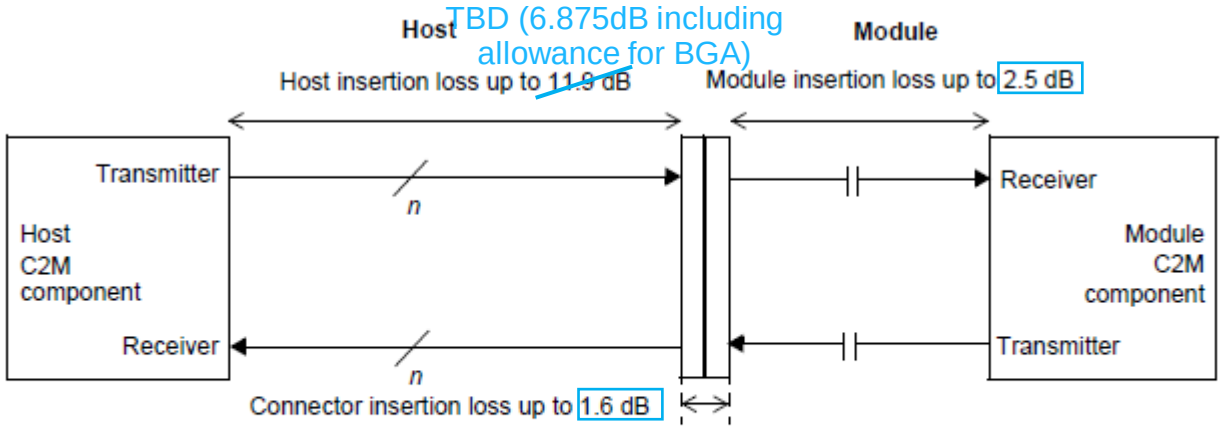


MALD-38435 optical output without MCB+HCB



MALD-38435 optical output with MCB+HCB

Linear Electrical Interface Considerations
Leveraging .ck efforts (C2M & CR)



Note—The number of lanes *n* is equal to 1 for 100GAUI-1, 2 for 200GAUI-2, and 4 for 400GAUI-4.

Figure 120G–2—~~100GAUI-1~~, ~~200GAUI-2~~, and ~~400GAUI-4 C2M~~ insertion loss budget at 26.56 GHz

100GLPI-1 400GLPI-4

200GLPI-2

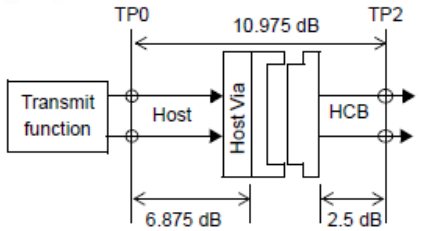
LPI = Linear Physical Interface

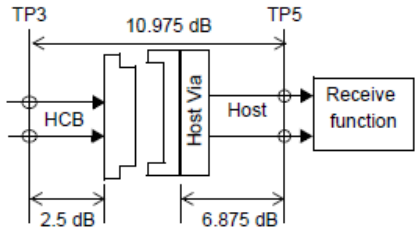
Consider Leveraging ~100GBASE-CR Budget

162.9.3.2 Insertion loss, TP0 to TP2 or TP3 to TP5

The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is given by Equation (162–5). Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.975 dB at 25.56 GHz.

TBD (162–5)





NOTE—The 6.875 dB IL includes allowance for BGA and connector footprint vias.

Linear Electrical Interface Considerations
Host Evaluation

- In Tx, consider partitioning TDECQ budget for Host and Module
- Leverage similar reference receiver for electrical TDECQ
  - CTLE to compensate for some ISI linearly
  - 5-Tap FFE (since this is used in SMF optical evaluation)
    - make electrical interface flexible similar to 10G XLPPI which applied to both SR and LR
- OR, leverage 5-tap FFE reference receiver at TP1a and set appropriate eye opening

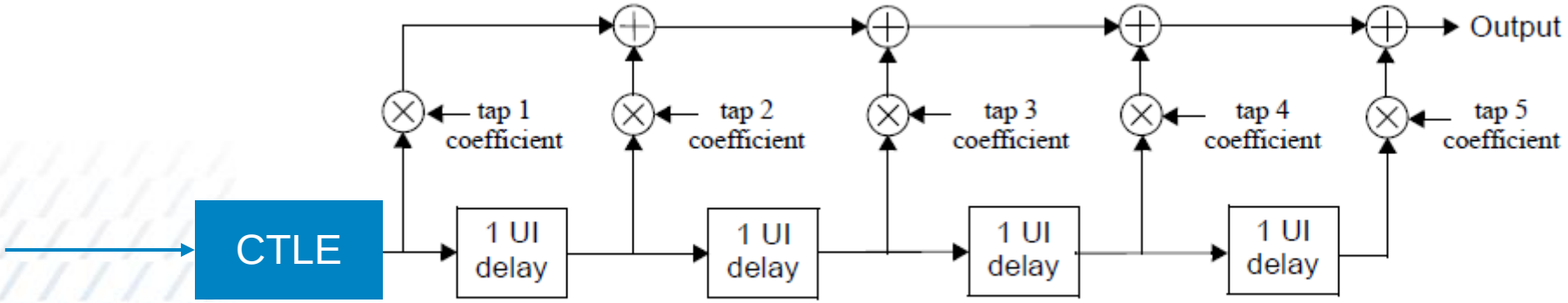


Figure 121–6—TDECQ reference equalizer functional model

Standardization of Linear Interface

- A linear interface can dramatically reduce solution power and cost
  - Demonstrated with measurements at 50G
  - Support at 100G for 30m and 100m
- Thoughts on Evaluating Host:
  - Align host with optical specs - consider Electrical TDECQ / SECQ based on linear Tx/Rx
- Thoughts on Evaluating Modules:
  - Evaluate with appropriate electrical inputs and ensure optical performance is still met
  - Evaluate electrical output from module with Rx FFE/DFE to ensure compliance
- Standardize both optical and electrical interfaces