Requirement for VCSEL based 100G/lane solution in SR scenario

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Ad Hoc Teleconference

Outlines

- VCSEL technical feasibility check-out
- System margin considerations in 100G/lane 100m MMF scenario
- Link budget, TDECQ and error floor
- Considerations on baseline
- Conclusions

VCSEL technical feasibility check-out

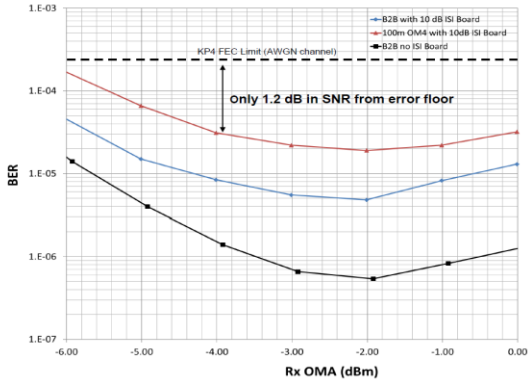
- Compared with 25GB VCSELs, a significant improvement has been made in VCSELs.
- Currently, the VCSEL and DFB would have similar device bandwidth (>25G), which meets the basic requirement for interoperability.
- Due to the multimode fiber impairment, the requirement for VCSEL specs are higher based on same Tx/Rx equalization.

	Parameters	MMF VCSELs	SMF DFB	Note
Tx	BW（GHz）	>25G[a]	>25G[b]	ISI penalty
	RIN without feedback (dB/Hz)	-145[c]	-148[d]	Link budget penalty &Error floor penalty
	Spectral width (nm)	<0.6	Not limited	Link budget penalty & Error floor penalty
	Mode Partition Noise factor	<0.1	0	Link budget penalty & Error floor penalty
Channel	Effective Bandwdith (GHz) @ 100m	24	Not limited	Modal dispersion & Chromatic dispersion penalty

a. murty_3db_01a_1120.pdf
b. 800G Pluggable MSA whitepaper
c. 2020 OFC M3D.5.pdf
d. 2017 OFC Th4G.6.pdf

System margin considerations in 100G/lane 100m MMF scenario

- TDECQ serves as evaluation on Tx for the link budget, the system margin such error floor was not within the scope.
- High error floor may lead to uncorrected symbol error after FEC.
- Safe error floor should be discussed to accommodate some impairment in system such as MPI, device nonlinearity, feedback tolerance, device uniformity.



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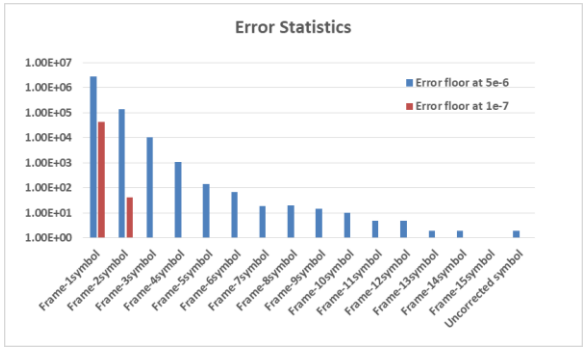
400G FR4 module reliability test

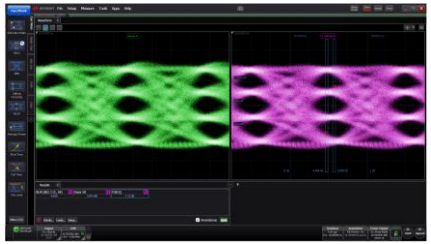


- Error floor larger than 1e-6 happens to fail after KP4 with higher possibility

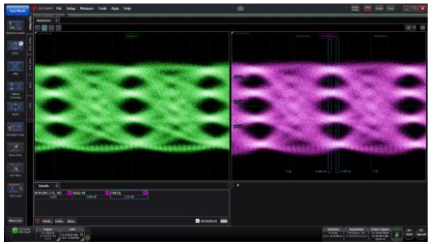
Link budget, TDECQ and error floor

- The experiments on commercial available 400G SR8 modules for 200m OM4 try to implement similar stress to mimic 100G/Lane 100m OM4 scenario
- The TDECQ could well predict the link budget change after fiber, but there is no clear specs to constrain the error floor.
- There are many other contributor to the error floor which may lead to the same TDECQ. In MMF, such contributors are more than that in SMF.

OM4 experiments using 400G SR8 modules with VCSEL from dominant venders

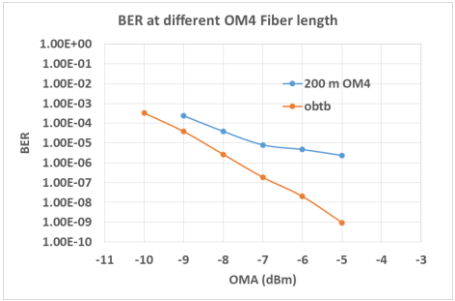


PRBS15
TDECQ=1.1 dB
obtb



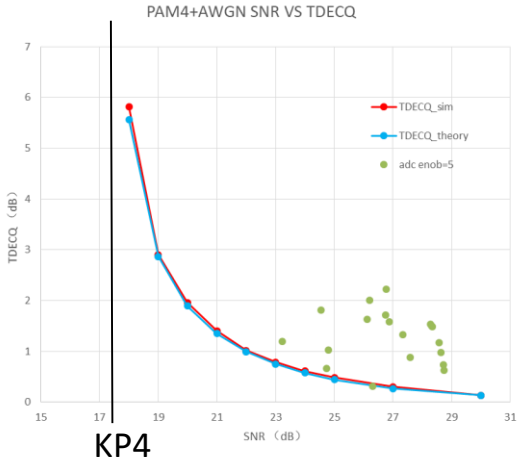
PRBS15
TDECQ=2.5 dB
200m OM4

Equalized by commercial available DSP



TDECQ of 2.5 dB is still far below 4.5 dB specs!

Simulation on TDECQ



KP4

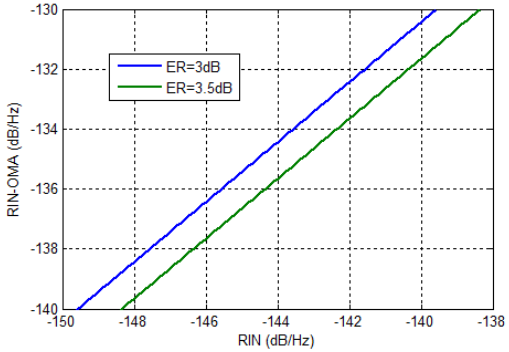
Note: So far the VCSEL test pattern is PRBS15, while SSPRQ test pattern is highly recommended to reflect stress in applications

Considerations on baseline

- Historically, the RIN_OMA for MMF based solutions is always higher than that for SMF based solutions
- For 100G SR, the RIN_OMA is suggested to line up with 100G SMF spec for error floor consideration.
- Lower ER requires more stringent RIN of VCSEL devices.

Parameters	50G FR	100G FR	100G DR	50G SR	100G SR
Rin_OMA (dB/Hz)	-132	-136	-136	-128	TBD
Optical return loss tolerance (max)	17.1	17.1	21.4	12	TBD
Extinction Ratio (dB)	3.5	3.5	3.5	3	TBD

Note: No isolator in VCSEL based solutions requires stringent feedback tolerance



Conclusions

- Due to the MMF channel impairment, VCSELs based solutions requires more stringent specs on devices.
- Based on massive system reliability tests, an error floor 2 order magnitude lower than FEC threshold is suggested for consideration.
- The baseline of RIN_OMA in 100G/lane SR is suggested to line up with other 100G/lane scenario.

Thank you

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