Clause 104 Maintenance Requests #3

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Overview

Item	Updated?
SCCP PSE/PD Watchdog Timer Overlap	No
SCCP C_{IN_CLASS}	Yes
→ SCCP t_{REC}	Yes
→ SCCP t_{RESET} Timing	New
→ SCCP $t_{READSLOT}$ Timing	Yes
→ SCCP $t_{WRITESLOT}$ Timing	Yes
Reduce $T_{F,\ min}$	New

PSE and PD SCCP Timers Overlap

- PSE Table 104-4

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
8	Classification time	T_{Class}	ms	—	366	~~All~~Classes 0 to 9	All	See 104.4.5
					1300	Classes 10 to 15		

- PD Table 104-7

…							
15	SCCP watchdog timeout	$T_{SCCP\_watchdog}$	ms	150	200	~~All~~A, B, C, D	See 104.5.5
				~~1000~~ 1300	~~1300~~ 2000	E	

SCCP Watchdog Timer

…							
15	SCCP watchdog timeout	$T_{SCCP\_watchdog}$	ms	150	200	~~All~~A, B, C, D	See 104.5.5
				~~1000~~ 1300	~~1300~~ 2000	E	

Technical, 802.3cg, Page 93, Table 104-7, Item 15

Comment:

The PSE and PD SCCP timers overlap. If all commands are executed at maximum timings the PD timeout can occur too aggressively.

Suggested Remedy:

Change SCCP, min:max for Class E from 1000ms:1300ms to 1300ms:2000ms.

Need to Address:

Solution Form:

Solution Details:

C_{IN_CLASS}

Need to Address:

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Solution Details:

Technical, 802.3cg, Page 93, Table 104-7, Item 6b

Comment

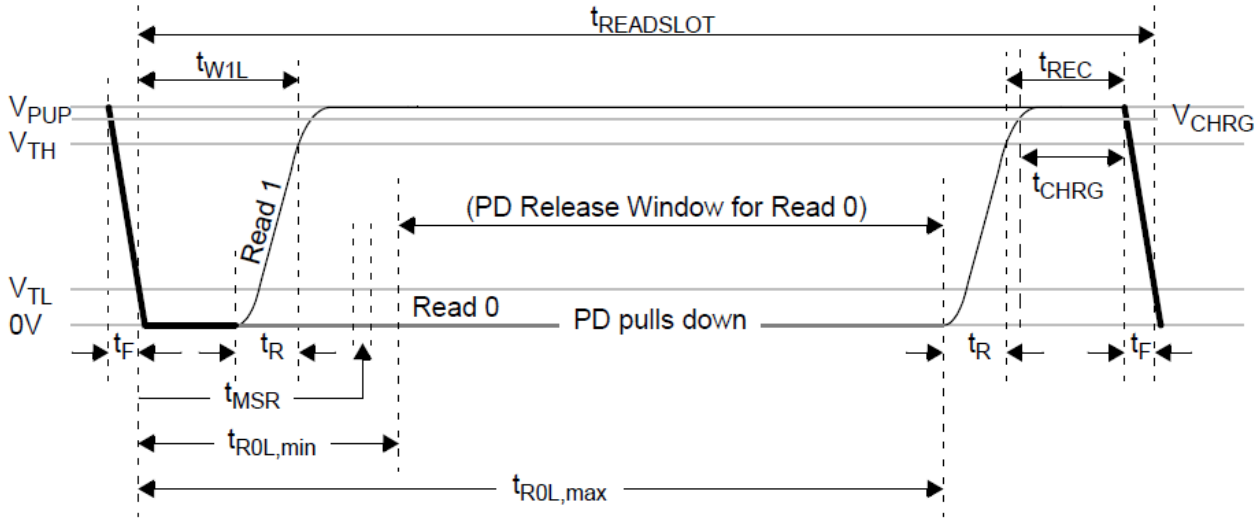
- C_{IN_CLASS} is limited to ensure that excessive rise and fall times do not interfere with SCCP
  - Other timing parameters are affected by C_{IN_CLASS}
  - t_R and t_F were generous and can already accommodate C_{IN_CLASS} of up to 0.8uF
- C_{IN_CLASS}, max is 0.4uF for Type E
- This value is unnecessarily restrictive and potentially infeasible
  - A reservoir cap is required to maintain PD operation during Reset commands

Suggested Remedy

Modify Table 104-7, Item 6b

6b	Input capacitance during DO_CLASSIFICATION state	C_{IN_Class}	µF	—	0.2	~~All~~A, B, C, D	All classes Applies during tR and tF only.
				—	~~0.4~~ 0.8	E	

SCCP t_{REC} Timing



Parameter	Min	Max
t_{REC}	~~0.27~~ 0.5	~~0.33~~
~~t_{CHRG}~~	~~0.2~~	
~~V_{CHRG}~~	~~$0.9 \times V_{PUPmin}$~~	

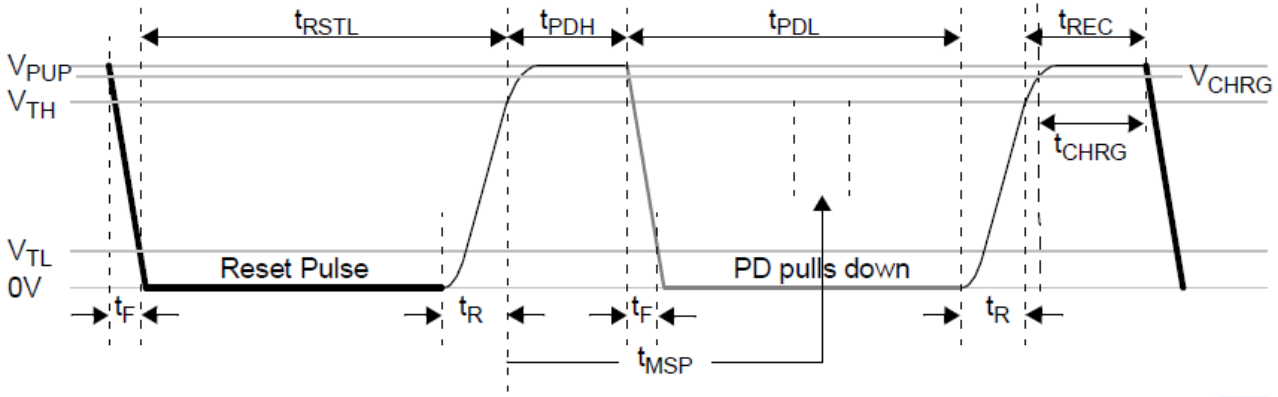
- t_{REC} should be treated like t_{CHRG}
  - t_{REC} max timing is already constrained by $t_{READ/WRITESLOT}$
  - Real world slew rates between V_{TH} and V_{PUP}, rising, cannot be accommodated by existing timing relationships
  - **Propose:** Only a min should be specified, increase min to track C_{IN_CLASS} change
- t_{CHRG} introduces confusion without adding value
  - t_{CHRG} was intended to enable reservoir capacitor recharge but instead interferes by over-constraining charge
  - **Propose:** Remove as redundant to t_{REC}

Need to Address:

Solution Form:

Solution Details:

SCCP Reset Command Timing



Parameter	Min	Max
t_F	0.025	0.25
t_{RSTL}	8	10.5
t_{PDH}	0.7	1.3
t_{MSP}	1.8	~~2.2~~ 2.4
$t_{PDL, E}$	2.8	5.2
$t_{PDL, E\ w/\ CRM}$	21	~~31~~ 39
t_R	0.025	0.5
t_{REC}	~~0.27~~ 0.5	~~0.33~~

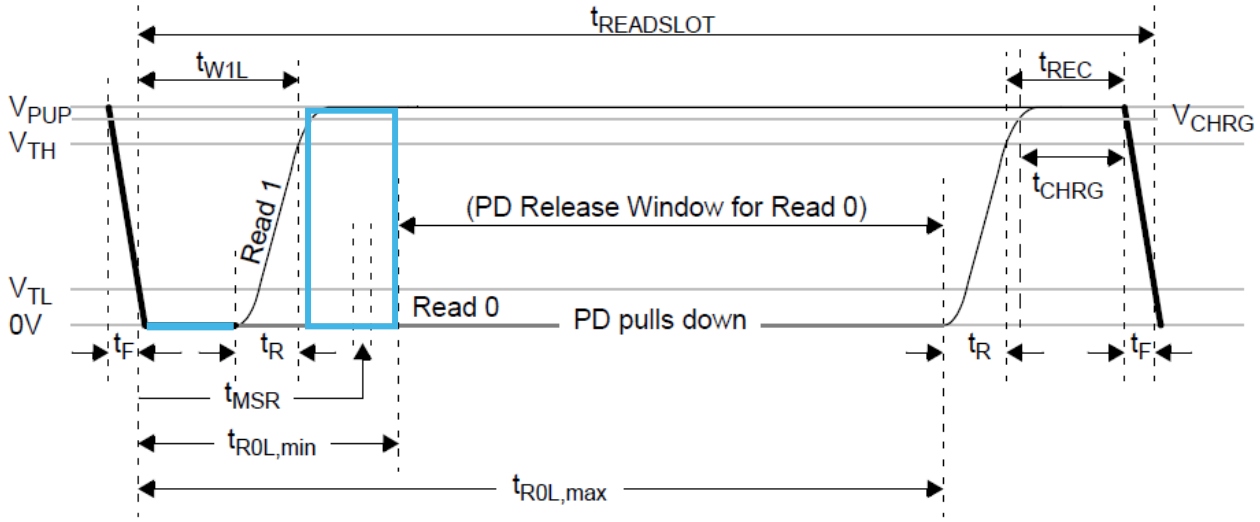
- C_{IN_CLASS} change lengthens real-world Reset component timings
- T_{PDL} was by far the tightest PD timing accuracy requirement
  - Make rationale and economically feasible by increasing to ~+/-20%
- Incorporate t_{REC} change as proposed previously
- **Propose:** Changes as shown

Need to Address:

Solution Form:

Solution Details:

SCCP $t_{READSLOT}$ Timing



Parameter	Min	Max
t_F	0.025	0.25
t_{MSR}	0.9	~~1.1~~ 1.3
t_{R0L}	1.75	3.25
t_R	0.025	0.5
t_{REC}	~~0.27~~ 0.5	~~0.33~~
$t_{READSLOT}$		~~3.83~~ 5

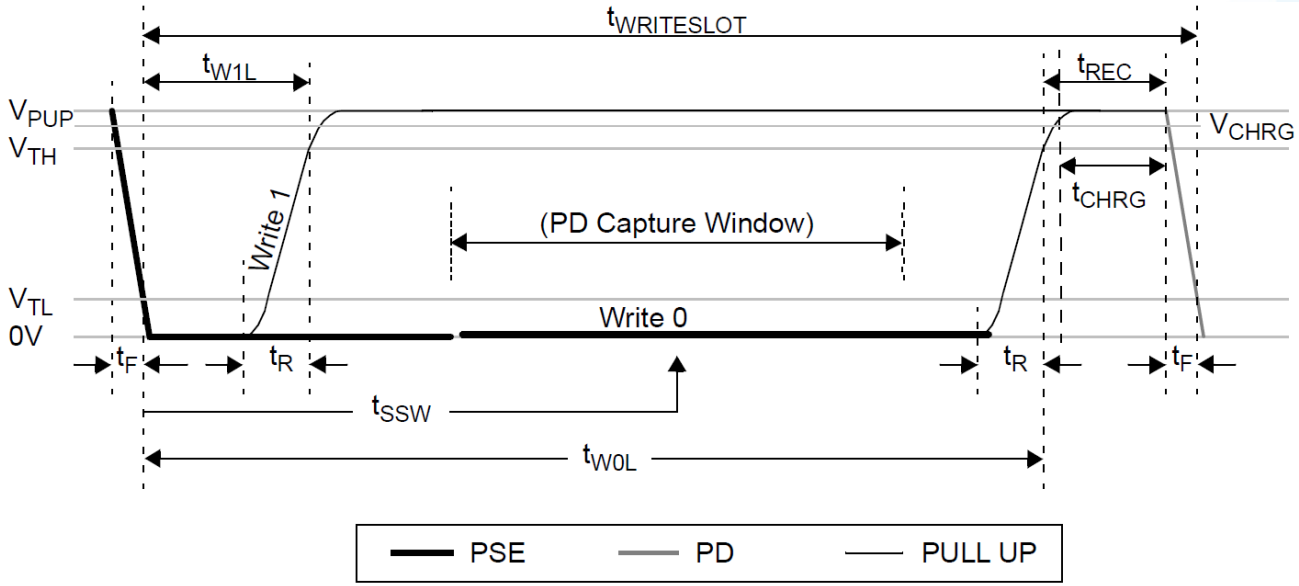
- Late changes to Read Slot component timing affected $t_{READSLOT}$ but were not accounted correctly
  - Original $t_{READSLOT,max}$ did not correlate to sum of components
- Original calcs did not account for PSE and PD discrepancies for t_R and t_F in end-to-end systems
- Incorporate t_{REC} change as proposed previously
- **Propose:** Changes as shown

Need to Address:

Solution Form:

Solution Details:

SCCP $t_{WRITESLOT}$ Timing



Parameter	Min	Max
t_F	0.025	0.25
t_{W1L}	0.09	~~0.61~~ 0.64
t_{W0L}	1.8	~~2.2~~ 2.6
t_R	0.025	0.5
t_{REC}	~~0.27~~ 0.5	~~0.33~~
$t_{WRITESLOT}$		~~2.78~~ 3.85

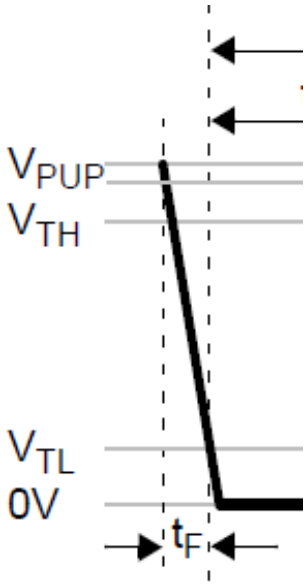
- Original calcs did not account for PSE and PD discrepancies for t_R and t_F in end-to-end systems
- C_{IN_CLASS} change lengthens real-world Write Slot component timings
- Incorporate t_{REC} change as proposed previously
- **Propose:** Changes as shown

Need to Address:

Solution Form:

Solution Details:

SCCP t_F Timing



Parameter	Min	Max
t_F	~~0.025~~ 0	0.25

- $t_{F,min}$ is over-specified and serves as a design recommendation while serving no interoperability value
  - Strong negative effect on economic feasibility
- **Propose:** Change as shown

Need to Address:

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Solution Details:

Figure 104-10 Reset command

Technical, 802.3cg, Page 95, Figure 104-10

Comment

V_CHRG and t_CHRG requirements are limiting without bringing value to the standard.

Suggested Remedy

Modify Figure 104-10 as shown.

Remove V_CHRG and associated voltage line.

Remove t_CHRG arrow and text.

Remove timing reference dashed line at right end of t_CHRG arrow.

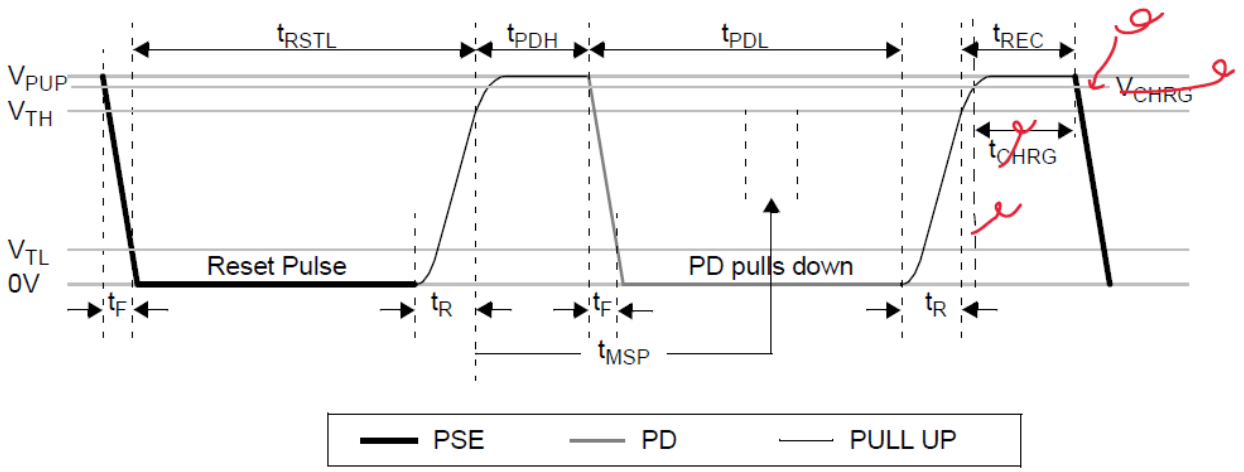

Figure 104–10—Reset command timing diagram

Need to Address:

Solution Form:

Solution Details:

Figure 104-11 Write 0/1 slot

Technical, 802.3cg, Page 96, Figure 104-11

Comment

V_CHRG and t_CHRG requirements are limiting without bringing value to the standard.

Suggested Remedy

Modify Figure 104-11 as shown.

Remove V_CHRG and associated voltage line.

Remove t_CHRG arrow and text.

Remove timing reference dashed line at right end of t_CHRG arrow.

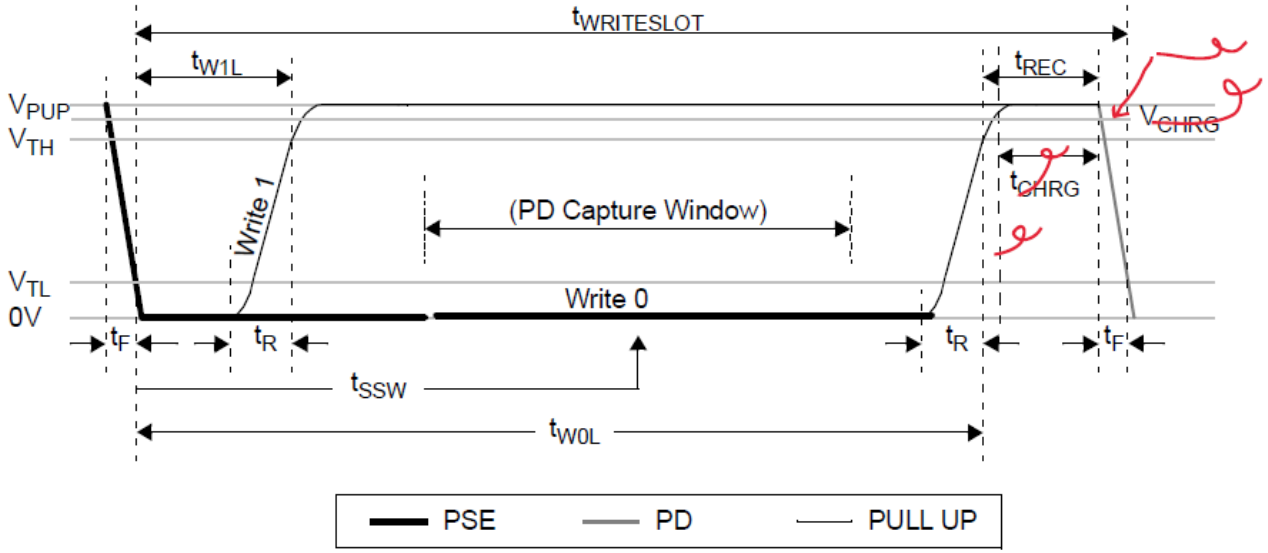

Figure 104–11—Write 0/1 slot timing diagram

Need to Address:

Solution Form:

Solution Details:

Figure 104-12 Read 0/1 slot

Technical, 802.3cg, Page 96, Figure 104-12

Comment

V_CHRG and t_CHRG requirements are limiting without bringing value to the standard.

Suggested Remedy

Modify Figure 104-12 as shown.

Remove V_CHRG and associated voltage line.

Remove t_CHRG arrow and text.

Remove timing reference dashed line at right end of t_CHRG arrow.

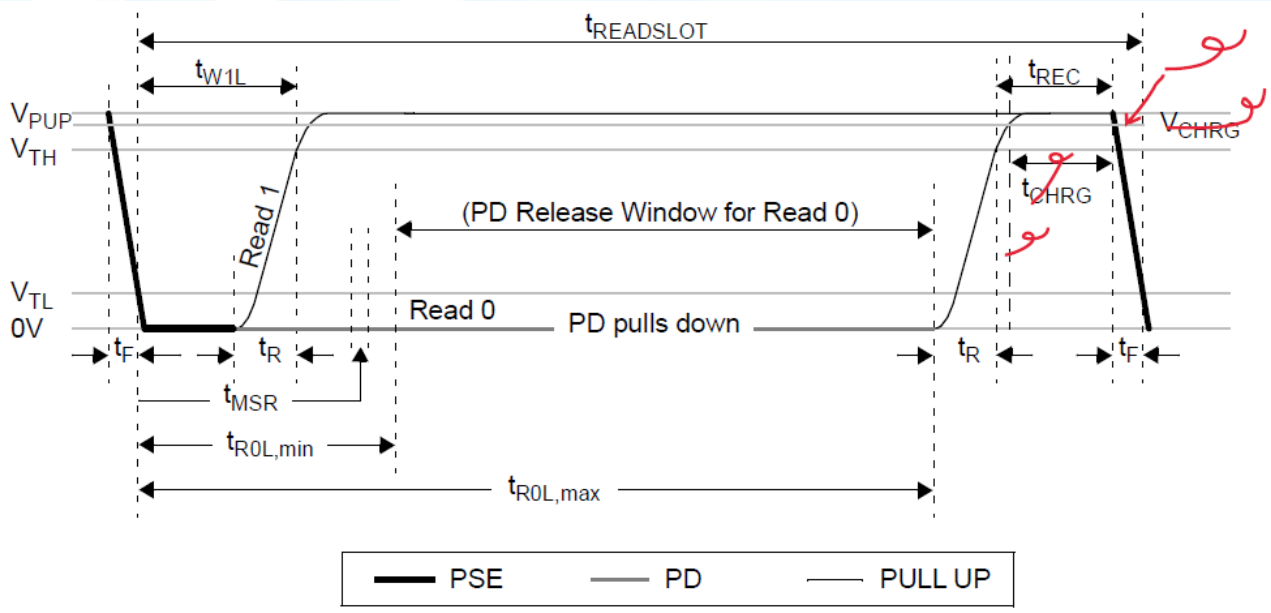

Figure 104–12—Read 0/1 slot timing diagram

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Solution Form:

Solution Details: