Clause 104 Maintenance Requests #5

Karl Peterson

Heath Stewart

ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

Overview

Item	Updated?
MDI Fault Tolerance (PSE)	New

MDI Fault Tolerance

- Type E Clause 104 PSEs and PDs, when co-located with Clause 146 MDIs, are required to meet a significant set of fault tolerance requirements as set forth in 104.6.2, 146.8.5, and 146.8.6
- We propose the fault tolerance has been driven by the following considerations
  - 146.8.5 and 146.8.6 are intended to encourage the deployment of robust PDs and data-only endpoints
  - A PSE should not be back-powered as described in 146.8.5 and 146.8.6, and certainly not for infinity
  - Any additional robustness a PSE would like to adopt is a value-add feature and should be outside the scope of the standard
- Specifically, we propose the fault tolerance requirements should not apply to a Clause 104 PSE

PSE MDI Fault Tolerance

Need to Address: **TODO**

Solution Details: **TODO**

Technical, 802.3cg, Page 94, 104.6.2

Comment

PSE fault tolerance adds cumbersome requirements to implementations. By design of the standard PSEs will not be powered by other PSEs.

Suggested Remedy

Change 104.6.2 second sentence from

The PI for Type E PSEs and PDs shall meet the fault tolerance requirements as specified in 146.8.5 and 146.8.6.

To

The PI for Type E ~~PSEs and~~ PDs shall meet the fault tolerance requirements as specified in 146.8.5 and 146.8.6.

PSE MDI Fault Tolerance

Need to Address: **TODO**

Solution Details: **TODO**

Technical, 802.3cg, Page 166, 146.8.6

Comment

104.6.2 references 146.8.6 which specifies a 60V, 2A fault tolerance requirement. PSE fault tolerance adds cumbersome requirements to implementations. By design of the standard PSEs will not be powered by other PSEs.

Suggested Remedy

Change 146.8.6 first sentence from

The wire pair of the MDI shall withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, as per Table 146–9, under all operating conditions, for an indefinite period of time.

To

The wire pair of the MDI, with the exception of MDIs encompassing Clause 104 PSEs, shall withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, as per Table 146–9, under all operating conditions, for an indefinite period of time with the source current limited to 2000mA.

PSE MDI Fault Tolerance

Need to Address: **TODO**

Solution Details: **TODO**

Technical, 802.3cg, Page 166, 146.8.5

Comment

104.6.2 references 146.8.5 which specifies a 60V, 2A fault tolerance requirement. PSE fault tolerance adds cumbersome requirements to implementations. By design of the standard PSEs will not be powered by other PSEs.

Suggested Remedy

Change 146.8.5 first sentence from

The DTE shall withstand without damage the application of any voltages between 0 V dc and 60 V dc with the source current limited to 2000 mA, applied across BI_DA+ and BI_DA–, in either polarity, under all operating conditions, for an indefinite period of time.

To

The DTE, with the exception of MDIs encompassing Clause 104 PSEs, shall withstand without damage the application of any voltages between 0 V dc and 60 V dc with the source current limited to 2000 mA, applied across BI_DA+ and BI_DA–, in either polarity, under all operating conditions, for an indefinite period of time.

Current State of 802.3dd Draft 1.0

146.8.6 MDI fault tolerance

Editor's Note (to be removed prior to Working Group ballot):

Motion #1 7/20/21: Stewart_3dd_01a_06152021.pdf slide 4

Change the first paragraph of 146.8.6, inserted by IEEE Std 802.3cg-2019, as shown:

The wire pair of the MDI shall withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, as per Table 146–9, under all operating conditions, for an indefinite period of time with the source current limited to 2000 mA. Normal operation shall resume after the short circuit(s) is/are removed.

Editor's Note (to be removed prior to Working Group ballot):

Motion #1 7/20/21: Stewart_3dd_01a_06152021.pdf slide 4

Delete NOTE at the end of 146.8.6 inserted by IEEE Std 802.3cg-2019, as shown:

~~NOTE—Typically, industrial control circuits are SELV/PELV limited to a maximum voltage of 60 V. The maximum current is limited by the 50 Ω termination resistors in each signal line. Depending on the internal structure of the PHY IC, additional external clamping diodes could be necessary. Due to the AC signal coupling, the maximum current is only applied while charging the signal coupling capacitors~~

Changes per stewart_3dd_02_06152021