Cl **FM** *SC* **FM** *P* **1** *L* **10** # 110

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"Amendment:" - there should be an amendment number here. According to pages 13 and 14, this would be number 10. But 9 amendments before a revision is too many so there should be another roll-up and this could be amendment 1 of 802.3-2023.

SuggestedRemedy

Insert number or placeholder. Also on pages 11 and 27. Add it on page 14. If some amendment numbers including this one are provisional, that can be stated.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
As the comment alludes, the amendment number that will be assigned to this amendment is not known at this time with any certainty. An amendments number may be inserted once a number is known with better certainty, likely near the end of WG Ballot.

Cl **FM** *SC* **FM** *P* **1** *L* **30** # 111

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation. Draft D1.0 is prepared for task force preview

SuggestedRemedy

Media Access Control parameters for 800 Gb/s and Physical Layers and management parameters for 400 Gb/s and 800 Gb/s operation. Draft D1.0 is prepared for Task Force preview

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The comment appears to be pointing out that capitalization on some words need s to be corrected.
Change: "Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation. Draft D1.0 is prepared for task force preview"
To:
"Media Access Control parameters for 800 Gb/s and Physical Layers and management parameters for 400 Gb/s and 800 Gb/s operation. Draft D1.0 is prepared for Task Force preview"
Implement with editorial license.

Cl **FM** *SC* **FM** *P* **6** *L* **39** # 112

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The superscript 3 should follow IEEE Xplore, not "contact IEEE."

SuggestedRemedy

Get the template at https://standards.ieee.org/develop/drafting-standard/resources/ fixed and implement the change.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
This footnote location is the same as in the cited template. This text is an official statement copied to the IEEE 802.3 template from the IEEE SA template. According to the 2021 IEEE SA Standards Style Manual , this text "Shall not be altered."

Cl **FM** *SC* **FM** *P* **8** *L* **12** # 178

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Task Force name Task Force

SuggestedRemedy

Task Force 3 times

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.
Delete "Task force name", three instances
Also, add list of clause editors.
Implement with editorial license.
[Editor's note: The page/line were change from 1/8 to 8/12.]

Cl **FM** *SC* **FM** *P* **10** *L* **1** # 113

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"When the IEEE-SA Standards Board": duplicate section

SuggestedRemedy

Remove

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The group of text starting with "When the IEEE-SA Standards Board:" is repeated twice. Remove one instance.

Implement with editorial license.

Cl **FM** *SC* **FM** *P* **27** *L* **48** # 114

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

3bj and 3bk!! They were approved in 2013 and 2014. 3cy uses 3cx and 3cz as its examples, 3cz uses 3dd, 3cs, 3db, 3ck, 3de and 3cx

SuggestedRemedy

Instead of or as well as this bad example, list all the exact amendments and drafts that this draft is built against, as P802.3cz does. Also, say which drafts affect this draft and which are believed not to, preferably clause by clause. The editors must have and agree this information; no reason not to share it with the volunteers who do the review work, and the staff editors.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The example projects listed are indeed obsolete. This example list from the FrameMaker template needs to be updated for each project and may again change as previous amendments are incorporate into a revision. The examples are not really required so these examples should be deleted here and in the template.
Delete "(e.g., IEEE P802.3bj and IEEE P802.3bk)"

Cl **1** *SC* **1.4** *P* **18** *L* **47** # 115

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

This project is adding another page of definitions to a very long section that doesn't have the usual pdf bookmarks.

SuggestedRemedy

To mitigate the deterioration of document structure and usability, divide 1.4 Definitions into subclauses, e.g.
1.4.1 1 to 8
1.4.2 A to G
1.4.3 H to M
1.4.4 N to S
1.4.5 T to Z
If Frame can deliver 1.4.0 ... 1.4.8 1.4.A ... 1.4.Z (some such as 1.4.3 are not needed), that would be even more user-friendly.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment is asking for broad changes to the base standard that are not related directly the new content that is being added by this amendment. Such sweeping changes should be addressed using the Base Standard maintenance process.

Cl **1** *SC* **1.5** *P* **30** *L* **30** # 116

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

This project is adding to an already long section that lacks the usual level of subdivision (somewhere around one subclause per page would be normal)

SuggestedRemedy

To mitigate the deterioration of document structure and usability, divide 1.5 Abbreviations into several subclauses

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment is asking for broad changes to the base standard that are not related directly the new content that is being added by this amendment. Such sweeping changes should be addressed using the Base Standard maintenance process.

Cl **30** *SC* **30.5** *P* **33** *L* **45** # 16

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

The base standard and 802.3db all list the "with reach up to at least xxx." to differentiate between the various Phy's. This draft does not.

SuggestedRemedy

Add the reach information to the new Phys.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

change 400GBASE-DR4 description to:
"400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD with reach up to at least 500 m as specified in Clause 124"

change 400GBASE-DR4-2 description to:
"400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 124"

change 800GBASE-DR4 description to:
"800GBASE-R PCS/PMA over 8-lane single-mode fiber PMD with reach up to at least 500 m as specified in Clause 124"

change 800GBASE-DR4-2 description to:
"800GBASE-R PCS/PMA over 8-lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 124"

change 800GBASE-SR8 description to:
"800GBASE-R PCS/PMA over 8-lane multimode fiber PMD with reach up to at least 100 m as specified in Clause 167"

change 800GBASE-VR8 description to:
"800GBASE-R PCS/PMA over 8-lane multimode fiber PMD with reach up to at least 50 m as specified in Clause 167"

Implement with editorial license.

Cl **30** *SC* **30.5.1.1.2** *P* **33** *L* **1** # 92

Wang, Haojie China Mobile

Comment Type **ER** *Comment Status* **D** *(bucket1)*

There should be "800GBASE-R" other than "400GBASE-R"

SuggestedRemedy

Change "400GBASE-R" to "800GBASE-R"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **30** *SC* **30.5.1.1.2** *P* **33** *L* **3** # 93

Wang, Haojie China Mobile

Comment Type **ER** *Comment Status* **D** *(bucket1)*

There should be "800GBASE-R" other than "400GBASE-R"

SuggestedRemedy

Change "400GBASE-R" to "800GBASE-R"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.1.2.163** *P* **41** *L* **50** # 70

Lusted, Kent Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

The paragraph provides mapping of registers 1.1220-1.1223 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

SuggestedRemedy

change:
" Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223."

to:
" Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, lane 3 maps to register 1.1223, lane 4 maps to register 1.1224, lane 5 maps to register 1.1225, lane 6 maps to register 1.1226, and lane maps to register 1.1227."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #46

Cl **45** *SC* **45.1.2.165** *P* **42** *L* **8** # 71

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

The paragraph provides mapping of registers 1.1320-1.1323 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

SuggestedRemedy

change:
" Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323."

to:
" Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, lane 3 maps to register 1.1323, lane 4 maps to register 1.1324, lane 5 maps to register 1.1325, lane 6 maps to register 1.1326, and lane maps to register 1.1327."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #30

Cl **45** *SC* **45.1.2.167** *P* **42** *L* **23** # 72

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

The paragraph provides mapping of registers 1.1420-1.1423 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

SuggestedRemedy

change:
" Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423."

to:
" Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, lane 3 maps to register 1.1423, lane 4 maps to register 1.1424, lane 5 maps to register 1.1425, lane 6 maps to register 1.1426, and lane maps to register 1.1427."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #31.

Cl **45** *SC* **45.2.1.6** *P* **36** *L* **3** # 43

Huber, Tom — Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Since the table includes 400ZR as existing text, the editing instruction should note that the text shown is as modified by 802.3cw.

SuggestedRemedy

Add "(as modified by IEEE 802.3cw-202x)" after "Change Table 45-7"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.6** *P* **36** *L* **20** # 117

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

Where possible, entries should be in the standard order: slow to fast, short to long, wide to narrow. Here, we have to read upwards because the entries are listed backwards.

SuggestedRemedy

Swap VR8 and SR8

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.7.4** *P* **37** *L* **23** # 118

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

Missing entries in transmit fault, receive fault and transmit disable tables

SuggestedRemedy

Include rows for
100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, 400GBASE-SR4, 800GBASE-VR8, 800GBASE-SR8
and
400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, 800GBASE-DR8-2
Revise the rubrics.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.8** *P* **38** *L* **13** # 17

Dudek, Mike Marvell

Comment Type **E** *Comment Status* **D** *(bucket1)*

In table 45-12 "and" is used in the list for BR but it has been deleted for KR and CR. The table should be consistent for all rows.

SuggestedRemedy

Add the "and" before 800.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.23** *P* **39** *L* **23** # 44

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

Register 1.72 is added by 802.3cz; presumably 1.73 is what was intended here

SuggestedRemedy

Change 1.72 to 1.73

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.23** *P* **39** *L* **24** # 18

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

This is listing register 1.72 but 45.2.1.60b is listing the abilities in Register 1.73

SuggestedRemedy

Change to register 1.72. Also on line39

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #44

Cl **45** *SC* **45.2.1.161** *P* **41** *L* **34** # 45

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

SuggestedRemedy

Change "Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123."
to
"Lanes 0-7 map to registers 1.1120 to 1.1127, respectively."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.161** *P* **41** *L* **34** # 69

Lusted, Kent Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

The paragraph provides mapping of registers 1.1120-1.1123 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

SuggestedRemedy

change:
" Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123."

to:
" Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, lane 3 maps to register 1.1123, lane 4 maps to register 1.1124, lane 5 maps to register 1.1125, lane 6 maps to register 1.1126, and lane maps to register 1.1127."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #45

Cl **45** *SC* **45.2.1.161** *P* **41** *L* **34** # 19

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

The mapping of lanes 4-7 is not provided.

SuggestedRemedy

Add the mapping for those lanes. Also in 45.2.1.163 on line 50, 45.2.1.165 and 45.2.1.167

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #45

Cl **45** *SC* **45.2.1.161** *P* **41** *L* **34** # 119

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.

SuggestedRemedy

Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, and so on, up to lane 7 and register 1.1127.
Similarly in 45.2.1.163, 45.2.1.165, 45.2.1.167

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #45.

Cl **45** *SC* **45.2.1.163** *P* **41** *L* **50** # 46

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

SuggestedRemedy

Change "Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223."
to
"Lanes 0-7 map to registers 1.1220 to 1.1227, respectively."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.165** *P* **42** *L* **8** # 30

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

SuggestedRemedy

Change "Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323."
to
"Lanes 0-7 map to registers 1.1320 to 1.1327, respectively."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.167** *P* **42** *L* **23** # 31

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

SuggestedRemedy

Change "Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423."
to
"Lanes 0-7 map to registers 1.1420 to 1.1427, respectively."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.168** *P* **42** *L* **24** # 122

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **D** *PRBS seed (bucket1)*

This says "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function."
This is in a section defining the meanings of bits in a memory map. The memory map serves the sublayer, not the other way round. Advice about signal integrity should be in the clause concerned.

With only four polynomials and eight lanes, the polynomials themselves can't all be different, but that's OK. Impairment is very unlikely unless adjacent lanes use the same polynomial AND the PRBS13Qs in the training pattern are aligned in time with each other. We have written generations of PMD and AUI clauses that use the same pattern on multiple lanes, but they should be skewed, e.g. 120G.3.2.2: "For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated." The training frame is 98.3% PRBS13Q. In principle, one could incur the risk warned against with a lane carrying "identifier_i" = 0 and an adjacent lane carrying "identifier_i" = 4, with an unlucky timing offset between lanes. As "The PMD shall implement one instance of the PMD control function described in 136.8.11 for each lane", the state machine for each lane can be started and restarted asynchronous to adjacent lanes, so starting the training pattern with a different seed won't solve the issue. The text "For 8-lane use cases different initial seeds should be used where the same polynomial is being reused" recommends a course of action that, on investigation, doesn't address the issue. We should tell the reader what to avoid, not how to avoid it.

Also, the ETC spec has already covered this ground. It uses the same four polynomials and seeds, twice over. No implementation can follow the ETC spec AND this draft (because the default seeds differ) but there is no benefit in the difference.

SuggestedRemedy

1. Put signal integrity recommendations in the spec, not in the register definitions for a memory map!
2. Change "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function" to "The polynomial identifier for adjacent lanes should be unique to avoid a risk of impairment of the PMD control function".
3. Change "For 8-lane use cases different initial seeds should be used where the same polynomial is being reused." to "For 8-lane use cases, see 162.8.11.1."
4. Make the default seeds in Table 162-10a the same as in the ETC spec (seeds 4 to 7 are the same as seeds 0 to 3).
5. ETC say "it is recommended to ensure that physically adjacent lanes do not use the same polynomial". Recommend this.
6. Also, suggest that when there are more lanes than polynomials to use, significant correlation between any lanes can be avoided by a combination of seed and timing offset. Leave it to the implementer to choose how to do this.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Replace "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11. For 8-lane use cases different initial seeds should be used where the same polynomial is being reused."
with
"The polynomial identifier for adjacent lanes should be unique to avoid a risk of impairment of the PMD control function. If the same polynomial identifier is used for multiple lanes, different initial seeds should be used for each of those lanes. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11."
The adopted baseline clearly states what the default seeds in Table 162-10a should be (see: https://www.ieee802.org/3/df/public/22_09/lusted_3df_01a_2209.pdf). A user would be able to change the default values so that the seeds for lanes 4 to 7 match 0 to 3 by writing appropriate seed values to registers 1.1450 through 1.1457. Therefore it is not appropriate to change Table 162-10a.
See also the response to comment #139

Cl **45** *SC* **45.2.1.168** *P* **42** *L* **38** # 32

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

While the mapping of registers to what they control is obvious, it would be better to spell it out a bit more completely to maintain similar structure to the other clauses that are specifying registers per-lane.

SuggestedRemedy

Change "Register 1.1450 controls the PMD training pattern for PMD lane 0; register 1.1451 controls the PMD training pattern for PMD lane 1; etc."
to
"Registers 1.1450 to 1.1457 control the PMD training pattern for PMD lanes 0-7, respectively."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.1.168** *P* **42** *L* **38** # 120

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"for PMD lane 1; etc.": a bit terse and informal

SuggestedRemedy

Suggested rewording: Register 1.1450 controls the PMD training pattern for PMD lane 0, register 1.1451 controls the PMD training pattern for PMD lane 1, and so on, up to register 1.1457 and PMD lane 7.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #32.

Cl **45** *SC* **45.2.1.168** *P* **42** *L* **41** # 121

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

92.7.12 and 136.8.11.1.3

SuggestedRemedy

92.7.12, 136.8.11.1.3, or 162.8.11.1 as appropriate

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change the first sentence of the second paragraph of 45.2.1.168 so it reads as "Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training a particular PMD lane as described in 92.7.12, 136.8.11.1.3, or 162.8.11.1."

Cl **45** *SC* **45.2.1.168** *P* **42** *L* **41** # 33

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The text "and 136.8.11.1.3" is in 802.3-2022, so it should not be identified as a change.

SuggestedRemedy

Remove the underlining from this text.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The reference to 136.8.11.1.3 is not in the base standard so the underlineing should remain.

Cl **45** *SC* **45.2.1.168** *P* **42** *L* **42** # 34

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

The last 3 sentences would be clearer if the order of the last two sentences is swapped, and the (current) last sentence is written more generically to apply to any situation where a polynomial identifier is being reused.

SuggestedRemedy

Replace "The polynomial identifier for each lane
should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11. For 8-lane use cases different initial seeds should be used where the same polynomial is being reused."
with
"The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function. If the same polynomial identifier is used for multiple lanes, different initial seeds should be used for each of those lanes. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #122

Cl **45** *SC* **45.2.3** *P* **43** *L* **12** # 35

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Subclauses 45.2.3.24-26 all exist in 802.3-2022, so they should not be indicated as changes in the table.

SuggestedRemedy

Remove the underlining from 45.2.3.24, 45.2.3.25, 45.2.3.26.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
Although these clauses are in the base standard, there are no references to them in Table 45-233. Therefore it is appropriate to add them to the table with underlining.

Cl **45** *SC* **45.2.3** *P* **43** *L* **50** # 36

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Subclause 45.2.3.50 exists in 802.3-2022, so it should not be indicated as a change in the table.

SuggestedRemedy

Remove the underlining from 45.2.3.50

Proposed Response *Response Status* **W**

PROPOSED REJECT.
Although this subclause is in the base standard there is no reference to it in the table.
Therefore it is appropriate to add it to Table 45-233 with underlining.

Cl **45** *SC* **45.2.3.26a** *P* **44** *L* **24** # 62

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

Clause 172 (and 119) use a variable named amps_lock[x] for lane alignment lock status. Which was the name used in Cl91 and 161 for the FEC sublayers.

SuggestedRemedy

Bring in 45.2.3.25.* and 45.2.3.26.*

For indexes 16 to 32 change the "(see 82.2.19.2.2)." to be "(see 82.2.19.2.2) or amps_lock[16] (see 172.2.6.2.2)"

For indexes 0 to 15 and change the "(see 82.2.19.2.2)." to be "(see 82.2.19.2.2) or amps_lock[16] (see 119.2.6.2.2 and 172.2.6.2.2)"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.3.60.1** *P* **46** *L* **54** # 65

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

Various clause 45 registers need to some Clause 172 references added.

SuggestedRemedy

A reference to Clause 172 needs to be added to 45.2.3.49

A reference to 172.2.5.3 needs to be added to:
45.2.3.60.1
45.2.3.60.2
45.2.4.61.4
45.2.3.61.6
45.2.3.64
45.2.3.65
45.2.3.66
45.2.4.21.1
45.2.4.21.2
45.2.4.22.2
45.2.4.22.3
45.2.4.22.4
45.2.4.22.5
45.2.4.25
45.2.4.26
45.2.4.27
45.2.5.21.1
45.2.5.21.2
45.2.5.22.2
45.2.5.22.3
45.2.5.22.4
45.2.5.22.5
45.2.5.25
45.2.5.26
45.2.5.27

A reference to 172.2.6.2.2 needs to be added to:
45.2.3.61.1
45.2.3.61.2
45.2.3.61.3
45.2.3.61.5
45.2.4.22.1
45.2.5.22.1

A reference to 172.3.2 needs to be added to 45.2.3.62, 45.2.4.23 and 45.2.5.23

A reference to 172.3.3 needs to be added to 45.2.3.63, 45.2.4.24 and 45.2.5.24

A reference to 172.3.4 needs to be added to 45.2.3.58

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.4** *P* **47** *L* **4** # 1

Marris, Arthur Cadence Design Systems

Comment Type **T** *Comment Status* **D** *(bucket1)*

"45.2.4 PHY XS registers" and "45.2.5 DTE XS registers" subsections need to be brought into the 802.3df draft and modifications made to increase the number of service interface lanes specified from 20 to 32

SuggestedRemedy

Update "Table 45–314—PHY XS registers" and "Table 45–339—DTE XS registers" and relevant sunclauses to address this. This will include an extra "XS alignment status 5" register at location 54, adding extra "XS lane mapping" registers above 415, adding extra "FEC symbol error counter" registers above 631, and add bit 4.801.6 for "Local degraded SER received"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.4.4** *P* **46** *L* **54** # 53

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

Need to add 800G capablity register to PHY XS

SuggestedRemedy

Assign a bit in register 4.4 for 800G capable and create a description the same as the 400G bit replacing 400G with 800G

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.4.15** *P* **46** *L* **54** # 66

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

PHY XS AM lock registers need to be updated with 800G references and expanded to 32 AM lanes

SuggestedRemedy

Update (see 119.2.6.2.2) to (see 119.2.6.2.2 and 172.2.6.2.2) in 45.2.4.15.* and 45.2.4.16.* Add the extra 16 lanes of amps_lock as well as was done for the PCS registers.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.4.17** *P* **46** *L* **54** # 67

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

PHY XS lane mapping registers need to update with 800G references and expanded to 32 lanes

SuggestedRemedy

Bring in and update 45.2.4.17 and 45.2.4.18 adding references to Clause 171 and adding 16 more registers

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.4.19** *P* **46** *L* **54** # 68

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

PHY XS symbol error counter registers needs update with 800G references and expanded to 32 lanes

SuggestedRemedy

Bring in and update 45.2.4.19 and 45.2.4.20 adding references to 172.3.4 and adding 16 more counters

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.5.4** *P* **46** *L* **54** # 54

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

Need to add 800G capablity register to DTE XS

SuggestedRemedy

Assign a bit in register 5.4 for 800G capable and create a description the same as the 400G bit replacing 400G with 800G

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.5.15** *P* **46** *L* **54** # 55

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

DTE XS AM lock registers need to be updated with 800G references and expanded to 32 AM lanes

SuggestedRemedy

Update (see 119.2.6.2.2) to (see 119.2.6.2.2 and 172.2.6.2.2) in 45.2.4.15.* and 45.2.4.16.* Add the extra 16 lanes of amps_lock as well as was done for the PCS registers.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.5.17** *P* **46** *L* **54** # 56

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

DTE XS lane mapping registers need to update with 800G references and expanded to 32 lanes

SuggestedRemedy

Bring in and update 45.2.5.17 and 45.2.5.18 adding references to Clause 171 and adding 16 more registers

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.5.19** *P* **46** *L* **54** # 57

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

DTE XS symbol error counter registers needs update with 800G references and expanded to 32 lanes

SuggestedRemedy

Bring in and update 45.2.5.19 and 45.2.5.20 adding references to 172.3.4 and adding 16 more counters

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **120F** *SC* **120F.1** *P* **198** *L* **25** # 49

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

To maintain parallel structure with the rest of the sentence, the new 800G AUI should be introduced as 800Gb/s eight-lane

SuggestedRemedy

change "and eight-lane Attachment Unit Interface" to "800 Gb/s eight-lane Attachment Unit Interface"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
change "and eight-lane" to "and 800 Gb/s eight-lane".

Cl **120F** *SC* **120F.1** *P* **198** *L* **48** # 81

Lusted, Kent Intel Corporation

Comment Type **T** *Comment Status* **D** *(bucket1)*

Paragraph omits the eight-lane 800GAUI-8.

SuggestedRemedy

Replace the second sentence in the 5th paragaph with "Each 100GAUI-1, 200GAUI-2, 400GAUI-4, or 800GAUI-8 C2C data path contains one, two, four, or eight, respectively, differential lanes, which are AC coupled."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **120F** *SC* **120F.1** *P* **198** *L* **52** # 82

Lusted, Kent Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

The mapping of the differential voltage level to the PAM4 symbol is missing in Annex 120F. It is also not present in Annex 120F in IEEE Std. 802.3ck-202x. The mapping of the differential voltage level to the PAM4 symbol level is important for interoperability.

SuggestedRemedy

Add a new sentence to the 5th paragraph: "The highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
In the sixth paragraph, change "The C2C transmitter and the receiver use PAM4 signaling"
To:
"The C2C transmitter and receiver use PAM4 signaling. The highest differential level corresponds to the tx_symbol or rx_symbol value three, and the lowest differential level corresponds to the tx_symbol or rx_symbol value zero."

Cl **120G** *SC* **120G.1** *P* **204** *L* **44** # 176

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Each 100GAUI-1, 200GAUI-2, 400GAUI-4 C2M, *and* 800GAUI-8 C2M data path contains one, two, four, *or* eight differential lanes

SuggestedRemedy

Change and to or

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **120G** *SC* **120G.3.2.1** *P* **209** *L* **21** # 87

Opsasnick, Eugene Broadcom

Comment Type **ER** *Comment Status* **D** *(bucket1)*

In Table 120G-4, four instances of "800GAUI-4" in last two rows of the table should likely be "800GAUI-8"

SuggestedRemedy

Replace "800GAUI-4" with "800GAUI-8"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change 800GAUI-4 to 800GAUI-8 in the bottom two rows of the table (4 instances).

Cl **124** *SC* **124.1** *P* **59** *L* **24** # 37

Huber, Tom Nokia

Comment Type **T** *Comment Status* **D** *(bucket1)*

Table 124-1 was modified by 802.3ck-2022

SuggestedRemedy

Change the editing instruction to add "(as modified by IEEE 802.3ck-2022)", and insert the rows for Annexes 120F and 120G into the table.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Implement proposed remedy with editorial license

Cl **124** *SC* **124.1** *P* **61** *L* **36** # 38

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Since there are only two items in the list, they should be separated with and rather than a comma

SuggestedRemedy

Change "400GBASE-DR4, 400GBASE-DR4-2" to "400GBASE-DR4 and 400GBASE-DR4-2"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.1** *P* **61** *L* **36** # 124

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

400GBASE-DR4, 400GBASE-DR4-2

SuggestedRemedy

400GBASE-DR4 and 400GBASE-DR4-2

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #38.

Cl **124** *SC* **124.2** *P* **62** *L* **13** # 125

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

six paragraphs 124.2

SuggestedRemedy

six paragraphs in 124.2

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change the instruction to:
"Change the first six paragraphs in 124.2 as follows:"

Cl **124** *SC* **124.2** *P* **62** *L* **16** # 95

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **D** *(bucket1)*

The space after "these" should be underlined.

SuggestedRemedy

Underline the space after "these"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.2** *P* **62** *L* **29** # 96

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **D** *(bucket1)*

The space after "have" should be underlined

SuggestedRemedy

Underline the space after "have"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.3.1** *P* **63** *L* **13** # 89

He, Xiang Huawei

Comment Type **ER** *Comment Status* **D** *(bucket1)*

Looks like a typo. "16834 bit times" should be "16384 bit times"

SuggestedRemedy

Change 16834 to 16384.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.5.1** *P* **65** *L* **13** # 97

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **D** *(bucket1)*

Missing editing instruction to update the title of Figure 124-2 from "Block diagram for 400GBASE-DR4 transmit/receive paths" to "Block diagram for 400GBASE-DR4 or 400GBASE-DR4-2 transmit/receive paths"

SuggestedRemedy

Change the title of Figure 124-2
from
"Block diagram for 400GBASE-DR4 transmit/receive paths"
to
"Block diagram for 400GBASE-DR4 or 400GBASE-DR4-2 transmit/receive paths"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.5.4** *P* **65** *L* **49** # 98

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **D** *(bucket1)*

Missing comma after "400GBASE-DR4-2"

SuggestedRemedy

Add missing comma after " 400GBASE-DR4-2"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.7.1** *P* **68** *L* **47** # 100

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **D** *(bucket1)*

Table 124-6. The row "Launch power in OMAouter minus TDECQ, each lane (min)" only applies to 400GBASE-DR4 and not to 800GBASE-DR8.

SuggestedRemedy

Correct this row in accordance with the comment to indicate that is row only applies to 400GBASE-DR$ and not to 800GBASE-DR8. It should look more like the "TDECQ – 10log10(Ceq)c (max)" row on line 52.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Implement proposed remedy with editorial license.

Cl **124** *SC* **124.7.1** *P* **69** *L* **15** # 101

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **D** *(bucket1)*

Table 124-6. Why are the rows "Transmitter overshoot and undershoot (max)", Transmitter power excursion (max) and "Transmitter transition time (max)" all in itallic ?

SuggestedRemedy

Change the font of the text in the rows mentioned in the comment to standard table text font.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.7.1** *P* **69** *L* **29** # 102

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **D** *(bucket1)*

Table 124-6. Footnote "b" only applies to 400GBASE-DR4

SuggestedRemedy

Update footnote b to make it clear this footnote only applies to 400GBASE-DR4 (see what was done in Table 140-6 in 3cu as an example).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Implement proposed remedy with editorial license.

Cl **124** *SC* **124.7.3** *P* **72** *L* **40** # 104

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **D** *(bucket1)*

The comma after "400GBASE-DR4" should be underlined.

SuggestedRemedy

Underline the comma after "400GBASE-DR4".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **124** *SC* **124.8.5a** *P* **76** *L* **15** # 88

Opsasnick, Eugene Broadcom

Comment Type **ER** *Comment Status* **D** *(bucket1)*

In second line of paragraph, "800GBASE-DR4" should probably be "...-DR8". Same text appears on line 25 in 124.8.5b, and on page 77, line 29, section 124.8.9.2.

SuggestedRemedy

Replace "800GBASE-DR4" with "800GBASE-DR8".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #13.

Cl **124** *SC* **124.8.5a** *P* **76** *L* **16** # 13

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

800GBASE-DR4 is not part of this specification

SuggestedRemedy

Change to 800GBASE-DR8 Also on line 25 and page 77 line 29

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change 800GBASE-DR4 to 800GBASE-DR8

Cl **124** *SC* **124.11.3.1** *P* **80** *L* **34** # 14

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

The optical lane assignments are wrong in figure 124-6.

SuggestedRemedy

Change them to match Figure 124-6 in the base document.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Figure was intended to be the same as in in-force figure. Probably formatting problem.
Check and update figure with editorial license

Cl **124** *SC* **124.11.3.1.1** *P* **80** *L* **32** # 26

Bruckman, Leon Huawei

Comment Type **E** *Comment Status* **D** *(bucket1)*

In figure 124-6 the labels are all squeezed together

SuggestedRemedy

Spread the TX/RX labels to the right position

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #14

Cl **124** *SC* **124.11.3.1.1** *P* **80** *L* **32** # 94

Wang, Haojie China Mobile

Comment Type **ER** *Comment Status* **D** *(bucket1)*

The positions of ''Rx'' in figure 124-6 is inconsistent with the text at line 27, which is depicted as the right-most four positions.

SuggestedRemedy

Plot the four ''Rx'' at the right-most four positions.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #14.

Cl **124** *SC* **124.11.3.1.1** *P* **80** *L* **33** # 134

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

TxTxTxTxRxRxRxRx

SuggestedRemedy

Should look like the base doc

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #14.

Cl **124** *SC* **124.11.3.1.1** *P* **80** *L* **38** # 106

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **D** *(bucket1)*

Figure 124-6 indicates a different lane assignment for 400GBASE-DR4 than is in Clause 124 of the published version of the 802.3 standard. This would appear to make 400GBASE-DR4 incompatible with the current published standard.

SuggestedRemedy

Change the lane assignment in Figure 124-6 in 802.3df D1.0 to match the lane assignment in Figure 124-6 of "P802.3_D3p2".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #14.

Cl **124** *SC* **124.11.3.3** *P* **81** *L* **29** # 15

Dudek, Mike Marvell

Comment Type **E** *Comment Status* **D** *(bucket1)*

Should be plural

SuggestedRemedy

Change "800GBASE-DR8 and 800GBASE-DR8-2 has" to "800GBASE-DR8 and 800GBASE-DR8-2 have"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.1** *P* **84** *L* **35** # 73

Lusted, Kent Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

In Table 162-3a, the rightmost column heading is incorrect as the table refers to 800GBASE-CR8.

SuggestedRemedy

Change rightmost column heading to "800GBASE-CR8"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.1** *P* **85** *L* **8** # 39

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Elsewhere in the clause (e.g. in 162.4), 800GAUI-n is used, which seems desirable since it will be more future-proof toward the 200G/lane AUI that will be added.

SuggestedRemedy

Change 800GAUI-8 to 800GAUI-n.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.7** *P* **89** *L* **24** # 74

Lusted, Kent Intel Corporation

Comment Type **E** *Comment Status* **D** *(bucket1)*

With the addition of new sub-note "a", the rest of the sub-notes from the table 162-5 in P802.3ck are re-indexed. (i.e. 'a' becomes 'b', 'b' becomes 'c'). However, the new notes 'b' and 'c' do not have the relevant strikeout text

SuggestedRemedy

Correct as necessary

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Table footnote are numbered automatically in FrameMaker and cannot be struck out.
Change the editorial instruction from
"Change Table 162–5, Table 162–6, and Table 162–7 as follows:"
to
"Change Table 162–5, Table 162–6, and Table 162–7, including footnotes, as follows:"

Cl **162** *SC* **162.7** *P* **89** *L* **49** # 75

Lusted, Kent Intel Corporation

Comment Type **E** *Comment Status* **D** *(bucket1)*

With the addition of new sub-note "a", the rest of the sub-notes from the table 162-6 in P802.3ck are re-indexed. (i.e. 'a' becomes 'b', 'b' becomes 'c'). However, the new notes 'b' and 'c' do not have the relevant strikeout text

SuggestedRemedy

Correct as necessary

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #74.

Cl **162** *SC* **162.8.1** *P* **91** *L* **22** # 84

Opsasnick, Eugene Broadcom

Comment Type **ER** *Comment Status* **D** *(bucket1)*

At top-middle of Figure 162-2, the added text reads "800GBASE-CR4 8x", but "-CR4" should probably be "-CR8".

SuggestedRemedy

Replace "800GBASE-CR4 8x" with "800GBASE-CR8 8x".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.9.5** *P* **93** *L* **36** # 141

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

This text is an informative NOTE in the standard in force, as below. While I can see the reason to make it normative for the transmitter, for the receiver this information about trannsmitter behavoiur is explanation, not something the receiver does.

SuggestedRemedy

Change it from a normative table footnote to an informative table note. Similarly for 163.9.3.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.11** *P* **94** *L* **51** # 20

Dudek, Mike Marvell

Comment Type **E** *Comment Status* **D** *(bucket1)*

There are 4 cable assembly types

SuggestedRemedy

Change "three" to "four"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.13** *P* **96** *L* **4** # 77

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

In P802.3ck, Clause 162.13 is the environmental specifications and Clause 162.14 is the PICS. The 162.13 sub clause is missing from the draft and creates an issue where the PICs became sub clause 162.13.

SuggestedRemedy

Fix editing instruction on p96, line 1 to reference the heading of 162.14

Correct the sub clause number for the PICS to 162.14 in the title and the sub clauses.

Update all editing instructions as required.

Implement with editorial license

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162** *SC* **162.13.3** *P* **97** *L* **21** # 76

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

Row entry for PMA800 has incorrect status value of "CR4:M". It should be "CR8:M"

SuggestedRemedy

Change to "CR8:M"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162B** *SC* **162B** *P* **215** *L* **11** # 83

Lusted, Kent — Intel Corporation

Comment Type **E** *Comment Status* **D** *(bucket1)*

The title of Annex 162B is missing "C2M" after the 800GAUI-8 entry.

SuggestedRemedy

Add "C2M" after 800GAUI-8

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **162B** *SC* **162B** *P* **215** *L* **11** # 51

Huber, Tom — Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The title is missing 'C2M' for 800GAUI-8

SuggestedRemedy

Add 'C2M' to the end of the title

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **163** *SC* **163.3** *P* **100** *L* **27** # 78

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **D** *(bucket1)*

Text references "CR" PMD types in the PMD service interfaces for Clause 163, which is for backplanes.

SuggestedRemedy

Change "100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4" to "100GBASE-KR1, 200GBASE-KR2, and 400GBASE-KR4"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The text states that the KR* service interfaces are identical to those of CR*. The addition of "KR8" was erroneous.
Resolve using the response to comment #22.

Cl **163** *SC* **163.3** *P* **100** *L* **27** # 85

Opsasnick, Eugene — Broadcom

Comment Type **ER** *Comment Status* **D** *(bucket1)*

At end of first line of paragraph, 800GBASE-KR4 (wraps to line 28), "-KR4" should probably be "-KR8"

SuggestedRemedy

Replace "800GBASE-KR4" with "800GBASE-KR8" and use non-breaking hyphen.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **163** *SC* **163.3** *P* **100** *L* **28** # 21

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

Should be 800GASE-KR8 not KR4

SuggestedRemedy

fix it.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **163** *SC* **163.3** *P* **100** *L* **29** # 22

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

should be 800GBASE-CR8 not KR8

SuggestedRemedy

Change it.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **167** *SC* **167.2** *P* **110** *L* **23** # 23

Dudek, Mike Marvell

Comment Type **E** *Comment Status* **D** *(bucket1)*

"have" should be "has" ("or" makes it singular)

SuggestedRemedy

change it.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Replace "PMD have eight" with "PMD has eight".

Cl **167** *SC* **167.5.1** *P* **111** *L* **7** # 142

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Strange to talk about 800G before 100G and 200G: not the usual order (slow MAC to fast MAC).

SuggestedRemedy

The block diagrams for 100GBASE-VR1 and 100GBASE-SR1 are equivalent to Figure 167-2, but for one lane per direction. The block diagrams for 200GBASE-VR2 and 200GBASE-SR2 are equivalent to Figure 167-2, but for two lanes per direction. The block diagrams for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for eight lanes per direction.
or
The block diagrams for 100GBASE-VR1 and 100GBASE-SR1, for 200GBASE-VR2 and 200GBASE-SR2, and for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for one, two and eight lanes per direction respectively.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change editing instruction to "Replace the first paragraph in 167.5.1 with the following:" with the text "The PMD block diagram for 400GBASE-VR4 or 400GBASE-SR4 is shown in Figure 167–2. The block diagrams for 100GBASE-VR1 and 100GBASE-SR1 are equivalent to Figure 167-2, but for one lane per direction. The block diagrams for 200GBASE-VR2 and 200GBASE-SR2 are equivalent to Figure 167-2, but for two lanes per direction. The block diagrams for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for eight lanes per direction."

Cl **167** *SC* **167.7.1** *P* **114** *L* **10** # 192

Nicholl, Gary Cisco Systems

Comment Type **E** *Comment Status* **D** *(bucket1)*

Table 167-7. The order of the PMDs in the 'Signaling rate" row is different from what was done in Clause 124.

SuggestedRemedy

Proposing to reorder the data in this row to put the lower speed and lower lane count PMDs first, i.e.
"Other PMDs"
"800GBASE-VR8, 800GBASE-SR8 PMDs"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change the order and associated parameters as proposed.

Cl **167** *SC* **167.7.2** *P* **115** *L* **12** # 193

Nicholl, Gary Cisco Systems

Comment Type **E** *Comment Status* **D** *(bucket1)*

Table 167-8. The order of the PMDs in the 'Signaling rate" row is different from what was done in Clause 124.

SuggestedRemedy

Proposing to reorder the data in this row to put the lower speed and lower lane count PMDs first, i.e.
"Other PMDs"
"800GBASE-VR8, 800GBASE-SR8 PMDs"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change the order and associated parameters as proposed.

Cl **167** *SC* **167.8.6** *P* **118** *L* **6** # 194

Nicholl, Gary Cisco Systems

Comment Type **E** *Comment Status* **D** *(bucket1)*

Table 167-12. The font for the text in the "PMD Type" column looks incorrect. Also the editing instruction is "change this table", but then no underline or strickthrough. Perhaps the editing instruction should have been "Replace Table 167-12 with the following:" ?

SuggestedRemedy

Change the font in the "PMD Type" column to use the standard table font and updte the editing instruction to "Replace Table 167-12 with the following:"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Correct the font and text type. Editing instruction is correct, underline new text and correct text alignment.

Cl **167** *SC* **167.8.6** *P* **118** *L* **9** # 144

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Font problem

SuggestedRemedy

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #194.

Cl **169** *SC* **169.1.2** *P* **127** *L* **36** # 40

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The dashed lines between the OSI layers and the Ethernet layers are not in the correct locations.

SuggestedRemedy

Align the upper two dashed lines with the boundaries of the data link layer in the OSI model.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **169** *SC* **169.1.2** *P* **128** *L* **4** # 41

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Singular/plural disagreement in item a)

SuggestedRemedy

Change "when implemented as logical interconnection points" to "when implemented as a logical interconnection point"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **169** *SC* **169.3.2** *P* **133** *L* **45** # 58

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

800GAUI-n is not listed in the list of acronyms for Figure 169-3

SuggestedRemedy

Add 800GAUI-n to list of acronyms in Figure 169-3

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **169** *SC* **169.5** *P* **134** *L* **53** # 150

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

116.5 says "Skew (or relative delay) can be introduced between lanes". This says "Skew (or relative delay) can be introduced between PCS lanes" which gives a false impression that PMA and PMD lanes don't get skewed.

SuggestedRemedy

Delete "PCS", once.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
Skew is constrained for each sublayer to limit the net skew between PCS lanes so that the cumulative skew between PCS lanes does not exceed the ability of the specified PCS deskew function.

Cl **169** *SC* **169.5** *P* **136** *L* **10** # 80

Lusted, Kent Intel Corporation

Comment Type **ER** *Comment Status* **D** *(bucket1)*

Figure 169-4 variable "q" should be italics like 'n' and 'p'. Both in middle and bottom of figure

SuggestedRemedy

consider changing 'q' to italics types

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change font to italic for variable q.
Implement with editorial license.

Cl **169** *SC* **169.5** *P* **136** *L* **27** # 151

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

points for single 800GAUI-n

SuggestedRemedy

points for a single 800GAUI-n

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
In Figure 169-4...
Change "800GBASE-R Skew points for single 800GAUI-n"
To: "800GBASE-R Skew points for a PHY with a single 800GAUI-n"
In Figure 169-5...
Change "Skew points for multiple 800GAUI-n"
To: "Skew points for a PHY with multiple 800GAUI-n"

Cl **169** *SC* **169.6** *P* **138** *L* **49** # 7

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **D** *fec degrade (bucket1)*

FEC degrade function is defined as optional in 116.6. Assuming it is optional here too, it should be stated, as in clause 116.

SuggestedRemedy

Add "(optional)" to the subclause title in 169.6.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The FEC degrade is indeed intended to be optional for 800 GbE as well. It is not sufficient or necessary to put the word "optional" in the title, rather the word should be included in the text.
Change: "FEC degrade functionality is identical"
To: "Optional FEC degrade functionality is identical"

Cl **170** *SC* **170** *P* **141** *L* **1** # 152

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

This has got so little to say it's a waste of a clause number. The 100/200/400/800GMII is like the MAC: almost identical apart from rates, timing and optional EEE.

SuggestedRemedy

Merge 170 into 117 or better, merge 170 and 117 into 81.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification to support the suggested remedy.
The current structure of the draft is consistent with the approach taken by previous projects.

Cl **171** *SC* **171.2** *P* **150** *L* **4** # 195

Nicholl, Gary Cisco Systems

Comment Type **E** *Comment Status* **D** *(bucket1)*

800GXS should be 400GXS

SuggestedRemedy

Change
"PCS and 800GXS sublayers specified in 118.2"
to
"PCS and 400GXS sublayers specified in 118.2"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **171** *SC* **171.4** *P* **151** *L* **38** # 59

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

There is no am_lock variable in Clause 172

SuggestedRemedy

Change am_lock to amps_lock in Table 171-3 and 171-5

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **171** *SC* **171.4** *P* **152** *L* **18** # 153

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

activate_t
hreshold

SuggestedRemedy

Make these tables full width, make the right hand columns wider, also in Clause 172. It may be necessary to set break points in these long "words". In maintenance we might change to shorter names, e.g. FEC_degraded_SER_thresh_on

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Improve appearance of the variable names with editorial license.

Cl **171** *SC* **171.4** *P* **153** *L* **11** # 155

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

16 bits for 32 lanes

SuggestedRemedy

Need more registers

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Update Table 171-5 to align with register/bit definitions in Clause 45.

Cl **171** *SC* **171.4** *P* **153** *L* **11** # 154

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

Under "MDIO status variable" there is an entry "Lane 0 to 31 aligned" but this isn't a variable that indicates if lanes 0 to 31 are aligned. Table 45-350 has "Name"s Lane 0 aligned, Lane 1 aligned, and so on. Is there such a thing as an "MDIO variable" anyway? Clauses such as PCS have variables, MDIO has registers. The way of talking about such multilane things was solved long ago; e.g. "84.7.5 PMD lane-by-lane signal detect function"

SuggestedRemedy

Because a "variable" must be talking about one lane not the pair of registers recording 16 or 32 lanes, change "Lane 0 to 31 aligned" back to how it is in 117: "Lane x aligned" or "Lane i aligned" or better, "Lane aligned". "Lane-by-lane aligned" seems odd, but "DTE XS FEC symbol errors lane 0 to lane 31" below can be "DTE XS FEC symbol errors by lane" Similarly in several tables, also in other clauses such as 172, PCS.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change "Lane 0 to 31 aligned" to "Lane aligned, lane 0 to 31"
Change "Lane 0 to 31 mapping" to "Lane mapping, lane 0 to 31"

Cl **172** *SC* **172.1.1** *P* **160** *L* **11** # 156

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The paragraph of introduction in 119.1.1 is missing: "Both 200GBASE-R and 400GBASE-R are based on a 64B/66B code. The 64B/66B code supports transmission of data and control characters. The 64B/66B code is then transcoded to 256B/257B encoding to reduce the overhead and make room for forward error correction (FEC). The 256B/257B encoded data is then FEC encoded before being transmitted. Data distribution is introduced to support multiple lanes in the Physical Layer. Part of the distribution includes the periodic insertion of an alignment marker, which allows the receive PCS to align data from multiple lanes."

SuggestedRemedy

At least refer to 172.1.3 as an introduction.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
172.1.1 is the scope and the current text is a sufficient description of the scope of the clause. All of the information noted in the comment is provided in 172.1.3 and there is no need to duplicate it in the scope.

Cl **172** *SC* **172.1.3** *P* **161** *L* **6** # 42

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

missing "(to)" in the transcoding description in item b)

SuggestedRemedy

Change "Transcoding from 66-bit blocks to (from 257-bit blocks (25B/257B)" to "Transcoding from (to) 66-bit blocks to (from 257-bit blocks (25B/257B)"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from "Transcoding from 66-bit blocks to (from) 257-bit blocks (256B/257B)" to "Transcoding from (to) 66-bit blocks to (from) 257-bit blocks (256B/257B)"

Cl **172** *SC* **172.1.5** *P* **162** *L* **12** # 157

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"66B Block distribution": bits not bytes, rogue capital, style

SuggestedRemedy

66-bit block distribution
also 66-bit block collection

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Replace 66B by 66-bit in Fig 172-2 in two places.

Cl **172** *SC* **172.1.5** *P* **162** *L* **12** # 158

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Transcode

SuggestedRemedy

transcode - 4 times Also in this figure: Encode, Decode, Interleave, Lane

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Correct the capitalization with editorial license.

Cl **172** *SC* **172.2.1** *P* **163** *L* **19** # 179

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"distributed in a round-robin fashion into two parallel transmit functions": sort of slang. Where I come from, all robins look round.

SuggestedRemedy

Change "a round-robin fashion" to "an alternating fashion" here; in 172.2.4.1, change "a round robin fashion" to "an alternating fashion". Similarly in 172.2.5.8.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This is a new function where 64B/66B blocks are distributed between or combined from two streams or flows, so "alternating" seems more appropriate here than "round-robin". The details of the distribution are not necessary in the summary, but in the detailed functional description "round-robin" should be replaced with "alternating".

In 172.2.1 on page 163 line 19...
Change:
"The 66-bit blocks are then distributed in a round-robin fashion into two parallel transmit functions, referred to as flow 0 and flow 1."
To:
"The 66-bit blocks are then distributed between two parallel transmit functions, referred to as flow 0 and flow 1."

In 172.2.1 on page 163, line 42
Change:
"A 66-bit block collection function merges the 66-bit blocks from the two flows in a round-robin fashion into a single stream of blocks that are then 64B/66B decoded."
To:
"A 66-bit block collection function merges the 66-bit blocks from the two flows into a single stream of blocks that are then 64B/66B decoded."

In 172.2.4.1 on page 164, line 23...
Change:
"The 66-bit blocks are distributed to the two flows in a round robin fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue the round robin distribution procedure across the two flows."
To:
"The 66-bit blocks are distributed to the two flows in an alternating fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue the distribution procedure across the two flows."

In 172.2.5.8 on page 168, line 21
Change: "The block collection reverses the block distribution done in the transmitter (see

172.2.4.1) by combining the 66-bit blocks from the two flows in a round robin fashion to form a single stream of 66-bit blocks."
To: "The block collection reverses the block distribution done in the transmitter (see 172.2.4.1) by combining the 66-bit blocks from the two flows in an alternating fashion to form a single stream of 66-bit blocks."

Cl **172** *SC* **172.2.1** *P* **163** *L* **22** # 181

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The data stream is distributed to two 5140-bit blocks and then FEC encoded. The two FEC codewords are then interleaved before data is distributed to individual PCS lanes.

SuggestedRemedy

For each flow, the data stream is distributed to two 5140-bit blocks and then FEC encoded. For each flow, the two FEC codewords are then interleaved before data is distributed to individual PCS lanes.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Replace
"The data stream is distributed to two 5140-bit blocks and then FEC encoded. The two FEC codewords are then interleaved before data is distributed to individual PCS lanes."
with
"For each flow, the data stream is distributed to two 5140-bit blocks and then FEC encoded. For each flow, the two FEC codewords are then interleaved before data is distributed to individual PCS lanes."

Cl **172** *SC* **172.2.2** *P* **163** *L* **46** # 182

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"Use of blocks" - ambiguous: there are 257-bit blocks as well as FEC blocks, even if we call those "codewords". This title dates from 49.2.3 Use of blocks, before 257-bit blocks and FEC.

SuggestedRemedy

Change "blocks" to "66-bit blocks" here and at line 49.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license

Cl **172** *SC* **172.2.4.4** *P* **165** *L* **8** # 184

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Two fifths of this table is useless clutter, and it would be good to use spaces in the normal way.

SuggestedRemedy

Change
0x9A,0x4A,0x26,0xB6,0x65,0xB5,0xD9,0xD9,0xFE,0x71,0xF3,0x26,0x01,0x8E,0x0C
to
9A, 4A, 26, B6, 65, B5, D9, D9, FE, 71, F3, 26, 01, 8E, 0C
and so on. In the text, say that these are in hex.
Similarly in Table 172-2.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The format used in Table 172-1 and Table 172-2 is consistent with the format used in Table 119-2 in Clause 119. Given that we are striving for consistency between this new and previous PCS specifications, retaining a common format is helpful for comparison.

The comment does not provide sufficient justification to make the suggested change nor do the proposed changes improve the accuracy or clarity of the draft.

Cl **172** *SC* **172.2.4.4** *P* **165** *L* **8** # 183

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The curly brackets must be trying to tell the reader something, but I don't know what.

SuggestedRemedy

Delete them, or define what they mean, or change to some notation that is defined.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The curly brackets in Tables 172-1 and 172-2 are consistent with what was used in Table 119-2 in Clause 119. Given that we are striving for consistency between this new and previous PCS specifications, retaining a common format is helpful for comparison.

The comment does not provide sufficient justification to make the suggested change nor do the proposed changes improve clarity or accuracy of the draft.

Cl **172** *SC* **172.2.4.8** *P* **166** *L* **51** # 185

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

Careful, "function" has a precise meaning in PCS clauses. This can be more specific and informative.

SuggestedRemedy

Change "The functions ... are" to "the 64B/66B encoder ... is"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from
"The functions above the “64B/66B to 256B/257B transcoder” are excluded."
to
"The portion of the figure above the “64B/66B to 256B/257B transcoder” is excluded".

Cl **172** *SC* **172.2.4.8** *P* **166** *L* **51** # 10

Ran, Adee Cisco

Comment Type **ER** *Comment Status* **D** *(bucket1)*

The functions above the “64B/66B to 256B/257B transcoder” are excluded'

This is confusing - looks as if these functions are not required, but of course they are.

II had to read it several times to understand that they are excluded from the "transmit function" blocks because they are present above them.

SuggestedRemedy

Change from
The functions above the “64B/66B to 256B/257B transcoder” are excluded
to
The functions above the “64B/66B to 256B/257B transcoder” in Figure 119—11 are not included in the transmit function blocks, and instead are located outside of these blocks, as shown in Figure 172—3.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using response to comment #185.

Cl **172** *SC* **172.2.5.3** *P* **167** *L* **52** # 11

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **D** *fec degrade (bucket1)*

The FEC degrade variables in clause 172 should be stated as optional, as in their original definition in clause 119.

SuggestedRemedy

Insert "If the optional PCS FEC degraded SER ability is implemented, " at the beginning of the first list item.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
It was intended for the FEC degrade to be optional, but as written that is not obvious.
Add the following sentence at the end of 172.2.5.3:
"The FEC degrade functionality is optional."

Cl **172** *SC* **172.2.5.3** *P* **168** *L* **1** # 187

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The relation between hi_ser_0, hi_ser_1 and hi_ser appears later within a state machine variable definition, which is too obscure. More generally, I could not find where the purpose of hi_ser is introduced.

SuggestedRemedy

Add something in regular text (possibly elsewhere) that says that what hi_ser for, and that it is the OR of hi_ser_0 and hi_ser_1.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
172.2.5.3 notes the exception that each flow has a unique hi_ser generated by its FEC decoder (hi_ser_0 and hi_ser_1). The purpose of hi_ser is defined in 119.2.5.3.

Cl **172** *SC* **172.2.5.4** *P* **168** *L* **5** # 12

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **D** *(bucket1)*

"The post-FEC interleave is identical to that specified in 119.2.5.4."

But 119.2.5.4 talks specifically about two FEC codewords, and we have four.

In similar subclauses for the transmit functions, the text includes "for each flow".

Also applies to 172.2.5.6 and 172.2.5.7.

SuggestedRemedy

Insert "for each flow" after "interleave".

Make similar changes in 172.2.5.6 and 172.2.5.7, with editorial license.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **172** *SC* **172.2.5.5** *P* **168** *L* **9** # 2

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **D** *(bucket1)*

"The alignment marker removal is identical to that of the 400GBASE-R PCS in 119.2.5.5." - but there are 32 AMs, so it can't be identical.

SuggestedRemedy

Make the necessary changes to the text (add exceptions or "for each flow").

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from
"The alignment marker removal is identical to that of the 400GBASE-R PCS in 119.2.5.5"
to
"The alignment marker removal in each flow is identical to that of the 400GBASE-R PCS in 119.2.5.5"

Cl **172** *SC* **172.2.5.8** *P* **168** *L* **33** # 188

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

This says "See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules" but those subclauses are titled "119.2.3.5 Idle (/I/)" and "119.2.3.8 Ordered set (/O/)" and the content isn't there so the reader doesn't know to look there, or follow the links from there to 83 to find the deletion and insertion rules.

SuggestedRemedy

Improve the titles of those subclauses: "Idle (/I/) and idle insertion and deletion" and "Ordered set (/O/) and ordered set deletion"

Proposed Response *Response Status* **W**

PROPOSED REJECT.
119.2.3.5 and 119.2.3.8 have links to 82.2.3.6 and 82.2.3.9 respectively, which the reader can follow to access the rules for insertion/deletion. Note that this double-reference is common throughout many subclauses in Clause 172. The proposed changes do not improve the accuracy of the draft.

Cl **172** *SC* **172.2.6.2.2** *P* **169** *L* **11** # 109

Nicholl, Shawn AMD

Comment Type **TR** *Comment Status* **D** *(bucket1)*

Missing any mention of 800GBASE-R.

SuggestedRemedy

For consistency with 119.2.6.2.2, propose to replace text "with x = 0:31" with text "with x = 0:31 for 800GBASE-R."

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The proposed change is not necessary since Clause 172 is only for 800GBASE-R. CL119 specified 200GBASE-R or 400GBASE-R because the same clause includes the PCS for both 200GE and 400GE.

Cl **172** *SC* **172.2.6.2.4** *P* **170** *L* **15** # 28

Bruckman, Leon Huawei

Comment Type **T** *Comment Status* **D** *(bucket1)*

From this clause it may be implied that counters are not aggregated, but in the MDIO Table 172-4 shows (and text indicates that) they are aggregated

SuggestedRemedy

Add exception indicating that counters are the aggregate of both flows

Proposed Response *Response Status* **W**

PROPOSED REJECT.
172.2.6.2.4 is defining the counters used in the state diagrams. The definition of these counters is identical to that in 119.2.6.2.4. Therefore, these counters are not aggregated and are not the same as those defined in Table 172-4.

Cl **172** *SC* **172.2.6.3** *P* **170** *L* **21** # 3

Ran, Adee Cisco

Comment Type **E** *Comment Status* **D** *(bucket1)*

Numbers above 10 should not be spelled out.

SuggestedRemedy

change "thirty two" to "32".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **172** *SC* **172.3.1** *P* **172** *L* **35** # 61

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **D** *(bucket1)*

The variable name is amps_lock not am_lock

SuggestedRemedy

Change am_lock to amps_lock in Table 172--4

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **173** *SC* **173.1.4** *P* **177** *L* **28** # 190

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

"A ... PMA is required to support an physical instantiation of the PMA service interface": doesn't make sense, as the PMA service interface is part of the PMA. an vs. a.

SuggestedRemedy

is used to implement a ...?

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from:
"An 8:8 PMA is required to support an physical instantiation of the PMA service interface (800GAUI-8)"
to
"An 8:8 PMA is required for a physical instantiation of the PMA service interface (800GAUI-8)"

Cl **173** *SC* **173.1.4** *P* **177** *L* **28** # 24

Dudek, Mike Marvell

Comment Type **E** *Comment Status* **D** *(bucket1)*

Should be "a physical instantiation"

SuggestedRemedy

Change "an" to "a"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **173** *SC* **173.1.4** *P* **178** *L* **33** # 25

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **D** *(bucket1)*

There are more than just two addresses (1 and 8) available for the MMD. (more are shown in figure 173-2)

SuggestedRemedy

Change "1 and 8" to "1,8,9 and 10".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from:
"Manageable Device (MMD) addresses 1 and 8"
to
"Manageable Device (MMD) addresses 1,8,9,10 and 11"

Cl **173** *SC* **173.2** *P* **178** *L* **51** # 191

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

"The PMA receives": confusing and incomplete.

SuggestedRemedy

In the transmit direction, the PMA receives 32 parallel bit streams, each at the nominal signaling rate of the PCSL. In the receive direction, it delivers 32 parallel bit streams to its client.
Similarly in the next paragraph for an 8-lane interface.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from
"The PMA receives 32 parallel bit streams, each at the nominal signaling rate of the PCSL."
to
"In the transmit direction, the PMA receives 32 parallel bit streams from either the 800GBASE-R PCS or the DTE 800GXS, each at the nominal signaling rate of the PCSL. In the receive direction, the PMA sends 32 parallel bit streams to the PMA client, each at the nominal signaling rate of the PCSL."
Change from
"The PMA receives PAM4 symbols on each of its input lanes at two times the PCSL rate, each symbol formed from two bits."
to
"In the transmit direction, the PMA receives 8 parallel PAM4 symbol streams from the PMA client, each operating at a nominal signaling rate of 53.125 GBd. In the receive direction, the PMA sends 8 parallel PAM4 symbol streams to the PMA client, each at a nominal signaling rate of 53.125 GBd."

Cl **173** *SC* **173.3** *P* **179** *L* **17** # 160

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

another PMA or PMD

SuggestedRemedy

a PMD or another PMA

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from:
"another PMA or PMD"
to
"another PMA or a PMD"

Cl **173** *SC* **173.3** *P* **179** *L* **19** # 161

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"defined in 169.3" but 173.2 says "defined in 169.3.1"

SuggestedRemedy

Reconcile

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change from "169.3" to "169.3.1"

Cl **173** *SC* **173.4** *P* **180** *L* **1** # 163

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

Something strange about the page layout; these sections start to the left of the header

SuggestedRemedy

Reconcile

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **173** *SC* **173.4** *P* **180** *L* **6** # 5

Ran, Adee Cisco

Comment Type **E** *Comment Status* **D** *(bucket1)*

The concept of restricted bit multiplexing appears in this subclause for the first time. It may be helpful for readers to have a cross reference to the definition of this restriction.

SuggestedRemedy

Add the following paragraphs after each of the three bulleted lists on page 180, respectively:

"Bit multiplexing restrictions for the 32:8 PMA are specified in 173.4.2.1."

"Bit multiplexing restrictions for the 8:32 PMA are specified in 173.4.2.2."

"Bit multiplexing restrictions for the 8:8 PMA are specified in 173.4.2.3."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **173** *SC* **173.4** *P* **180** *L* **10** # 164

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

32:8 PMA Functional Block Diagram

SuggestedRemedy

32:8 PMA functional block diagram - 3 figures

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
In the titles for Figure 173-3, 173-4 and 173-5, change from:
"Functional Block Diagram"
to
"functional block diagram"

Cl **173** *SC* **173.4.1** *P* **183** *L* **44** # 165

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The next sentence says "at the service interface below the PMA"

SuggestedRemedy

So, this one should say "at its service interface"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Replace the text in 173.4.1 with the following splitting the text into two paragraphs:
"If the interface between the PMA client and the PMA is physically instantiated as 800GAUI-8, the PMA shall meet the electrical and timing specifications as specified in Annex 120F or Annex 120G as appropriate at the PMA service interface.
If the interface between the sublayer below the PMA and the PMA is physically instantiated as 800GAUI-8, the PMA shall meet the electrical and timing specifications as specified in Annex 120F or Annex 120G as appropriate at the service interface below the PMA."
[Editor's note: page was changed from 180 to 183.]

Cl **173** *SC* **173.4.2.3** *P* **185** *L* **2** # 168

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

This can be made clearer.

SuggestedRemedy

Change "lane shall be mapped together to an output lane" to "lane shall be mapped to the same output lane"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **173** *SC* **173.4.3.5** *P* **185** *L* **49** # 170

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

"group of PMAs" puzzled me. PMAs are not used in parallel.

SuggestedRemedy

Change group to series, or sequence

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The text is consistent with subclauses 120.5.3.5 and 83.5.3.6 in the base standard and is accurate as written. The proposed changes do not improve the accurary or clarity of the text.

Cl **173** *SC* **173.5** *P* **187** *L* **33** # 172

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *(bucket1)*

"Mapping of MDIO control variables to PMA control variables is shown in Table 173–2. Mapping of MDIO status variables to PMA status variables is shown in Table 173–3." But status and control go in opposite directions.

SuggestedRemedy

Mapping of PMA status variables to MDIO status variables is shown in Table 173–3. Similarly in next sentence.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The wording is consistent with similar subclauses in multiple clauses in the base standard and is accurate as written. The proposed changes do not improve the accuracy or clarity of the text.

Cl **173** *SC* **173.5** *P* **189** *L* **9** # 173

Dawe, Piers Nvidia

Comment Type **E** *Comment Status* **D** *(bucket1)*

PRBS Tx pattern testing

SuggestedRemedy

PRBS Tx pattern testing error counter

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change "PRBS Tx pattern testing" to "PRBS Tx pattern testing error counter, lane 0 to lane 7"
Change "PRBS Rx pattern testing" to "PRBS Rx pattern testing error counter, lane 0 to lane 7"

Cl **173A** *SC* **173A** *P* **226** *L* **1** # 52

Huber, Tom Nokia

Comment Type **E** *Comment Status* **D** *(bucket1)*

The text should be referencing figure 173A-3.

SuggestedRemedy

Change 173A-4 to 173A-3.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.