IEEE P802.3df D1.0 1st Task Force review comments

---

**Comment ID 1**

**Cl 45**  
**SC 45.2.4**  
**P 47**  
**L 4**  
**# 1**  

Marris, Arthur  
Cadence Design Systems

**Comment Type** T  
**Comment Status** A

"45.2.4 PHY XS registers" and "45.2.5 DTE XS registers" subsections need to be brought into the 802.3df draft and modifications made to increase the number of service interface lanes specified from 20 to 32

**SuggestedRemedy**

Update "Table 45–314—PHY XS registers" and "Table 45–339—DTE XS registers" and relevant sunclauses to address this. This will include an extra "XS alignment status 5" register at location 54, adding extra "XS lane mapping" registers above 415, adding extra "FEC symbol error counter" registers above 631, and add bit 4.801.6 for "Local degraded SER received".

**Response**  
**Response Status** C

ACCEPT.

---

**Comment ID 2**

**Cl 172**  
**SC 172.2.5.5**  
**P 168**  
**L 9**  
**# 2**  

Ran, Adee  
Cisco

**Comment Type** TR  
**Comment Status** A

"The alignment marker removal is identical to that of the 400GBASE-R PCS in 119.2.5.5." — but there are 32 AMs, so it can't be identical.

**SuggestedRemedy**

Make the necessary changes to the text (add exceptions or "for each flow").

**Response**  
**Response Status** C

ACCEPT IN PRINCIPLE.

---

**Comment ID 3**

**Cl 172**  
**SC 172.2.6.3**  
**P 170**  
**L 21**  
**# 3**  

Ran, Adee  
Cisco

**Comment Type** E  
**Comment Status** A

Numbers above 10 should not be spelled out.

**SuggestedRemedy**

change "thirty two" to "32".

**Response**  
**Response Status** C

ACCEPT.

---

**Comment ID 4**

**Cl 172**  
**SC 172.3.5**  
**P 173**  
**L 31**  
**# 4**  

Ran, Adee  
Cisco

**Comment Type** ER  
**Comment Status** A

FEC_cw_counter is defined as optional in 161.6.21. Assuming it is optional here too, it should be stated, as in clause 161.

Otherwise, state that it is not optional for this PCS (but I assume it's not the case).

Similarly for 172.3.6 FEC_codeword_error_bin_i.

**SuggestedRemedy**

Add "(optional)" to the subclause title in 172.3.5 and 172.3.6.

**Response**  
**Response Status** C

ACCEPT IN PRINCIPLE.  
Resolve using the response to comment #189.

---

**Comment ID 5**

**Cl 173**  
**SC 173.4**  
**P 180**  
**L 6**  
**# 5**  

Ran, Adee  
Cisco

**Comment Type** E  
**Comment Status** A

The concept of restricted bit multiplexing appears in this subclause for the first time. It may be helpful for readers to have a cross reference to the definition of this restriction.

**SuggestedRemedy**

Add the following paragraphs after each of the three bulleted lists on page 180, respectively:

"Bit multiplexing restrictions for the 32:8 PMA are specified in 173.4.2.1."

"Bit multiplexing restrictions for the 8:32 PMA are specified in 173.4.2.2."

"Bit multiplexing restrictions for the 8:8 PMA are specified in 173.4.2.3."

**Response**  
**Response Status** C

ACCEPT.
The restriction for the 32:8 multiplexing is intended to improve the FEC performance with correlated errors. The analysis was done with an AB/CD muxing scheme where one UI has bits from codewords A and B (flow 0) and the following UI has bits from C and D (flow 1). This way, combined with the checkerboard scheme, spreads the errors in a burst across the four codewords with equal probabilities.

The restriction as written does not preclude a different muxing, AC/BD, where one UI has bits from A and C and the following UI has bits from B and D. For example, muxing bits from lanes 0 and 16 as MSB+LSB in one UI and bits from lanes 1 and 17 as MSB+LSB in the next UI.

Since the checkerboard pattern swaps codewords A/B on each pair of lanes in flow 0, and swaps codewords C/D on each pair of lanes in flow 1, this would result in always taking the MSB from either codeword A or B, and the LSB from either codeword C or D. Since the BER for the LSB is twice that of the MSB, this would make flow 1 have an increased BER: it would get 2/3 of the errors (33% higher BER than with the AB/CD muxing).

If this muxing is performed, the result would be an increased FLR (by 1-2 orders of magnitude) compared to 400GBASE-R, just due to sub-optimal muxing - regardless of whether errors are correlated or not!

This degradation can be prevented by adding a restriction that two bits from each flow create one PAM4 symbol.

Suggested Remedy

Change the second item of the first list in 173.4.2.1 from
"The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from PMA client lanes i = 0 to 15 and two unique PCSLs from PMA client lanes i = 16 to 31" to
"The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from PMA client lanes i = 0 to 15 encoded as one PAM4 symbol, and two unique PCSLs from PMA client lanes i = 16 to 31 encoded as the subsequent PAM4 symbol (see 173.4.7)."

Make a similar change in the second item of the second list in 173.4.2.2 (which has "service interface lanes" instead of "PMA client lanes").

Also, change the second item of the list in 173.4.2.3 from
"The 4 PCSLs received on any input lane shall be mapped together to an output lane. The order of PCSLs from an input lane does not have to be maintained on the output lane." to
"The 4 PCSLs received on any input lane shall be mapped together to an output lane, maintaining the bit pairs encoded on each PAM4 symbol. Other than that, the order of PCSLs from an input lane does not have to be maintained on the output lane."
IEEE P802.3df D1.0  1st Task Force review comments

Cl 172  SC 172.2.4.4  P 164  L 45  # 8
Ran, Adee  Cisco

Comment Type: TR  Comment Status: R  alignment

"Alignment marker encoding values for flow 1 are specified in Table 172–2 and the variable x in 119.2.4.4.2 takes the values of PCS lane number minus 16"

In 119.2.4.4.2, x is used as part of the variable am_x. We have 32 distinct alignment markers, for lanes 0 through 31, so assigning x to "lane number minus 16" would result in am_0 through am_15 assigned twice, and am_16 through am_31 not assigned at all.

Instead, we should specify that for flow 1, AM are constructed per 119.2.4.4.2 but with x taking values from 16 to 31, and the variable j used in the mapping procedure takes values from 8 to 16 (instead of 0 to 7).

This difference may be listed as another exception, but it seems that it makes it worthwhile to have a new subclause for creating the 32 AMs.

SuggestedRemedy
Replace the reference to 119.2.4.4.2 with a full specification of AM creation and insertion, based on the content (text and equations) of 119.2.4.4.2, but with AMs for lanes 16 to 31 constructed as in the comment.

Response: REJECT.

Each Flow is a unique "instance" of the 119.4.4.2 so the fact that there are 2 copies of variable "am_#", one in Flow0 and another in Flow1 that have different values is how it's intended to be specified.

Comment Status: D
Response Status: C

Cl 172  SC 172.2.4.4  P 164  L 51  # 9
Ran, Adee  Cisco

Comment Type: TR  Comment Status: A  AM sync

In the baseline proposal https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf, slide 10, it is written that "AM insertion is aligned across the two flows".

I do not see that requirement in clause 172. The text in 172.2.4.4 does not preclude inserting AM blocks independently in each flow.

SuggestedRemedy
If the subclause specifying AM creation is updated to include full text, this requirement can be included in it (a similar statement exists in 119.2.4.4.2 for the 16 lanes).

Otherwise, add this requirement as another exception, with editorial license.

Response: ACCEPT IN PRINCIPLE.

Resolve using the response to comment #90.

Comment Status: A
Response Status: C

Cl 172  SC 172.2.4.8  P 166  L 51  # 10
Ran, Adee  Cisco

Comment Type: ER  Comment Status: A  (bucket2)

The functions above the "64B/66B to 256B/257B transcoder" are excluded

This is confusing - looks as if these functions are not required, but of course they are.

I had to read it several times to understand that they are excluded from the "transmit function" blocks because they are present above them.

SuggestedRemedy
Change from
The functions above the "64B/66B to 256B/257B transcoder" are excluded to
The functions above the "64B/66B to 256B/257B transcoder" in Figure 119—11 are not included in the transmit function blocks, and instead are located outside of these blocks, as shown in Figure 172—3.

Response: ACCEPT IN PRINCIPLE.

Resolve using response to comment #185.
<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>SuggestedRemedy</th>
<th>Response</th>
<th>Response Status</th>
<th>Comment ID</th>
<th>Page 4 of 47</th>
</tr>
</thead>
<tbody>
<tr>
<td>172</td>
<td>172.2.5.3</td>
<td>167</td>
<td>52</td>
<td>TR</td>
<td>A</td>
<td>The FEC degrade variables in clause 172 should be stated as optional, as in their original definition in clause 119.</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Insert &quot;If the optional PCS FEC degraded SER ability is implemented, &quot; at the beginning of the first list item.</td>
<td>Ran, Adee</td>
<td>Cisco</td>
<td></td>
<td></td>
</tr>
<tr>
<td>172</td>
<td>172.2.5.4</td>
<td>168</td>
<td>5</td>
<td>TR</td>
<td>A</td>
<td>&quot;The post-FEC interleave is identical to that specified in 119.2.5.4.&quot; But 119.2.5.4 talks specifically about two FEC codewords, and we have four. In similar subclauses for the transmit functions, the text includes &quot;for each flow&quot;. Also applies to 172.2.5.6 and 172.2.5.7.</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Insert &quot;for each flow&quot; after &quot;interleave&quot;. Make similar changes in 172.2.5.6 and 172.2.5.7, with editorial license.</td>
<td>Ran, Adee</td>
<td>Cisco</td>
<td></td>
<td></td>
</tr>
<tr>
<td>124</td>
<td>124.8.5a</td>
<td>76</td>
<td>16</td>
<td>T</td>
<td>A</td>
<td>800BASE-DR4 is not part of this specification</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Change to 800BASE-DR8. Also on line 25 and page 77 line 29</td>
<td>Dudek, Mike</td>
<td>Marvell</td>
<td></td>
<td></td>
</tr>
<tr>
<td>124</td>
<td>124.11.3.1</td>
<td>80</td>
<td>34</td>
<td>T</td>
<td>A</td>
<td>The optical lane assignments are wrong in figure 124-6.</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Change them to match Figure 124-6 in the base document.</td>
<td>Dudek, Mike</td>
<td>Marvell</td>
<td></td>
<td></td>
</tr>
<tr>
<td>124</td>
<td>124.11.3.3</td>
<td>81</td>
<td>29</td>
<td>E</td>
<td>A</td>
<td>Should be plural</td>
<td>Should be plural</td>
<td>C</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Change &quot;800BASE-DR8 and 800BASE-DR8-2 have&quot; to &quot;800BASE-DR8 and 800BASE-DR8-2 has&quot;</td>
<td>Dudek, Mike</td>
<td>Marvell</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Comment Type: T | Comment Status: A | (bucket1)

The base standard and 802.3db all list the "with reach up to at least xxx." to differentiate between the various Phy’s. This draft does not.

SuggestedRemedy
Add the reach information to the new Phys.

Response | Response Status: C
ACCEPT IN PRINCIPLE.

- change 400GBASE-DR4 description to:
  "400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD with reach up to at least 500 m as specified in Clause 124"

- change 400GBASE-DR4-2 description to:
  "400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 124"

- change 800GBASE-DR4 description to:
  "800GBASE-R PCS/PMA over 8-lane single-mode fiber PMD with reach up to at least 500 m as specified in Clause 124"

- change 800GBASE-DR4-2 description to:
  "800GBASE-R PCS/PMA over 8-lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 124"

- change 800GBASE-SR8 description to:
  "800GBASE-R PCS/PMA over 8-lane multimode fiber PMD with reach up to at least 100 m as specified in Clause 167"

- change 800GBASE-VR8 description to:
  "800GBASE-R PCS/PMA over 8-lane multimode fiber PMD with reach up to at least 50 m as specified in Clause 167"

Implement with editorial license.

Comment Type: E | Comment Status: A | (bucket1)

In table 45-12 "and" is used in the list for BR but it has been deleted for KR and CR. The table should be consistent for all rows.

SuggestedRemedy
Add the "and" before 800.

Response | Response Status: C
ACCEPT.

Comment Type: T | Comment Status: A | (bucket2)

This is listing register 1.72 but 45.2.1.60b is listing the abilities in Register 1.73

SuggestedRemedy
Change to register 1.72. Also on line 39

Response | Response Status: C
ACCEPT IN PRINCIPLE.

Resolve using the response to comment #44.

Comment Type: T | Comment Status: A | (bucket1)

The mapping of lanes 4-7 is not provided.

SuggestedRemedy
Add the mapping for those lanes. Also in 45.2.1.163 on line 50, 45.2.1.165 and 45.2.1.167

Response | Response Status: C
ACCEPT IN PRINCIPLE.

Resolve using the response to comment #45
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Response</th>
<th>Response Status</th>
<th>SuggestedRemedy</th>
<th>Comment Text</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>162</td>
<td>162.11</td>
<td>94</td>
<td>51</td>
<td>20</td>
<td>E</td>
<td>A</td>
<td></td>
<td>C</td>
<td>ACCEPT.</td>
<td>There are 4 cable assembly types</td>
</tr>
<tr>
<td>21</td>
<td>163</td>
<td>163.3</td>
<td>100</td>
<td>28</td>
<td>21</td>
<td>T</td>
<td>A</td>
<td></td>
<td>C</td>
<td>ACCEPT.</td>
<td>Should be 800GASE-KR8 not KR4</td>
</tr>
<tr>
<td>22</td>
<td>163</td>
<td>163.3</td>
<td>100</td>
<td>29</td>
<td>22</td>
<td>T</td>
<td>A</td>
<td></td>
<td>C</td>
<td>ACCEPT.</td>
<td>should be 800GBASE-CR8 not KR8</td>
</tr>
<tr>
<td>23</td>
<td>167</td>
<td>167.2</td>
<td>110</td>
<td>23</td>
<td>23</td>
<td>E</td>
<td>A</td>
<td></td>
<td>C</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>173</td>
<td>173.1.4</td>
<td>177</td>
<td>28</td>
<td>24</td>
<td>E</td>
<td>A</td>
<td></td>
<td>C</td>
<td>ACCEPT.</td>
<td>Should be &quot;a physical instantiation&quot;</td>
</tr>
<tr>
<td>25</td>
<td>173</td>
<td>173.1.4</td>
<td>178</td>
<td>33</td>
<td>25</td>
<td>T</td>
<td>A</td>
<td></td>
<td>C</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>124</td>
<td>124.11.3.1.1</td>
<td>80</td>
<td>32</td>
<td>26</td>
<td>E</td>
<td>A</td>
<td></td>
<td>C</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td></td>
</tr>
</tbody>
</table>

**Comment ID** 26  
**Page 6 of 47**  
**2022-12-08 1:09:00 PM**  
**TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general**  
**COMMENT STATUS: D/dispatched A/accepted R/rejected**  
**RESPONSE STATUS: O/open W/written C/closed Z/withdrawn**  
**SORT ORDER: Comment ID**
IEEE P802.3df D1.0 1st Task Force review comments

Cl  172  SC  172.2.4.9  P 167  L 25  #  27  
Bruckman, Leon  Huawei
Comment Type  T  Comment Status  A  test pattern (CC)
I assume test pattern shall be applied to both flows together
SuggestedRemedy
It may be beneficial to note that the test function when activated affects both flows
Response  Response Status  C
ACCEPT IN PRINCIPLE.
The scrambled idle pattern for 800GBASE-R is different from that for 400GBASE-R and 200GBASE-R.
Implement with editorial license the changes on slide 18 of the following presentation:

Cl  172  SC  172.2.6.2.4  P 170  L 15  #  28  
Bruckman, Leon  Huawei
Comment Type  T  Comment Status  R  (bucket1)
From this clause it may be implied that counters are not aggregated, but in the MDIO Table 172-4 shows (and text indicates that) they are aggregated
SuggestedRemedy
Add exception indicating that counters are the aggregate of both flows
Response  Response Status  C
REJECT.
172.2.6.2.4 is defining the counters used in the state diagrams. The definition of these counters is identical to that in 119.2.6.2.4. Therefore, these counters are not aggregated and are not the same as those defined in Table 172-4.

Cl  173  SC  173.2  P 179  L 10  #  29  
Bruckman, Leon  Huawei
Comment Type  T  Comment Status  A  PMA SI
"In the case where the sublayer below the PMA is a PHY 800GXS the PMA does not receive a PHY_XS:IS_SIGNAL_indication as an input to the SIL". Figure 173-4 that describes this interface does include the PHY_XS:IS_SIGNAL_indication
SuggestedRemedy
Update Figure 173-4 according to text
Response  Response Status  C
ACCEPT IN PRINCIPLE.
Resolve using the response to comment #196.

Cl  45  SC  45.2.1.165  P 42  L 8  #  50  
Huber, Tom  Nokia
Comment Type  T  Comment Status  A  (bucket2)
While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.
SuggestedRemedy
Change "Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323." to "Lanes 0-7 map to registers 1.1320 to 1.1327, respectively."
Response  Response Status  C
ACCEPT IN PRINCIPLE.
The word "to" should be used instead of "."
Change text to: "Lanes 0 to 7 map to registers 1.1320 to 1.1327, respectively."

Cl  45  SC  45.2.1.167  P 42  L 23  #  51  
Huber, Tom  Nokia
Comment Type  T  Comment Status  A  (bucket2)
While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.
SuggestedRemedy
Change "Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423." to "Lanes 0-7 map to registers 1.1420 to 1.1427, respectively."
Response  Response Status  C
ACCEPT IN PRINCIPLE.
The word "to" should be used instead of "."
Change text to: "Lanes 0 to 7 map to registers 1.1420 to 1.1427, respectively."
While the mapping of registers to what they control is obvious, it would be better to spell it out a bit more completely to maintain similar structure to the other clauses that are specifying registers per-lane.

**Suggested Remedy**

Change "Register 1.1450 controls the PMD training pattern for PMD lane 0; register 1.1451 controls the PMD training pattern for PMD lane 1; etc." to "Registers 1.1450 to 1.1457 control the PMD training pattern for PMD lanes 0-7, respectively."

**Response**

ACCEPT IN PRINCIPLE.

The word "to" should be used instead of "-".

Change text to: "Registers 1.1450 to 1.1457 control the PMD training pattern for PMD lanes 0 to 7, respectively."

---

The text "and 136.8.11.1.3" is in 802.3-2022, so it should not be identified as a change.

**Suggested Remedy**

Remove the underlining from this text.

**Response**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #122.

---

Subclauses 45.2.3.24-26 all exist in 802.3-2022, so they should not be indicated as changes in the table.

**Suggested Remedy**

Remove the underlining from 45.2.3.24, 45.2.3.25, 45.2.3.26.

**Response**

REJECT.

Although these clauses are in the base standard, there are no references to them in Table 45-233. Therefore it is appropriate to add them to the table with underlining.
IEEE P802.3df D1.0 1st Task Force review comments

**Comment ID 36**

**Cl 45 SC 45.2.3 P 43 L 50 # 36**

Huber, Tom Nokia

**Comment Type E**  **Comment Status R**  (bucket1)

Subclause 45.2.3.50 exists in 802.3-2022, so it should not be indicated as a change in the table.

**Suggested Remedy**

Remove the underlining from 45.2.3.50

**Response**  **Response Status C**

REJECT.

Although this subclause is in the base standard there is no reference to it in the table. Therefore it is appropriate to add it to Table 45-233 with underlining.

**Comment ID 37**

**Cl 124 SC 124.1 P 59 L 24 # 37**

Huber, Tom Nokia

**Comment Type T**  **Comment Status A**  (bucket1)

Table 124-1 was modified by 802.3ck-2022

**Suggested Remedy**

Change the editing instruction to add "(as modified by IEEE 802.3ck-2022)", and insert the rows for Annexes 120F and 120G into the table.

**Response**  **Response Status C**

ACCEPT IN PRINCIPLE.

Implement proposed remedy with editorial license

**Comment ID 38**

**Cl 169 SC 169.1.2 P 127 L 36 # 39**

Huber, Tom Nokia

**Comment Type E**  **Comment Status A**  (bucket1)

Elsewhere in the clause (e.g. in 162.4), 800GAUI-n is used, which seems desirable since it will be more future-proof toward the 200G/lane AUI that will be added.

**Suggested Remedy**

Change 800GAUI-8 to 800GAUI-n.

**Response**  **Response Status C**

ACCEPT.

**Comment ID 39**

**Cl 169 SC 169.1.2 P 128 L 4 # 40**

Huber, Tom Nokia

**Comment Type E**  **Comment Status A**  (bucket1)

The dashed lines between the OSI layers and the Ethernet layers are not in the correct locations.

**Suggested Remedy**

Align the upper two dashed lines with the boundaries of the data link layer in the OSI model.

**Response**  **Response Status C**

ACCEPT.

**Comment ID 41**

**Cl 169 SC 169.1.2 P 128 L 4 # 41**

Huber, Tom Nokia

**Comment Type E**  **Comment Status A**  (bucket1)

Singular/plural disagreement in item a)

**Suggested Remedy**

Change "when implemented as logical interconnection points" to "when implemented as a logical interconnection point"

**Response**  **Response Status C**

ACCEPT.
IEEE P802.3df D1.0 1st Task Force review comments

**Comment ID: 42**

Huber, Tom  
Nokia

**Comment Type:** E  
**Comment Status:** A (bucket1)

- missing "(to)" in the transcoding description in item b)

**SuggestedRemedy**
- Change "Transcoding from 66-bit blocks to (from 257-bit blocks (25B/257B))" to "Transcoding from (to) 66-bit blocks to (from 257-bit blocks (25B/257B))"

**Response**  
**Response Status:** C

**ACCEPT IN PRINCIPLE.**
- Change from "Transcoding from 66-bit blocks to (from) 257-bit blocks (256B/257B)" to "Transcoding from (to) 66-bit blocks to (from) 257-bit blocks (256B/257B)"

**Comment ID: 43**

Huber, Tom  
Nokia

**Comment Type:** E  
**Comment Status:** A (bucket1)

- Since the table includes 400Zr as existing text, the editing instruction should note that the text shown is as modified by 802.3cw.

**SuggestedRemedy**
- Add "(as modified by IEEE 802.3cw-202x)" after "Change Table 45-7"

**Response**  
**Response Status:** C

**ACCEPT.**

**Comment ID: 44**

Huber, Tom  
Nokia

**Comment Type:** T  
**Comment Status:** A (bucket2)

- While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

**SuggestedRemedy**
- Change "Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123."
- to "Lanes 0-7 map to registers 1.1120 to 1.1127, respectively."

**Response**  
**Response Status:** C

**ACCEPT IN PRINCIPLE.**
- The word "to" should be used instead of "-".
- Change text to: "Lanes 0 to 7 map to registers 1.1120 to 1.1127, respectively."

**Comment ID: 45**

Huber, Tom  
Nokia

**Comment Type:** T  
**Comment Status:** A (bucket2)

- While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

**SuggestedRemedy**
- Change "Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223."
- to "Lanes 0-7 map to registers 1.1220 to 1.1227, respectively."

**Response**  
**Response Status:** C

**ACCEPT IN PRINCIPLE.**
- The word "to" should be used instead of "-".
- Change text to: "Lanes 0 to 7 map to registers 1.1220 to 1.1227, respectively."
There is some repetition between the paragraph about the PCS Synchronization process and the paragraph about the PCS Receive process in terms of aligning, reordering, and deskewing. Per the state diagrams, the PCS synchronization process ensures that all the lanes are aligned and deskewed, and the receive process deals with decoding the 66b characters.

Suggested Remedy:
Add a sentence to the end of the penultimate paragraph: "When all 32 lanes are aligned and deskewed, and reordered, the align_status flag is set to indicate that the PCS has obtained alignment."
Revise the first two sentences of the final paragraph as follows: "The PCS Receive process separates the reordered PCS lanes into two sets of 16 PCs lanes..."

Response
Implement with editorial license the changes on slide 33 of the following presentation:

There is consensus to adopt the proposal on slide 7 in the reviewed presentation.

The inserted text is more complex than is necessary.
Suggested Remedy:
Change "800GAUI-8 C2C or for 100GAUI-1, 200GAUI-2, or 400GAUI-4 C2C with" to "100GAUI-1, 200GAUI-2, 400GAUI-4, or 800GAUI-8 C2C"

Response
The text intentionally distinguishes between 800GAUI-8, for which the range is always +/- 50 PPM, and the other interfaces, for which it is conditional. Therefore, the suggested remedy would not be correct. However, the text can be clarified.
In Table 120F-1 change the first sentence in footnote a to the following:
"For 100GAUI-1, 200GAUI-2, or 400GAUI-4 C2C with a PMA in the same package as the PCS sublayer or for any 800GAUI-8 C2C."
In Table 120G-1 change the first sentence in footnote a to the following:
"For 100GAUI-1, 200GAUI-2, or 400GAUI-4 C2M with a PMA in the same package as the PCS sublayer or for any 800GAUI-8 C2M."

The following presentation was reviewed by the task force:

There is consensus to adopt the proposal on slide 7 in the reviewed presentation.

Implement with editorial license the proposal on slide 7 of the reviewed presentation.
Comment ID  51
Cl  162B  SC  162B  P 215  L 11  # [51]
Huber, Tom  Nokia

Comment Type  E  Comment Status  A
The title is missing 'C2M' for 800G

SuggestedRemedy
Add 'C2M' to the end of the title

Response
Response Status  C
ACCEPT.

Comment ID  52
Cl  173A  SC  173A  P 226  L 1  # [52]
Huber, Tom  Nokia

Comment Type  E  Comment Status  A
The text should be referencing figure 173A-5.

SuggestedRemedy

Response
Response Status  C
ACCEPT.

Comment ID  53
Cl  45  SC  45.2.4.4  P 46  L 54  # [53]
Slavick, Jeff  Broadcom

Comment Type  T  Comment Status  A
Need to add 800G capability register to PHY XS

SuggestedRemedy
Assign a bit in register 4.4 for 800G capable and create a description the same as the
400G bit replacing 400G with 800G

Response
Response Status  C
ACCEPT.

Comment ID  54
Cl  45  SC  45.2.5.4  P 46  L 54  # [54]
Slavick, Jeff  Broadcom

Comment Type  T  Comment Status  A
Need to add 800G capability register to DTE XS

SuggestedRemedy
Assign a bit in register 5.4 for 800G capable and create a description the same as the
400G bit replacing 400G with 800G

Response
Response Status  C
ACCEPT.

Comment ID  55
Cl  45  SC  45.2.5.15  P 46  L 54  # [55]
Slavick, Jeff  Broadcom

Comment Type  T  Comment Status  A
DTE XS AM lock registers need to be updated with 800G references and expanded to 32
AM lanes

SuggestedRemedy
Update (see 119.2.6.2.2) to (see 119.2.6.2.2 and 172.2.6.2.2) in 45.2.4.15.* and 45.2.4.16.*
Add the extra 16 lanes of amps_lock as well as was done for the PCS registers.

Response
Response Status  C
ACCEPT.

Comment ID  56
Cl  45  SC  45.2.5.17  P 46  L 54  # [56]
Slavick, Jeff  Broadcom

Comment Type  T  Comment Status  A
DTE XS lane mapping registers need to update with 800G references and expanded to 32
lanes

SuggestedRemedy
Bring in and update 45.2.5.17 and 45.2.5.18 adding references to Clause 171 and adding
16 more registers

Response
Response Status  C
ACCEPT.
Comment ID: 62

**Comment Type:** T

**Comment Status:** A

**Slavick, Jeff**

**Broadcom**

**Comment:**

800GAUIN is not listed in the list of acronyms for Figure 169-3

**Suggested Remedy:**

Add 800GAUIN to list of acronyms in Figure 169-3

**Response:**

ACCEPT.

---

Comment ID: 61

**Comment Type:** T

**Comment Status:** A

**Slavick, Jeff**

**Broadcom**

**Comment:**

The variable name is am_lock not amps_lock

**Suggested Remedy:**

Change am_lock to amps_lock in Table 172-4

**Response:**

ACCEPT.

---

Comment ID: 60

**Comment Type:** T

**Comment Status:** A

**Slavick, Jeff**

**Broadcom**

**Comment:**

There is no am_lock variable in Clause 172

**Suggested Remedy:**

Change am_lock to amps_lock in Table 171-3 and 171-5

**Response:**

ACCEPT.
### IEEE P802.3df D1.0 1st Task Force review comments

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
<th>Slavick, Jeff</th>
<th>Broadcom</th>
</tr>
</thead>
<tbody>
<tr>
<td>172</td>
<td>172.3.5</td>
<td>173</td>
<td>32</td>
<td>83</td>
<td>Comment Type: T, Comment Status: A, fec counters</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>45.2.3.60.1</td>
<td>46</td>
<td>54</td>
<td>65</td>
<td>Slavick, Jeff</td>
<td>Broadcom</td>
</tr>
<tr>
<td>63</td>
<td>Cl 172 SC 172.3.5 P 173 L 32 # 83</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>Cl 45 SC 45.2.3.60.1 P 46 L 54 # 65</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment Type: T, Comment Status: A, fec counters**

**The CW counter is a RS-FEC sublayer counter in MDIO space, not a PCS counter.**

**SuggestedRemedy**

- Copy of the definition of 45.2.1.120a (802.3ck) into a set of PCS registers (45.2.3.###) and replace the Clause 161 references with 172.
- Replace the text in 172.2.3.5 with the same text from 161.6.21 updating the MDIO register references to point to the newly created MDIO registers.
- Update Table 172-4 to point to the newly created MDIO registers.

**Response**

- Response Status: C

**ACCEPT IN PRINCIPLE.**

Implement the suggested remedy with editorial license.

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
<th>Slavick, Jeff</th>
<th>Broadcom</th>
</tr>
</thead>
<tbody>
<tr>
<td>172</td>
<td>172.3.6</td>
<td>173</td>
<td>32</td>
<td>84</td>
<td>Comment Type: T, Comment Status: A, fec counters</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>45.2.3.60.1</td>
<td>46</td>
<td>54</td>
<td>65</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment Type: T, Comment Status: A, fec counters**

**The FEC_codeword_error_bin_i is a RS-FEC sublayer set of counters in MDIO space, not PCS counters.**

**SuggestedRemedy**

- Copy of the definition of 45.2.1.131a (802.3ck) into a set of PCS registers (45.2.3.###) and replace the Clause 161 references with 172.
- Replace the text in 172.2.3.6 with the same text from 161.6.17 updating the MDIO register references to point to the newly created MDIO registers.
- Update Table 172-4 to point to the newly created MDIO registers.

**Response**

- Response Status: C

**ACCEPT IN PRINCIPLE.**

Implement suggested remedy with editorial license.

**Various clause 45 registers need to some Clause 172 references added.**

**SuggestedRemedy**

- A reference to Clause 172 needs to be added to 45.2.3.49
- A reference to 172.2.5.3 needs to be added to:
  - 45.2.3.60.1
  - 45.2.3.60.2
  - 45.2.3.61.4
  - 45.2.3.61.6
  - 45.2.3.64
  - 45.2.3.65
  - 45.2.3.66
  - 45.2.4.21.1
  - 45.2.4.21.2
  - 45.2.4.22.2
  - 45.2.4.22.3
  - 45.2.4.22.4
  - 45.2.4.22.5
  - 45.2.4.25
  - 45.2.4.26
  - 45.2.4.27
  - 45.2.5.21.1
  - 45.2.5.21.2
  - 45.2.5.22.2
  - 45.2.5.22.3
  - 45.2.5.22.4
  - 45.2.5.22.5
  - 45.2.5.25
  - 45.2.5.26
  - 45.2.5.27
- A reference to 172.2.6.2.2 needs to be added to:
  - 45.2.3.61.1
  - 45.2.3.61.2
  - 45.2.3.61.3
  - 45.2.3.61.5
  - 45.2.4.22.1
  - 45.2.5.22.1
- A reference to 172.3.2 needs to be added to 45.2.3.62, 45.2.4.23 and 45.2.5.23
- A reference to 172.3.3 needs to be added to 45.2.3.63, 45.2.4.24 and 45.2.5.24

---

**TYPE:** TR/technical required, ER/editorial required, GR/general required, T/technical, E/editorial, G/general

**COMMENT STATUS:** D/dispatched, A/accepted, R/rejected

**RESPONSE STATUS:** O/open, W/written, C/closed, Z/withdrawn

**SORT ORDER:** Comment ID

**Comment ID 65**

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2022-12-08 1:09:00 PM
A reference to 172.3.4 needs to be added to 45.2.3.58

**Response**

**Response Status** C

**ACCEPT.**

---

**Comment ID** 66

**Cl** 45 **SC** 45.2.4.15 **P** 46 **L** 54  
**Suggested Remedy**

PHY XS AM lock registers need to be updated with 800G references and expanded to 32 AM lanes

**Response**

**Response Status** C

**ACCEPT.**

---

**Comment ID** 67

**Cl** 45 **SC** 45.2.4.17 **P** 46 **L** 54  
**Suggested Remedy**

PHY XS lane mapping registers need to update with 800G references and expanded to 32 lanes

**Response**

**Response Status** C

**ACCEPT.**

---

**Comment ID** 68

**Cl** 45 **SC** 45.2.1.161 **P** 41 **L** 34  
**Suggested Remedy**

The paragraph provides mapping of registers 1.1120-1.1123 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

**Response**

**Response Status** C

**ACCEPT IN PRINCIPLE.**

Resolve using the response to comment #45

---

**Comment ID** 70

**Cl** 45 **SC** 45.1.2.163 **P** 41 **L** 50  
**Suggested Remedy**

The paragraph provides mapping of registers 1.1220-1.1223 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

**Response**

**Response Status** C

**ACCEPT IN PRINCIPLE.**

Resolve using the response to comment #46
IEEE P802.3df D1.0 1st Task Force review comments

CI/ 45  SC 45.1.2.165  P 42  L 8  # [71]
Lusted, Kent  Intel Corporation

Comment Type TR Comment Status A (bucket1)
The paragraph provides mapping of registers 1.1320-1.1323 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

SuggestedRemedy
change:
"Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323."
to:
"Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, lane 3 maps to register 1.1323, lane 4 maps to register 1.1324, lane 5 maps to register 1.1325, lane 6 maps to register 1.1326, and lane maps to register 1.1327."

Response Response Status C
ACCEPT IN PRINCIPLE.
Resolve using the response to comment #30

CI/ 162  SC 162.7  P 89  L 24  # [74]
Lusted, Kent  Intel Corporation

Comment Type E Comment Status A (bucket1)
With the addition of new sub-note "a", the rest of the sub-notes from the table 162-6 in P802.3ck are re-indexed. (i.e. 'a' becomes 'b', 'b' becomes 'c'). However, the new notes 'b' and 'c' do not have the relevant strikeout text

SuggestedRemedy
Correct as necessary

Response Response Status C
ACCEPT IN PRINCIPLE.
Resolve using the response to comment #74.
<table>
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</thead>
<tbody>
<tr>
<td><strong>Cl 162 SC 162.13</strong></td>
<td><strong>Cl 162 SC 162.13</strong></td>
</tr>
<tr>
<td><strong>P 97</strong></td>
<td><strong>P 105</strong></td>
</tr>
<tr>
<td><strong>L 21</strong></td>
<td><strong>L 4</strong></td>
</tr>
<tr>
<td><strong># 76</strong></td>
<td><strong># 79</strong></td>
</tr>
</tbody>
</table>

**Comment Type:** TR

**Comment Status:** A

Row entry for PMA800 has incorrect status value of "CR4:M". It should be "CR8:M"

**Suggested Remedy:**
Change to "CR8:M" **ACCEPT.**

<table>
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<tr>
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<tbody>
<tr>
<td><strong>Cl 162 SC 162.13</strong></td>
<td><strong>Cl 162 SC 162.13</strong></td>
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<tr>
<td><strong>P 96</strong></td>
<td><strong>P 105</strong></td>
</tr>
<tr>
<td><strong>L 4</strong></td>
<td><strong>L 4</strong></td>
</tr>
<tr>
<td><strong># 77</strong></td>
<td><strong># 79</strong></td>
</tr>
</tbody>
</table>

**Comment Type:** TR

In P802.3ck, Clause 162.13 is the environmental specifications and Clause 162.14 is the PICS. The 162.13 sub clause is missing from the draft and creates an issue where the PICs became sub clause 162.13.

**Suggested Remedy:**
Fix editing instruction on p96, line 1 to reference the heading of 162.14
Correct the sub clause number for the PICS to 162.14 in the title and the sub clauses.
Update all editing instructions as required.
Implement with editorial license

**Proposed Response**

**Response**

**Response Status:** C

**Withdrawn**

**This comment was WITHDRAWN by the commenter.**

<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Page 17 of 47</th>
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</thead>
<tbody>
<tr>
<td><strong>Cl 169 SC 169.5</strong></td>
<td><strong>Cl 169 SC 169.5</strong></td>
</tr>
<tr>
<td><strong>P 136</strong></td>
<td><strong>P 136</strong></td>
</tr>
<tr>
<td><strong>L 10</strong></td>
<td><strong>L 10</strong></td>
</tr>
<tr>
<td><strong># 80</strong></td>
<td><strong># 80</strong></td>
</tr>
</tbody>
</table>

**Comment Type:** ER

Figure 169-4 variable "q" should be italics like 'n' and 'p'. Both in middle and bottom of figure

**Suggested Remedy**
consider changing 'q' to italics types

**Response**

**Response Status:** C

**ACCEPT IN PRINCIPLE.**

The text states that the KR* service interfaces are identical to those of CR*. The addition of "KR8" was erroneous.
Resolve using the response to comment #18.
### IEEE P802.3df D1.0 1st Task Force review comments

<table>
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<tr>
<th>CI 120F</th>
<th>SC 120F.1</th>
<th>P 198</th>
<th>L 48</th>
<th># 81</th>
<th>Lusted, Kent Intel Corporation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comment Type</td>
<td>T</td>
<td>Comment Status</td>
<td>A</td>
<td>(bucket1)</td>
<td></td>
</tr>
<tr>
<td>Paragraph omits the eight-lane 800GAUI-8.</td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>Suggested Remedy</strong></td>
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<tr>
<td>Replace the second sentence in the 5th paragraph with &quot;Each 100GAUI-1, 200GAUI-2, 400GAUI-4, or 800GAUI-8 C2C data path contains one, two, four, or eight, respectively, differential lanes, which are AC coupled.&quot;</td>
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<td></td>
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<tr>
<td><strong>Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACCEPT.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CI 120F</th>
<th>SC 120F.1</th>
<th>P 198</th>
<th>L 52</th>
<th># 82</th>
<th>Lusted, Kent Intel Corporation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comment Type</td>
<td>TR</td>
<td>Comment Status</td>
<td>A</td>
<td>(bucket1)</td>
<td></td>
</tr>
<tr>
<td>The mapping of the differential voltage level to the PAM4 symbol is missing in Annex 120F. It is also not present in Annex 120F in IEEE Std. 802.3ck-202x. The mapping of the differential voltage level to the PAM4 symbol level is important for interoperability.</td>
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<tr>
<td><strong>Suggested Remedy</strong></td>
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</tr>
<tr>
<td>Add a new sentence to the 5th paragraph: &quot;The highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero.&quot;</td>
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<tr>
<td><strong>Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACCEPT IN PRINCIPLE.</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>In the sixth paragraph, change &quot;The C2C transmitter and the receiver use PAM4 signaling&quot; To: &quot;The C2C transmitter and receiver use PAM4 signaling. The highest differential level corresponds to the tx_symbol or rx_symbol value three, and the lowest differential level corresponds to the tx_symbol or rx_symbol value zero.&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CI 162</th>
<th>SC 162.8.1</th>
<th>P 91</th>
<th>L 22</th>
<th># 84</th>
<th>Opsasnick, Eugene Broadcom</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comment Type</td>
<td>ER</td>
<td>Comment Status</td>
<td>A</td>
<td>(bucket1)</td>
<td></td>
</tr>
<tr>
<td>At top-middle of Figure 162-2, the added text reads &quot;800BASE-CR4 8x&quot;, but &quot;-CR4&quot; should probably be &quot;-CR8&quot;.</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td><strong>Suggested Remedy</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Replace &quot;800BASE-CR4 8x&quot; with &quot;800BASE-CR8 8x&quot;.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACCEPT.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CI 163</th>
<th>SC 163.3</th>
<th>P 100</th>
<th>L 27</th>
<th># 85</th>
<th>Opsasnick, Eugene Broadcom</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comment Type</td>
<td>ER</td>
<td>Comment Status</td>
<td>A</td>
<td>(bucket1)</td>
<td></td>
</tr>
<tr>
<td>At end of first line of paragraph, 800BASE-KR4 (wraps to line 28), &quot;-KR4&quot; should probably be &quot;-KR8&quot;.</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>Suggested Remedy</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Replace &quot;800BASE-KR4 8x&quot; with &quot;800BASE-KR8 8x&quot; and use non-breaking hyphen.</td>
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<td><strong>Response</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
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<tr>
<td>ACCEPT.</td>
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</tr>
</tbody>
</table>

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**Sort Order:** Comment ID

**Comment ID:** 85

**Response Status:** C

**Comment Status:** A

**Type:** T/technical E/editorial G/general

**Comment Status:** D/dispatched A/accepted R/rejected

**Response Status:** O/open W-written C/closed Z/withdrawn

**Page 18 of 47**

**Date:** 2022-12-08 1:09:00 PM
IEEE P802.3df D1.0 1st Task Force review comments

**Comment ID: 86**

**Cl 172 SC 172.2.6.3 P 170 L 19 # 86**

Opsasnick, Eugene

**Comment Type:** TR

**Comment Status:** A

State diagrams are identical to those specified in 119.2.6.3 ...

State diagrams in Figure 119-14 "Transmit state diagram" and Figure 119-15 "Receive state diagram" can cause logic implementation issues at high rate port speeds (i.e. 800GbE) as shown in opasnick_3df_01a_221005.pdf. A "stateless" encode/decode option to these state diagrams could be allowed since the state diagrams were originally designed for non-FEC interfaces. Interfaces with required FEC should have sufficient protection to allow for the stateless coding. An updated presentation showing the error analysis will be forthcoming.

**Suggested Remedy**

To be shown in an updated presentation for December comment resolution meetings.

**Response Status:** C

**Comment ID: 87**

**Cl 124 SC 124.2.6.3 P 170 L 19 # 87**

Opsasnick, Eugene

**Comment Type:** ER

In Table 120G-4, four instances of "800GAUI-4" in last two rows of the table should likely be "800GAUI-8".

**Suggested Remedy**

Replace "800GAUI-4" with "800GAUI-8".

**Response Status:** C

**Comment ID: 88**

**Cl 124 SC 124.8.5a P 76 L 15 # 88**

Opsasnick, Eugene

**Comment Type:** ER

In second line of paragraph, "800GBASE-DR4" should probably be ".-DR8". Same text appears on line 25 in 124.8.5b, and on page 77, line 29, section 124.8.9.2.

**Suggested Remedy**

Replace "800GBASE-DR4" with "800GBASE-DR8".

**Response Status:** C

**Comment ID: 89**

**Cl 124 SC 124.3.1 P 63 L 13 # 89**

He, Xiang

**Comment Type:** ER

Looks like a typo. "16834 bit times" should be "16384 bit times"

**Suggested Remedy**

Change 16834 to 16384.

**Response Status:** C

**Comment ID: 90**

**Cl 172 SC 172.1.5 P 162 L 3 # 90**

Rechtman, Zvi

**Comment Type:** T

Figure 172–2—Functional block diagram

The block diagram includes two flows for TX and Rx. Both TX flows are supposed to insert the alignment markers in sync with each other. This does not appear explicitly in the diagram.

**Suggested Remedy**

Possible improvement #1:

Add arrow with the word synchronization between the "Alignment insertion" blocks.

Possible improvement #2:

Add a footnote that the two "Alignment insertion" should operate in synchronized manner.

**Response Status:** C

Implement with editorial license the changes on slide 38 of https://www.ieee802.org/3/df/public/22_12/brown_3df_03b_2212.pdf
### IEEE P802.3df D1.0 1st Task Force review comments

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#:</th>
<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>172</td>
<td>172.2.4.4</td>
<td>164</td>
<td>48</td>
<td>#91</td>
<td>91</td>
</tr>
<tr>
<td>Rechtman, Zvi</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong>: T <strong>Comment Status</strong>: AM sync</td>
<td></td>
<td></td>
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<tr>
<td>&quot;The first 66-bit block of the 257-bit transcoded block .. from the 64B/66B encoder.&quot;</td>
<td></td>
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<tr>
<td>This sentence implicitly means that the alignment insertion process of the two flows should be synchronized. To avoid mistakes, it would be preferable to explicitly state that the two alignment insertion are synchronized</td>
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<tr>
<td><strong>Suggested Remedy</strong>: Add the following sentence before &quot;The first 66-bit...&quot; sentence: &quot;The marker insertion functions of the two flows must insert their markers at the exact same time (block unit), i.e. in a synchronized manner&quot;</td>
<td></td>
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<tr>
<td><strong>Response</strong> <strong>Response Status</strong>: C</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>ACCEPT IN PRINCIPLE. Resolve using the response to comment #90.</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#:</th>
<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>30.5.1.1.2</td>
<td>33</td>
<td>1</td>
<td>#92</td>
<td>92</td>
</tr>
<tr>
<td>Wang, Haojie</td>
<td>China Mobile</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong>: ER <strong>Comment Status</strong>: A (bucket1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>There should be &quot;800GBASE-R&quot; other than &quot;400GBASE-R&quot;</td>
<td></td>
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<tr>
<td><strong>Suggested Remedy</strong>: Change &quot;400GBASE-R&quot; to &quot;800GBASE-R&quot;</td>
<td></td>
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<tr>
<td><strong>Response</strong> <strong>Response Status</strong>: C</td>
<td></td>
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<td>ACCEPT.</td>
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</tbody>
</table>

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<thead>
<tr>
<th>Cl</th>
<th>SC</th>
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<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>30.5.1.1.2</td>
<td>33</td>
<td>3</td>
<td>#93</td>
<td>93</td>
</tr>
<tr>
<td>Wang, Haojie</td>
<td>China Mobile</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong>: ER <strong>Comment Status</strong>: A (bucket1)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>There should be &quot;800GBASE-R&quot; other than &quot;400GBASE-R&quot;</td>
<td></td>
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</tr>
<tr>
<td><strong>Suggested Remedy</strong>: Change &quot;400GBASE-R&quot; to &quot;800GBASE-R&quot;</td>
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<tr>
<td><strong>Response</strong> <strong>Response Status</strong>: C</td>
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<td>ACCEPT.</td>
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</tbody>
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<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#:</th>
<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>124</td>
<td>124.11.3.1.1</td>
<td>80</td>
<td>32</td>
<td>#94</td>
<td>94</td>
</tr>
<tr>
<td>Wang, Haojie</td>
<td>China Mobile</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong>: ER <strong>Comment Status</strong>: A (bucket1)</td>
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<td></td>
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</tr>
<tr>
<td>The positions of &quot;Rx&quot; in figure 124-6 is inconsistent with the text at line 27, which is depicted as the right-most four positions.</td>
<td></td>
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<td></td>
</tr>
<tr>
<td><strong>Suggested Remedy</strong>: Plot the four &quot;Rx&quot; at the right-most four positions.</td>
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</tr>
<tr>
<td><strong>Response</strong> <strong>Response Status</strong>: C</td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>ACCEPT IN PRINCIPLE. Resolve using the response to comment #14.</td>
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</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#:</th>
<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>124</td>
<td>124.2</td>
<td>62</td>
<td>16</td>
<td>#95</td>
<td>95</td>
</tr>
<tr>
<td>Nicholl, Gary</td>
<td>Cisco Systems</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong>: ER <strong>Comment Status</strong>: A (bucket1)</td>
<td></td>
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<tr>
<td>The space after &quot;these&quot; should be underlined.</td>
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<tr>
<td><strong>Suggested Remedy</strong>: Underline the space after &quot;these&quot;</td>
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<tr>
<td><strong>Response</strong> <strong>Response Status</strong>: C</td>
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<td>ACCEPT.</td>
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</table>

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<thead>
<tr>
<th>Cl</th>
<th>SC</th>
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<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>124</td>
<td>124.2</td>
<td>62</td>
<td>29</td>
<td>#96</td>
<td>96</td>
</tr>
<tr>
<td>Nicholl, Gary</td>
<td>Cisco Systems</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong>: ER <strong>Comment Status</strong>: A (bucket1)</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>The space after &quot;have&quot; should be underlined.</td>
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<td></td>
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<tr>
<td><strong>Suggested Remedy</strong>: Underline the space after &quot;have&quot;</td>
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<tr>
<td><strong>Response</strong> <strong>Response Status</strong>: C</td>
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<td>ACCEPT.</td>
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</tr>
</tbody>
</table>
IEEE P802.3df D1.0 1st Task Force review comments

Comment Type: ER (bucket1)
Comment Status: A

Missing editing instruction to update the title of Figure 124-2 from "Block diagram for 400GBASE-DR4 transmit/receive paths" to "Block diagram for 400GBASE-DR4 or 400GBASE-DR4-2 transmit/receive paths"

Suggested Remedy:
Change the title of Figure 124-2 from "Block diagram for 400GBASE-DR4 transmit/receive paths" to "Block diagram for 400GBASE-DR4 or 400GBASE-DR4-2 transmit/receive paths"

Response Status: C

Nicholl, Gary
Cisco Systems

Response:
ACCEPT.

Comment Type: TR (bucket1)
Comment Status: A

Table 124-6. The row for "Outer Optical Modulation Amplitude (OMAouter), each lane (min)b" for 400GBASE-DR4 is different from what we did for 100GBASE-DR in Table 140-6 in 802.3cu. I am not sure it is correct to add "for TDECQ < 3.4 dB" as the value of OMA (min) is dependent on the value of TDECQ and is not flat across the board at -0.8dBm

Suggested Remedy:
I would suggest using the same format for 400GBASE-DR4 that was used for 100GBASE-DR in Table 140-6 of 802.3cu.

Response Status: C

Nicholl, Gary
Cisco Systems

Response:
ACCEPT IN PRINCIPLE.

The row for OMAouter is formatted correctly. However, in Table 124-6 for Launch power in OMAouter minus TDECQ, each lane (min) value of -2.2 should only apply to 400GBASE-DR4.

Fix the table with editorial license.

Comment Type: TR (bucket1)
Comment Status: A

Table 124-6. The row "Launch power in OMAouter minus TDECQ, each lane (min)" only applies to 400GBASE-DR4 and not to 800GBASE-DR8.

Suggested Remedy:
Correct this row in accordance with the comment to indicate that row only applies to 400GBASE-DR4 and not to 800GBASE-DR8. It should look more like the "TDECQ – 10log10(Ceq)c (max)" row on line 52.

Response Status: C

Nicholl, Gary
Cisco Systems

Response:
ACCEPT IN PRINCIPLE.

Implement proposed remedy with editorial license.
Comment Type ER  Comment Status A  (bucket1)
Table 124.6. Why are the rows "Transmitter overshoot and undershoot (max)", Transmitter power excursion (max) and "Transmitter transition time (max)" all in italics?
Suggested Remedy
Change the font of the text in the rows mentioned in the comment to standard table text.
Response Response Status C
ACCEPT.

Comment Type TR  Comment Status A  (bucket1)
Table 124.6. Footnote "b" only applies to 400GBASE-DR4
Suggested Remedy
Update footnote b to make it clear this footnote only applies to 400GBASE-DR4 (see what was done in Table 140-6 in 3cu as an example).
Response Response Status C
ACCEPT IN PRINCIPLE.
Implement proposed remedy with editorial license.

Comment Type TR  Comment Status A  (bucket1)
Table 124.6. The row "Receiver sensitivity (OMAouter), each lane (max)" for 400GBASE-DR4 is different than what was done for 100GBASE-DR in Table 140-7 in 3cu, and I am not sure it is technically correct.
Suggested Remedy
Remove "for TDECQ < 3.4 dB" for the row for 400GBASE-DR4, to follow the same format that was used for 100GBASE-DR in Table 140-7 in 802.3cu.
Response Response Status C
REJECT.
The format commented to is not broken for 400GBASE-DR4. It was considered an improvement to the format used in the base standard.

Comment Type TR  Comment Status A  (bucket1)
Table 124.11. Why would the optical return loss be any different between DR4/DR8 and DR4-2/DR8-2? Don't they both use the same MPO connector. The value of 25dB for DR4-2/DR8-2 appears to have been copied over from 100GBASE-FR1 in 802.3cu, but isn't FR1 using a different optical connector (LC versus MPO).
Suggested Remedy
This is more of a question for clarification.
Response Response Status C
ACCEPT IN PRINCIPLE.
In Table 124-11 change 25 dB for Optical return loss (min) to 37 dB.

Comment Type TR  Comment Status A  (bucket1)
Figure 124-6 indicates a different lane assignment for 400GBASE-DR4 than is in Clause 124 of the published version of the 802.3 standard. This would appear to make 400GBASE-DR4 incompatible with the current published standard.
Suggested Remedy
Change the lane assignment in Figure 124-6 in 802.3df D1.0 to match the lane assignment in Figure 124-6 of "P802.3_D3p2".
Response Response Status C
ACCEPT IN PRINCIPLE.
Resolve using the response to comment #14.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Comment ID

Comment ID 106  Page 22 of 47  2022-12-08 1:09:00 PM
The NOTE says "The stream of 66-bit blocks generated by this process". However, there are two streams generated in the above process. It would be clearer if the end of the sub-clause represented the end of the process and aligned with the OTN reference point in the note.

Also, it would be clearer for the text related to tx_coded<65:0> to coincide with the end of the sub-clause (i.e. for that text to follow any discussion related to rate compensation).

Also, where possible it is helpful to re-use text from 802.3-2022 Clause 119.2.4.1 as it enhances readability (i.e. simplifies compare/contrast between Clause 119 and Clause 172).

Suggested Remedy

Propose the following text:

172.2.4.1 Encode and rate matching

The transmit PCS generates 66-bit blocks based upon the TXD<63:0> and TXC<7:0> signals received from the 800GMII. One 800GMII data transfer is encoded into one 66-bit block. If the transmit PCS spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle control characters.

Idle control characters or sequence ordered sets are removed, if necessary, to accommodate the insertion of the alignment markers. See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules, and 172.2.4.5 for more details on alignment markers.

The transmit PCS generates blocks as specified in the transmit state diagram as shown in Figure 119-14. The contents of each 66-bit block are contained in a vector tx_coded<65:0>, tx_coded<1:0> contains the sync header and the remainder of the bits contain the payload.

NOTE: The stream of tx_coded<65:0> 66-bit blocks generated by this process, together with the FEC_degraded_SER and rx_local_degraded bits should be used as the reference signal for mapping to OTN.

172.2.4.1 66B/66B block distribution

The stream of tx_coded<65:0> 66-bit blocks are distributed to the two flows in a round robin fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue in a round robin distribution procedure across the two flows. This forms two streams, tx_coded_flow0<65:0> and tx_coded_flow1<65:0>.

172.2.4.3 64B/66B to 256B/257B transcoder

Let tx_coded_j<65:0> and tx_coded_k<65:0> represent two consecutive blocks in the tx_coded<65:0> stream. Notably, tx_coded_j<65:0> belongs to tx_coded_flow0<65:0> stream. And, tx_coded_k<65:0> belongs to tx_coded_flow1<65:0> stream.

Let tx_coded_j<65:0> represent the first 66-bit block of the 257-bit transcoded block following the alignment marker group in flow 0. It is required that tx_coded_k<65:0> shall be the first 66-bit block of the 257-bit transcoded block following the alignment marker group in flow 1.

Proposed Response

Propose the following text:

Let tx_coded_j<65:0> and tx_coded_k<65:0> represent two consecutive blocks in the tx_coded<65:0> stream. Notably, tx_coded_j<65:0> belongs to tx_coded_flow0<65:0> stream. And, tx_coded_k<65:0> belongs to tx_coded_flow1<65:0> stream.

Let tx_coded_j<65:0> represent the first 66-bit block of the 257-bit transcoded block following the alignment marker group in flow 0. It is required that tx_coded_k<65:0> shall be the first 66-bit block of the 257-bit transcoded block following the alignment marker group in flow 1.

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #90.
### 802.3df D1.0 1st Task Force review comments

**Comment ID 109**

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>FM</th>
<th>P169</th>
<th>L 11</th>
<th>#</th>
<th>109</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nicholl, Shawn</td>
<td>AMD</td>
<td><strong>Comment Type</strong></td>
<td>TR</td>
<td><strong>Comment Status</strong></td>
<td>R</td>
<td><strong>(bucket1)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Missing any mention of 800GBASE-R.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SuggestedRemedy</strong></td>
<td></td>
<td>For consistency with 119.2.6.2.2, propose to replace text &quot;with x = 0:31&quot; with text &quot;with x = 0:31 for 800GBASE-R.&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Response</strong></td>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The proposed change is not necessary since Clause 172 is only for 800GBASE-R. CL119 specified 200GBASE-R or 400GBASE-R because the same clause includes the PCS for both 200GE and 400GE.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment ID 110**

<table>
<thead>
<tr>
<th>Cl</th>
<th>FM</th>
<th>SC</th>
<th>FM</th>
<th>P1</th>
<th>L 10</th>
<th>#</th>
<th>110</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td><strong>Comment Type</strong></td>
<td>E</td>
<td><strong>Comment Status</strong></td>
<td>R</td>
<td><strong>(bucket1)</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;Amendment:&quot; - there should be an amendment number here. According to pages 13 and 14, this would be number 10. But 9 amendments before a revision is too many so there should be another roll-up and this could be amendment 1 of 802.3-2023.</td>
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<tr>
<td></td>
<td></td>
<td><strong>SuggestedRemedy</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Insert number or placeholder. Also on pages 11 and 27. Add it on page 14. If some amendment numbers including this one are provisional, that can be stated.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Response</strong></td>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>REJECT.</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>As the comment alludes, the amendment number that will be assigned to this amendment is not known at this time with any certainty. An amendments number may be inserted once a number is known with better certainty, likely near the end of WG Ballot.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment ID 111**

<table>
<thead>
<tr>
<th>Cl</th>
<th>FM</th>
<th>SC</th>
<th>FM</th>
<th>P1</th>
<th>L 30</th>
<th>#</th>
<th>111</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td><strong>Comment Type</strong></td>
<td>E</td>
<td><strong>Comment Status</strong></td>
<td>A</td>
<td><strong>(bucket1)</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation. Draft D1.0 is prepared for task force preview</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>SuggestedRemedy</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Media Access Control parameters for 800 Gb/s and Physical Layers and management parameters for 400 Gb/s and 800 Gb/s operation. Draft D1.0 is prepared for Task Force preview</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Response</strong></td>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>ACCEPT IN PRINCIPLE.</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The comment appears to be pointing out that capitalization on some words need s to be corrected.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Change: &quot;Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation. Draft D1.0 is prepared for task force preview&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>To: &quot;Media Access Control parameters for 800 Gb/s and Physical Layers and management parameters for 400 Gb/s and 800 Gb/s operation. Draft D1.0 is prepared for Task Force preview&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Implement with editorial license.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment ID 112**

<table>
<thead>
<tr>
<th>Cl</th>
<th>FM</th>
<th>SC</th>
<th>FM</th>
<th>P6</th>
<th>L 39</th>
<th>#</th>
<th>112</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td><strong>Comment Type</strong></td>
<td>E</td>
<td><strong>Comment Status</strong></td>
<td>R</td>
<td><strong>(bucket1)</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The superscript 3 should follow IEEE Xplore, not &quot;contact IEEE.&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>SuggestedRemedy</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Get the template at <a href="https://standards.ieee.org/develop/drafting-standard/resources/">https://standards.ieee.org/develop/drafting-standard/resources/</a> fixed and implement the change.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Response</strong></td>
<td><strong>Response Status</strong></td>
<td>C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>REJECT.</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This footnote location is the same as in the cited template. This text is an official statement copied to the IEEE 802.3 template from the IEEE SA template. According to the 2021 IEEE SA Standards Style Manual, this text &quot;Shall not be altered.&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cl/ FM</td>
<td>SC FM</td>
<td>P</td>
<td>L</td>
<td>#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>----</td>
<td>----</td>
<td>----</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td>1</td>
<td>113</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dawe, Piers
Nvidia

Comment Type: E  Comment Status: A

“When the IEEE-SA Standards Board”: duplicate section

Suggested Remedy
Remove

Response
Response Status: C

ACCEPT IN PRINCIPLE.

The group of text starting with “When the IEEE-SA Standards Board:” is repeated twice. Remove one instance.

Implement with editorial license.

<table>
<thead>
<tr>
<th>Cl/ FM</th>
<th>SC FM</th>
<th>P</th>
<th>L</th>
<th>#</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td></td>
<td></td>
<td>48</td>
<td>114</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dawe, Piers
Nvidia

Comment Type: E  Comment Status: A

3bj and 3bk!! They were approved in 2013 and 2014. 3cy uses 3cx and 3cz as its examples, 3cz uses 3dd, 3cs, 3db, 3ck, 3de and 3cx

Suggested Remedy
Instead of or as well as this bad example, list all the exact amendments and drafts that this draft is built against, as P802.3cz does. Also, say which drafts affect this draft and which are believed not to, preferably clause by clause. The editors must have and agree this information; no reason not to share it with the volunteers who do the review work, and the staff editors.

Response
Response Status: C

ACCEPT IN PRINCIPLE.

The example projects listed are indeed obsolete. This example list from the FrameMaker template needs to be updated for each project and may again change as previous amendments are incorporate into a revision. The examples are not really required so these examples should be deleted here and in the template.

Delete "(e.g., IEEE P802.3bj and IEEE P802.3bk)"

<table>
<thead>
<tr>
<th>Cl/ FM</th>
<th>SC FM</th>
<th>P</th>
<th>L</th>
<th>#</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td></td>
<td></td>
<td>30</td>
<td>116</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dawe, Piers
Nvidia

Comment Type: E  Comment Status: R

This project is adding another page of definitions to a very long section that doesn't have the usual pdf bookmarks.

Suggested Remedy
To mitigate the deterioration of document structure and usability, divide 1.4 Definitions into subclauses, e.g.
1.4.1 1 to 8
1.4.2 A to G
1.4.3 H to M
1.4.4 N to S
1.4.5 T to Z
If Frame can deliver 1.4.0 ... 1.4.8 1.4.A ... 1.4.Z (some such as 1.4.3 are not needed), that would be even more user-friendly.

Response
Response Status: C

REJECT.

The comment is asking for broad changes to the base standard that are not related directly the new content that is being added by this amendment. Such sweeping changes should be addressed using the Base Standard maintenance process.

<table>
<thead>
<tr>
<th>Cl/ FM</th>
<th>SC FM</th>
<th>P</th>
<th>L</th>
<th>#</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.4</td>
<td>P</td>
<td>18</td>
<td>47</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dawe, Piers
Nvidia

Comment Type: E  Comment Status: R

This project is adding to an already long section that lacks the usual level of subdivision (somewhere around one subclause per page would be normal)

Suggested Remedy
To mitigate the deterioration of document structure and usability, divide 1.5 Abbreviations into several subclauses

Response
Response Status: C

REJECT.

The comment is asking for broad changes to the base standard that are not related directly the new content that is being added by this amendment. Such sweeping changes should be addressed using the Base Standard maintenance process.
IEEE P802.3df D1.0  1st Task Force review comments

Comment #117
Cl 45 SC 45.2.1.6 P 36 L 20

Dawe, Piers  Nvidia

Comment Type T  Comment Status A  (bucket1)
Where possible, entries should be in the standard order: slow to fast, short to long, wide to narrow. Here, we have to read upwards because the entries are listed backwards.

SuggestedRemedy
Swap VR8 and SR8

ACCEPT.

Response  Response Status C

Comment #118
Cl 45 SC 45.2.1.7.4 P 37 L 23

Dawe, Piers  Nvidia

Comment Type T  Comment Status A  (bucket1)
Missing entries in transmit fault, receive fault and transmit disable tables

SuggestedRemedy
Include rows for 100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, 400GBASE-SR4, 800GBASE-VR8, 800GBASE-SR8 and 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, 800GBASE-DR8-2
Revise the rubrics.

Response  Response Status C

ACCEPT.

Comment #119
Cl 45 SC 45.2.1.161 P 41 L 34

Dawe, Piers  Nvidia

Comment Type E  Comment Status A  (bucket1)
92.7.12 and 136.8.11.1.3

SuggestedRemedy
92.7.12, 136.8.11.1.3, or 162.8.11.1 as appropriate

Response  Response Status C

ACCEPT IN PRINCIPLE. Change the first sentence of the second paragraph of 45.2.1.168 so it reads as "Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training a particular PMD lane as described in 92.7.12, 136.8.11.1.3, or 162.8.11.1."

Comment #120
Cl 45 SC 45.2.1.168 P 42 L 38

Dawe, Piers  Nvidia

Comment Type E  Comment Status A  (bucket1)
"for PMD lane 1; etc.": a bit terse and informal

SuggestedRemedy
Suggested rewording: Register 1.1450 controls the PMD training pattern for PMD lane 0, register 1.1451 controls the PMD training pattern for PMD lane 1, and so on, up to register 1.1457 and PMD lane 7.

Response  Response Status C

ACCEPT IN PRINCIPLE. Resolve using the response to comment #32.

Comment #121
Cl 45 SC 45.2.1.168 P 42 L 41

Dawe, Piers  Nvidia

Comment Type E  Comment Status A  (bucket1)
92.7.12 and 136.8.11.1.3

SuggestedRemedy
92.7.12, 136.8.11.1.3, or 162.8.11.1 as appropriate

Response  Response Status C

ACCEPT IN PRINCIPLE. Change the first sentence of the second paragraph of 45.2.1.168 so it reads as "Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training a particular PMD lane as described in 92.7.12, 136.8.11.1.3, or 162.8.11.1."
IEEE P802.3df D1.0 1st Task Force review comments

**SuggestedRemedy**

1. Put signal integrity recommendations in the spec, not in the register definitions for a memory map!
2. Change "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function." This says "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function.."
   
   This is a section defining the meanings of bits in a memory map. The memory map serves the sublayer, not the other way round. Advice about signal integrity should be in the clause concerned.

   With only four polynomials and eight lanes, the polynomials themselves can't all be different, but that's OK. Impairment is very unlikely unless adjacent lanes use the same polynomial AND the PRBS13Qs in the training pattern are aligned in time with each other. We have written generations of PMD and AUI clauses that use the same pattern on multiple lanes, but they should be skewed, e.g. 120G.3.2.2: "For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated." The training frame is 98.3% PRBS13Q. In principle, one could incur the risk warned against with a lane carrying "identifier_1 = 0 and an adjacent lane carrying "identifier_1 = 4, with an unlucky timing offset between lanes. As "The PMD shall implement one instance of the PMD control function described in 136.8.11 for each lane", the state machine for each lane can be started and restarted asynchronously to adjacent lanes, so starting the training pattern with a different seed won't solve the issue. The text "For 8-lane use cases different initial seeds should be used where the same polynomial is being reused." recommends a course of action that, on investigation, doesn't address the issue. We should tell the reader what to avoid, not how to avoid it.

   Also, the ETC spec has already covered this ground. It uses the same four polynomials and seeds, twice over. No implementation can follow the ETC spec AND this draft (because the default seeds differ) but there is no benefit in the difference.

**SuggestedRemedy**

1. Put signal integrity recommendations in the spec, not in the register definitions for a memory map!
2. Change "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function." to "The polynomial identifier for adjacent lanes should be unique to avoid a risk of impairment of the PMD control function." (see: https://www.ieee802.org/3/df/public/22_09/lusted_3df_01a_2209.pdf). A user would be able to change the default values so that the seeds for lanes 4 to 7 match 0 to 3 by writing appropriate seed values to registers 1.1450 through 1.1457. Therefore it is not appropriate to change Table 162-10a. See also the response to comment #139

   **SuggestedRemedy**

   If people will want to connect 200G-class servers with SMF, perhaps to a CPO switch, before 200GBASE-DR1 is cheaper, then it will happen. If it will happen, it would be best to move on to 400G-class servers?

   **SuggestedRemedy**

   Wondering if we want 200GBASE-DR2 and 200GBASE-DR2-2. Will people connect 200G-class servers with copper or MMF only until 200GBASE-DR1 is cheaper or they move on to 400G-class servers?

   **SuggestedRemedy**

   If people will want to connect 200G-class servers with SMF, perhaps to a CPO switch, before 200GBASE-DR1 is cheaper, then it will happen. If it will happen, it would be best to move on to 400G-class servers.

   **SuggestedRemedy**

   A user would be able to change the default values so that the seeds for lanes 4 to 7 match 0 to 3 by writing appropriate seed values to registers 1.1450 through 1.1457. Therefore it is not appropriate to change Table 162-10a.

   See also the response to comment #139

   **SuggestedRemedy**

   Replace "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11. For 8-lane use cases different initial seeds should be used where the same polynomial is being reused." with "The polynomial identifier for adjacent lanes should be unique to avoid a risk of impairment of the PMD control function. If the same polynomial identifier is used for multiple lanes, different initial seeds should be used for each of those lanes. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11." The adopted baseline clearly states what the default seeds in Table 162-10a should be (see: https://www.ieee802.org/3/df/public/22_09/lusted_3df_01a_2209.pdf). A user would be able to change the default values so that the seeds for lanes 4 to 7 match 0 to 3 by writing appropriate seed values to registers 1.1450 through 1.1457. Therefore it is not appropriate to change Table 162-10a.

   **SuggestedRemedy**

   If people will want to connect 200G-class servers with SMF, perhaps to a CPO switch, before 200GBASE-DR1 is cheaper, then it will happen. If it will happen, it would be best to include it so that it gets official code points.

   **SuggestedRemedy**

   The comment is proposing the addition of two PMD types which are not in scope for the IEEE P802.3df project.
<table>
<thead>
<tr>
<th>CI</th>
<th>124</th>
<th>SC</th>
<th>124.1</th>
<th>P61</th>
<th>L36</th>
<th>#</th>
<th>124</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Status</strong></td>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SuggestedRemedy</strong></td>
<td>400GBASE-DR4, 400GBASE-DR4-2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CI</th>
<th>124</th>
<th>SC</th>
<th>124.2</th>
<th>P62</th>
<th>L40</th>
<th>#</th>
<th>125</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Status</strong></td>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SuggestedRemedy</strong></td>
<td>six paragraphs 124.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CI</th>
<th>124</th>
<th>SC</th>
<th>124.7.2</th>
<th>P70</th>
<th>L36</th>
<th>#</th>
<th>127</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>TR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Status</strong></td>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| **SuggestedRemedy** | The unlikely case of defective transition density is far more significant than the very modest difference between 2-way and 4-way RS-FEC interleaving. If we are going to break precedent and abandon unrestricted bit-multiplexing, transition density is the first thing to get right, always. With 100G AUI lanes, the Tx silicon can ensure the problem doesn't happen, and we are not mandating 50G/lane AUIs for 800G. We have had some years after this problem was discovered before 800G designs, so it should not be happening now. Let's say so.

<table>
<thead>
<tr>
<th>Response</th>
<th><strong>Response Status</strong></th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACCEPT IN PRINCIPLE. Resolve using the response to comment #38.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CI</th>
<th>124</th>
<th>SC</th>
<th>124.7.2</th>
<th>P70</th>
<th>L36</th>
<th>#</th>
<th>127</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>TR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Status</strong></td>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| **SuggestedRemedy** | As elsewhere: change "See NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate." to "For 400GBASE-DR4 and 400GBASE-DR4-2, see NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate. For 800GBASE-DR8 and 800GBASE-DR8-2, see 173.4.2." Similarly in 124.7.2.

In 173.4.2, say that unlike in 120, it is the transmit side PCS and PMA's responsibility to avoid the defective transition density, and give some recommendations. See other comments.

<table>
<thead>
<tr>
<th>Response</th>
<th><strong>Response Status</strong></th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>REJECT. Resolve using the response to comment #166.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CI</th>
<th>124</th>
<th>SC</th>
<th>124.7.2</th>
<th>P70</th>
<th>L36</th>
<th>#</th>
<th>127</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>TR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Status</strong></td>
<td>R</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SuggestedRemedy</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Response</th>
<th><strong>Response Status</strong></th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>REJECT. Resolve using the response to comment #166.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cl 124</td>
<td>SC 124.7.2</td>
<td>P 71</td>
</tr>
<tr>
<td>------</td>
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<td>-----</td>
</tr>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td>Comment Type E</td>
</tr>
<tr>
<td>Suggested Remedy</td>
<td></td>
<td>SECO (as in 124.8.9.1), three times</td>
</tr>
<tr>
<td>Response</td>
<td>Response Status C</td>
<td>ACCEPT IN PRINCIPLE.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For parameter, Receiver sensitivity (OMAouter), each lane (max), change first occurrence of TDECQ to SECQ and 2 further occurrences to TECQ.</td>
</tr>
<tr>
<td></td>
<td>Implement with editorial license.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cl 124</th>
<th>SC 124.8.1</th>
<th>P 75</th>
<th>L 4</th>
<th># 129</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td>Comment Type E</td>
<td>Comment Status A</td>
<td>test pattern (CC)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>800G scrambled idle isn't in 119.2.4.9: different rate, different PCS. See another comment.</td>
<td></td>
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<tr>
<td>Suggested Remedy</td>
<td></td>
<td>In Table 124-9, after 119.2.4.9, add ’or 172.2.4.9’</td>
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</tr>
<tr>
<td>Response</td>
<td>Response Status C</td>
<td>ACCEPT IN PRINCIPLE.</td>
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<tr>
<td></td>
<td>Implement the suggested remedy with editorial license.</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cl 124</th>
<th>SC 124.8.5</th>
<th>P 76</th>
<th>L 5</th>
<th># 130</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td>Comment Type E</td>
<td>Comment Status A</td>
<td>TX test</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This says “The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel that meets the requirements for 100GBASE-FR1 in 140.7.5.2” but these PMDs have an optical return loss tolerance of 21.4 while 100GBASE-FR1 uses an optical return loss of 17.1 dB. The cable plant is different (array connectors are angled).</td>
<td></td>
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<tr>
<td>Suggested Remedy</td>
<td></td>
<td>Change The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel that meets the requirements for 100GBASE-FR1 in 140.7.5.2.</td>
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<td></td>
<td></td>
<td>To The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel with dispersion and insertion loss as for 100GBASE-FR1 in 140.7.5.2, and optical return loss at the maximum for optical return loss tolerance in Table 124-6.</td>
<td></td>
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</tr>
<tr>
<td>Response</td>
<td>Response Status C</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Implement suggested remedy with editorial license.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cl 124</th>
<th>SC 124.11.1</th>
<th>P 79</th>
<th>L 20</th>
<th># 131</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td>Comment Type E</td>
<td>Comment Status A</td>
<td>reflections</td>
</tr>
<tr>
<td></td>
<td></td>
<td>These fiber optic cabling characteristics for 400GBASE-DR4-2 and 800GBASE-DR8-2 are not in the baseline, but are the same as for 100GBASE-FR1. The optical return loss should not follow FR1, as the optical return loss tolerance is significantly different and the table of discrete reflectances is different.</td>
<td></td>
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<tr>
<td>Suggested Remedy</td>
<td></td>
<td>Adjust the optical return loss as necessary to be consistent with the adopted optical return loss tolerance and table of discrete reflectances.</td>
<td></td>
<td></td>
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<tr>
<td>Response</td>
<td>Response Status C</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Resolve using the response to comment #105.</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>CI</td>
<td>SC</td>
<td>PAGE</td>
<td>LIN</td>
<td>COMMENT ID</td>
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<td>------------</td>
</tr>
<tr>
<td>124</td>
<td>124.11.2.2</td>
<td>P 79</td>
<td>L 43</td>
<td># 132</td>
</tr>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td><strong>Comment Type:</strong> T</td>
<td><strong>Comment Status:</strong> R</td>
<td></td>
</tr>
<tr>
<td>Part of the baselines is missing. Both baselines have a table of discrete reflectances above 55 dB</td>
<td></td>
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<td></td>
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<tr>
<td><strong>Suggested Remedy:</strong></td>
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<tr>
<td>Add this (these) as a new column(s) in Table 124-9</td>
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<tr>
<td><strong>Response:</strong> REJECT.</td>
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<tr>
<td>The baselines previously agreed were not correct with respect to the table of discrete reflectances for the 2km interfaces. Table 124-13 in the in-force Clause 124 has not been modified (as such not shown in P802.3-df D1.0) and is therefore valid for all 4 DR PMD types.</td>
<td></td>
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<tr>
<td>No changes to the draft are required.</td>
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</tr>
</tbody>
</table>

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<thead>
<tr>
<th>CI</th>
<th>SC</th>
<th>PAGE</th>
<th>LIN</th>
<th>COMMENT ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>124</td>
<td>124.11.2.2</td>
<td>P 79</td>
<td>L 43</td>
<td># 133</td>
</tr>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td><strong>Comment Type:</strong> E</td>
<td><strong>Comment Status:</strong> R</td>
<td></td>
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<tr>
<td>It seems odd that the table of discrete reflectances above 55 dB for 800GBase-DR8 in the baseline is not the same as the existing table for 400GBase-DR4, but it is the same as 400GBase-DR4-2 and 800GBase-DR8-2.</td>
<td></td>
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</tr>
<tr>
<td><strong>Suggested Remedy:</strong> Reconcile the tables for 400GBase-DR4 and 800GBase-DR8</td>
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</tr>
<tr>
<td><strong>Response:</strong> REJECT.</td>
<td></td>
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</tr>
</tbody>
</table>

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<thead>
<tr>
<th>CI</th>
<th>SC</th>
<th>PAGE</th>
<th>LIN</th>
<th>COMMENT ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>124</td>
<td>124.11.3.1.1</td>
<td>P 80</td>
<td>L 33</td>
<td># 134</td>
</tr>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td><strong>Comment Type:</strong> E</td>
<td><strong>Comment Status:</strong> R</td>
<td></td>
</tr>
<tr>
<td>“The transmit optical lanes occupy the leftmost eight positions. The receive optical lanes occupy the rightmost eight positions”: as there are only 12 positions, “most” is not really applicable.</td>
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</tr>
<tr>
<td><strong>Suggested Remedy:</strong> Change to “The transmit optical lanes occupy the eight positions on the left. The receive optical lanes occupy the eight positions on the right.”</td>
<td></td>
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<tr>
<td><strong>Response:</strong> REJECT.</td>
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<tr>
<td>The proposed changes do not improve the accuracy or clarity of the draft. There are 16 positions.</td>
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</tbody>
</table>

**Note:** The comments and responses continue with similar structure, indicating detailed feedback on specific technical aspects of the draft, including tables, table entries, and figure information, along with the status of the comments (accepted, rejected, or pending).
Comment Type: T  Comment Status: A  PRBS seed

the state of the PRBS generator shall be set to a value in the variable - eh? If the variable is a 13-bit seed, it contains 0s and 1s.

Suggested Remedy

Rewrite for clarity

Response

ACCEPT IN PRINCIPLE.

In the second paragraph of 162.8.11.1, change from "the state of the PRBS generator shall be set to a value in the variable seed_i." to "the state of the PRBS generator shall be set to the value of the variable seed_i."

Comment Type: T  Comment Status: A  PRBS seed

The variable seed_i is not defined. 136.8.11.1.3 says "The default value of seed_i shall be the value given in Table 136-8 for p = l," but neither p nor Table 136-8 apply here. Maybe they should?

Suggested Remedy

If the seed bits in Table 162-10a are the defaults for seed_i, say so.

Response

ACCEPT IN PRINCIPLE.

In the third paragraph of 162.8.11.1, change "the default seed for each lane" to "the default value of seed_i for each lane i." In Table 162-10a, change the heading of the fourth column from "Default seed bits" to "Default seed_i".

Dawe, Piers
Nvidia

Comment Type: TR
Comment Status: R
PRBS seed

Dedual seeds 4 to 7 are different to seeds 0 to 3, contrary to the ETC 800G spec. No implementation can follow the ETC spec AND this draft (because the default seeds differ) but there is no benefit in the difference.

We have written generations of PMD and AUI clauses that use the same pattern on multiple lanes, but they should be skewed, e.g. 120G.3.2.2: "For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated." The training frame is 98.3% PRBS13Q. In principle, one could incur the risk warned against with a lane carrying "identifier_i" = 0 and an adjacent lane carrying "identifier_i" = 4, with an unlucky timing offset between lanes. As "The PMD shall implement one instance of the PMD control function described in 136.8.11 for each lane", the state machine for each lane can be started and restarted asynchronous to adjacent lanes, so starting the training pattern with a different seed won't solve the issue.

Suggested Remedy

1. Make the default seeds in Table 162-10a the same as in the ETC spec (seeds 4 to 7 are the same as seeds 0 to 3).
2. ETC say "it is recommended to ensure that physically adjacent lanes do not use the same polynomial". Recommend this.
4. Also, point out that significant correlation between any lanes can be avoided by a combination of seed and timing offset. Leave it to the implementer to choose how to do this.

Response

REJECT.

Aligning an IEEE standard with a previously published document may be preferable where possible, but it is not always done.

The default seed values were explicitly set by the adopted baseline proposal https://www.ieee802.org/3/df/public/22_09/lusted_3df_01a_2209.pdf, which included a detailed description, and was approved by unanimous consent.

The seed values are not normative, and using non-default values is permitted, so there is no compliance concern.

The content of item 2 and 4 of the suggested remedy is covered by text in 45.2.1.168 ("should" is a recommendation).
IEEE P802.3df D1.0 1st Task Force review comments

Cl 162 SC 162.9.4 P 93 L 17 # 140
Dawe, Piers Nvidia

Comment Type E Comment Status A

"For an 800GBASE-CR8 PMD or for a 100GBASE-CR1, 200GBASE-CR2, or 400GBASE-CR4 PMD in the same package as the PCS sublayer": it's very easy to misunderstand this.

Suggested Remedy
At least put a comma after "CR8 PMD". Also in 163.9.2.

Response
Accept in principle.

The text intentionally distinguishes between 800GAUI-8, for which the range is always +/- 50 PPM, and the other interfaces, for which it is conditional.

The text can be clarified.

In Table 162-11 change the first sentence in footnote a to the following:
"For 100GBASE-CR1, 200GBASE-CR2, or 400GBASE-CR4 PMD with a PMA in the same package as the PCS sublayer or for any 800GBASE-CR8 PMD."

In Table 163-5 change the first sentence in footnote a to the following:
"For 100GBASE-KR1, 200GBASE-KR2, or 400GBASE-KR4 PMD with a PMA in the same package as the PCS sublayer or for any 800GBASE-KR8 PMD."

Cl 162 SC 162.9.5 P 93 L 36 # 141
Dawe, Piers Nvidia

Comment Type E Comment Status A (bucket 1)

This text is an informative NOTE in the standard in force, as below. While I can see the reason to make it normative for the transmitter, for the receiver this information about transmitter behaviour is explanation, not something the receiver does.

Suggested Remedy
Change it from a normative table footnote to an informative table note. Similarly for 163.9.3.

Response
Accept.

Cl 167 SC 167.5.1 P 111 L 7 # 142
Dawe, Piers Nvidia

Comment Type E Comment Status A (bucket 1)

Strange to talk about 800G before 100G and 200G: not the usual order (slow MAC to fast MAC).

Suggested Remedy
The block diagrams for 100GBASE-VR1 and 100GBASE-SR1 are equivalent to Figure 167-2, but for one lane per direction. The block diagrams for 200GBASE-VR2 and 200GBASE-SR2 are equivalent to Figure 167-2, but for two lanes per direction. The block diagrams for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for eight lanes per direction.

or
The block diagrams for 100GBASE-VR1 and 100GBASE-SR1, for 200GBASE-VR2 and 200GBASE-SR2, and for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for one, two and eight lanes per direction respectively.

Response
Accept in principle.

Change editing instruction to "Replace the first paragraph in 167.5.1 with the following:" with the text "The PMD block diagram for 400GBASE-VR4 or 400GBASE-SR4 is shown in Figure 167–2. The block diagrams for 100GBASE-VR1 and 100GBASE-SR1 are equivalent to Figure 167-2, but for one lane per direction. The block diagrams for 200GBASE-VR2 and 200GBASE-SR2 are equivalent to Figure 167-2, but for two lanes per direction. The block diagrams for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for eight lanes per direction."

Cl 167 SC 167.8.1 P 117 L 4 # 143
Dawe, Piers Nvidia

Comment Type T Comment Status A (test pattern (CC))

In Table 167-10, Test patterns, need a new reference for scrambled idle. See another comment.

Suggested Remedy
Change "82.2.11 and 91, or 119.2.4.9" to "82.2.11 and 91, or 119.2.4.9, or 172.2.4.9"

Response
Accept in principle.

Implement the suggested remedy with editorial license.
### IEEE P802.3df D1.0 1st Task Force review comments

<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Page</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Comment</th>
<th>SuggestedRemedy</th>
</tr>
</thead>
<tbody>
<tr>
<td>#144</td>
<td>17</td>
<td>E</td>
<td></td>
<td>Font problem</td>
<td>_ACCEPT IN PRINCIPLE. Resolve using the response to comment #194.</td>
</tr>
<tr>
<td>#145</td>
<td>17</td>
<td>T</td>
<td></td>
<td>The two options for 400GBASE-SR8 were defined but we should check if the industry is still split on how to connect 8-lane MMF modules.</td>
<td>Check if Option B, 16-fiber interface, has traction in the industry. If it doesn’t, don’t include it.</td>
</tr>
</tbody>
</table>

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### TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general

### COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn

### SORT ORDER: Comment ID

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**Comment ID 144**

**Comment**

Font problem

**SuggestedRemedy**

_ACCEPT IN PRINCIPLE. Resolve using the response to comment #194.

---

**Comment ID 145**

**Comment**

The two options for 400GBASE-SR8 were defined but we should check if the industry is still split on how to connect 8-lane MMF modules.

**SuggestedRemedy**

Check if Option B, 16-fiber interface, has traction in the industry. If it doesn’t, don’t include it.

**Response**

_ACCEPT IN PRINCIPLE. Resolve using the response to comment #146.
MPO active device receptacle, angled interface for 16 fibers, as defined in IEC 61754-7-4. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-4-1: MPO female plug, down-angled interface for 16 fibers. The MPO female plug connector and MDI are structurally similar to those depicted in Figure 167-9, but with 16 fibers, an offset keyway, and with different pin diameter and locations. The MDI connection shall meet the interface performance specifications of IEC 63267-1 for performance grade Bm/1m.

**Comment ID 147**

**Dawe, Piers**

**Nvidia**

**Comment Type** E  **Comment Status** R

**PMA description**

Wow, this is too mean with the information. Compare 116.2.4: the equivalent of this is missing: “The 200GBASE-R and 400GBASE-R PMAs perform the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMA performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test pattern generation and checking.”

**Suggested Remedy**

At least say that a PMA connects the PCS and PMA via the PMA service interface, and the PMA and PMD via the PMD service interface, and that there can be more than one PMA (in series) for one MAC. It performs retiming of the received data stream when appropriate. There are optional defined physical instantiations called AUIs. And/or, at line 35, add “and a summary of its functions is given in 173.1.3”.

**Response** C  **Response Status** C

REJECT.

The description provided in Clause 116 was overly verbose with repeated details that are listed in the reference PMA clause. The PMA description in Clause 169 provides the general function of a PMA with similar detail provided in the other sublayer descriptions and references the relevant PMA subclauses where the reader may find all of the details relevant to each PMA type.

**Comment ID 149**

**Dawe, Piers**

**Nvidia**

**Comment Type** T  **Comment Status** R

**Figure lanes**

In Figure 116-2, multiple lanes are shown explicitly: PMA:IS_UNITDATA_0.request PMA:IS_UNITDATA_1.request ... PMA:IS_UNITDATA_7.request

**Suggested Remedy**

As a compromise, follow e.g. Figure 120G-2: add the short diagonal lines "n" to show n lanes, not n requests on one lane with a constant ordering. Several figures, including Fig 172-2 where showing the numbers, 16 and 32, will be helpful.

**Response** C  **Response Status** C

REJECT.

A single line with an SI parameter with vector notation clearly conveys the fact that there are multiple lanes 0 to n-1. This approach is used to reduce the clutter compared to similar diagrams in Clause 116. This approach is used consistently in various figures in 802.3df. The proposed changes do not improve the accuracy or clarity of the draft.
Comment Type: E  Comment Status: R  (bucket2)

116.5 says "Skew (or relative delay) can be introduced between lanes". This says "Skew (or relative delay) can be introduced between PCS lanes" which gives a false impression that PMA and PMD lanes don't get skewed.

Suggested Remedy
Delete "PCS", once.

Response  Response Status: C
REJECT.
Skew is constrained for each sublayer to limit the net skew between PCS lanes so that the cumulative skew between PCS lanes does not exceed the ability of the specified PCS deskew function.

Comment Type: E  Comment Status: A  (bucket1)

points for a single 800GAUI-n

Suggested Remedy
points for a single 800GAUI-n

Response  Response Status: C
ACCEPT IN PRINCIPLE.
In Figure 169-4...
Change "800BASE-R Skew points for single 800GAUI-n" To: "800BASE-R Skew points for a PHY with a single 800GAUI-n"
In Figure 169-5...
Change "Skew points for multiple 800GAUI-n" To: "Skew points for a PHY with multiple 800GAUI-n"

Comment Type: T  Comment Status: R  (bucket2)

Under "MDIO status variable" there is an entry "Lane 0 to 31 aligned" but this isn’t a variable that indicates if lanes 0 to 31 are aligned. Table 45-350 has "Name’s Lane 0 aligned, Lane 1 aligned, and so on. Is there such a thing as an "MDIO variable" anyway? Clauses such as PCS have variables, MDIO has registers. The way of talking about such multilane things was solved long ago; e.g. "84.7.5 PMD lane-by-lane signal detect function"

Suggested Remedy
Because a "variable" must be talking about one lane not the pair of registers recording 16 or 32 lanes, change "Lane 0 to 31 aligned" back to how it is in 117: "Lane x aligned" or "Lane i aligned" or better, "Lane aligned". "Lane-by-lane aligned" seems odd, but "DTE XS FEC symbol errors lane 0 to lane 31" below can be "DTE XS FEC symbol errors by lane" Similarly in several tables, also in other clauses such as 172, PCS.

Response  Response Status: C
REJECT.
There is no consensus to make a change at this time. Further work and consensus building is encouraged.
IEEE P802.3df D1.0 1st Task Force review comments

Cl 171 SC 171.4 P 153 L 11 # [155] (bucket1)
Dawe, Piers Nvidia
Comment Type T  Comment Status A
16 bits for 32 lanes
SuggestedRemedy
Need more registers
Response Response Status C
ACCEPT IN PRINCIPLE.
Update Table 171-5 to align with register/bit definitions in Clause 45.

Cl 172 SC 172.1.1 P 160 L 11 # [156] (bucket2)
Dawe, Piers Nvidia
Comment Type E  Comment Status R
The paragraph of introduction in 119.1.1 is missing: "Both 200GBASE-R and 400GBASE-R are based on a 64B/66B code. The 64B/66B code supports transmission of data and control characters. The 64B/66B code is then transcode to 256B/257B encoding to reduce the overhead and make room for forward error correction (FEC). The 256B/257B encoded data is then FEC encoded before being transmitted. Data distribution is introduced to support multiple lanes in the Physical Layer. Part of the distribution includes the periodic insertion of an alignment marker, which allows the receive PCS to align data from multiple lanes."
SuggestedRemedy
At least refer to 172.1.3 as an introduction.
Response Response Status C
REJECT.
172.1.1 is the scope and the current text is a sufficient description of the scope of the clause. All of the information noted in the comment is provided in 172.1.3 and there is no need to duplicate it in the scope.

Cl 172 SC 172.1.5 P 162 L 12 # [158] (bucket1)
Dawe, Piers Nvidia
Comment Type E  Comment Status A
Transcode
SuggestedRemedy
transcode - 4 times  Also in this figure: Encode, Decode, Interleave, Lane
Response Response Status C
ACCEPT IN PRINCIPLE.
Correct the capitalization with editorial license.

Cl 173 SC 173.3 P 179 L 17 # [160] (bucket1)
Dawe, Piers Nvidia
Comment Type E  Comment Status A
another PMA or a PMD
SuggestedRemedy
a PMD or another PMA
Response Response Status C
ACCEPT IN PRINCIPLE.
Resolve using the response to comment #180

Comment ID 160  Page 36 of 47
TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Comment ID
**IEEE P802.3df D1.0 1st Task Force review comments**

**Comment ID 161**

**Cl 173 SC 173.3 P 179 L 19 # [161]**

Dawe, Piers Nvidia

**Comment Type E**  **Comment Status A** (bucket1)

"defined in 169.3" but 173.2 says "defined in 169.3.1"

**SuggestedRemedy**

Reconcile

**Response**  **Response Status C**

ACCEPT IN PRINCIPLE.

Change from "169.3" to "169.3.1"

**Comment ID 162**

**Cl 173 SC 173.4 P 180 L 20 # [162]**

Dawe, Piers Nvidia

**Comment Type T**  **Comment Status A** PMA SI

The interface below the PMA (8 lanes) connects with either a PMD or a physically instantiated interface (800GAUI-8).

**SuggestedRemedy**

The interface below the PMA (8 lanes) either connects with a PMD or it is a physically instantiated interface (800GAUI-8) connecting to another 800GAUI-8 PMA interface in another PMA. Similarly twice more.

**Response**  **Response Status C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #196.

**Comment ID 163**

**Cl 173 SC 173.4 P 180 L 1 # [163]**

Dawe, Piers Nvidia

**Comment Type E**  **Comment Status A** (bucket1)

Something strange about the page layout; these sections start to the left of the header

**SuggestedRemedy**

Reconcile

**Response**  **Response Status C**

ACCEPT.

**Comment ID 164**

**Cl 173 SC 173.4 P 180 L 10 # [164]**

Dawe, Piers Nvidia

**Comment Type E**  **Comment Status A** (bucket1)

32.8 PMA Functional Block Diagram

**SuggestedRemedy**

32.8 PMA functional block diagram - 3 figures

**Response**  **Response Status C**

ACCEPT IN PRINCIPLE.

In the titles for Figure 173-3, 173-4 and 173-5, change from: "Functional Block Diagram" to "functional block diagram"

**Comment ID 165**

**Cl 173 SC 173.4.1 P 183 L 44 # [165]**

Dawe, Piers Nvidia

**Comment Type E**  **Comment Status A** (bucket1)

The next sentence says "at the service interface below the PMA"

**SuggestedRemedy**

So, this one should say "at its service interface"

**Response**  **Response Status C**

ACCEPT IN PRINCIPLE.

Replace the text in 173.4.1 with the following splitting the text into two paragraphs:

"If the interface between the PMA client and the PMA is physically instantiated as 800GAUI-8, the PMA shall meet the electrical and timing specifications as specified in Annex 120F or Annex 120G as appropriate at the service interface.

If the interface between the sublayer below the PMA and the PMA is physically instantiated as 800GAUI-8, the PMA shall meet the electrical and timing specifications as specified in Annex 120F or Annex 120G as appropriate at the service interface below the PMA."

[Editor's note: page was changed from 180 to 183.]
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>P802.3df D1.0 1st Task Force review comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>#166</td>
<td><strong>Cl 173 SC 173.4.2.1 P 184 L 10</strong></td>
</tr>
<tr>
<td></td>
<td>Dawe, Piers Nvidia</td>
</tr>
<tr>
<td></td>
<td><strong>Comment Type</strong> TR <strong>Comment Status</strong> R <strong>PCSL interleaving (CC)</strong></td>
</tr>
<tr>
<td></td>
<td>This additional constraint provides a very modest benefit that is judged not necessary in 400G Ethernet. However, the rare but much more harmful &quot;clock content&quot; (transition density) issue that was discovered late in P802.3bs should now be outlawed. There are many easy ways to do this.</td>
</tr>
<tr>
<td></td>
<td><strong>SuggestedRemedy</strong></td>
</tr>
<tr>
<td></td>
<td>Make this a recommendation &quot;It is recommended that each of the 8 output lanes contain two unique PCSLs from PMA client lanes i = 0 to 15 and two unique PCSLs from PMA client lanes i = 16 to 31&quot;.</td>
</tr>
<tr>
<td></td>
<td>Add constraint: &quot;The arrangement of lanes and their skew shall ensure that the reduced transition density described at the end of 120.5.2 does not occur.&quot;</td>
</tr>
<tr>
<td></td>
<td><strong>Response</strong> Response Status C REJECT.</td>
</tr>
<tr>
<td></td>
<td>The constrained PCS multiplexing specified in Clause 173 is consistent with slides 17 and 18 in the adopted PCS/PMA baseline (<a href="https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf">https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf</a>).</td>
</tr>
<tr>
<td></td>
<td>There is no evidence that clock content is worse than for four-lane 400GBASE-R PMDs lanes. We are not aware of any harmful issues with four-lane 400GBASE-R PMDs due to clock content.</td>
</tr>
<tr>
<td></td>
<td>Although some analysis has shown the possibility of reduced clock content, no evidence has been provided to justify further constraints.</td>
</tr>
</tbody>
</table>

| #167       | **Cl 173 SC 173.4.2.2 P 184 L 37**          |
|            | Dawe, Piers Nvidia                          |
|            | **Comment Type** TR **Comment Status** R **PCSL interleaving (CC)** |
|            | This is a PMA. On the receive side, it doesn't know and can't control the PCSLs of the signals it carries. |
|            | **SuggestedRemedy** |
|            | Replace this with a practical criterion to ensure that the reduced transition density doesn't happen, if any is needed, e.g. that each of the 8 outputs is derived from four contiguous lanes in the set of 32 incoming PMA lanes. There is negligible benefit in the 4-FEC multiplexing on the receive side because there are only PMAs that can make more errors after this, and their maximum error ratios are far lower than the PMD's. |
|            | **Response** Response Status C REJECT. |
|            | The issue described in the comment is not correct. |
|            | Subclause 173.4.2.2 is specifically referring to the 8:32 PMA, which is always co-located with a PHY 800GX5 below it (see 173.1.4). In the receive direction, this PMA receives 32 parallel bit streams from the PHY 800GX5. Each one of the 32 bit streams is a specific and known PCSL. The PMA is therefore able to identify the specific PCSLs it is receiving from the PHY 800GX5 (from the "PHY_XS:IS_UNITDATA_0:31.indication" service interface primitive) and arrange them appropriately. |
|            | This receive direction of the 8:32 PMA is functionally identical to the transmit direction of the 32:8 PMA, where the 32:8 PMA receives 32 parallel bit streams from the 800GBASE-R PCS above it. |
|            | The constrained PCSL multiplexing can thus be performed in accordance with slides 17 and 18 in the adopted PCS/PMA baseline (https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf). |
|            | The clock content mentioned in the suggested remedy are addressed in comments #166, 169, 126, and 127. |

| #168       | **Cl 173 SC 173.4.2.3 P 185 L 2**          |
|            | Dawe, Piers Nvidia                          |
|            | **Comment Type** E **Comment Status** A (bucket1) |
|            | This can be made clearer. |
|            | **SuggestedRemedy** |
|            | Change "lane shall be mapped together to an output lane" to "lane shall be mapped to the same output lane" |
|            | **Response** Response Status C ACCEPT. |

---

**Comment ID** 168  
**Comment ID** 167  
**Comment ID** 168  
**Comment ID** 168  
**Page 38 of 47**  
**Type:** TR/technical required  
**ER/editorial required**  
**GR/general required**  
**T/technical**  
**E/editorial**  
**G/general**  
**Comment Status:** D/dispatched  
**A/accepted**  
**R/rejected**  
**RESPONSE STATUS:** O/open  
**W/written**  
**C/closed**  
**Z/withdrawn**  
**SORT ORDER:** Comment ID  
**2022-12-08 1:09:00 PM**
IEEE P802.3df D1.0 1st Task Force review comments

**Comment ID 169**

**Dawe, Piers**

**Comment Type**: TR  **Comment Status**: R

**Comment**: PCSL interleaving (CC)

"The order of PCSLs from an input lane does not have to be maintained on the output lane"

**Suggested Remedy**

Is this enough to exclude the reduced transition density issue? If not, it can be tightened to require the lanes remain in the same or reversed order, not re-ordered about any old how.

**Response**

REJECT.

Resolve using the response to comment #166.

**Comment ID 170**

**Dawe, Piers**

**Comment Type**: E  **Comment Status**: R

"group of PMAs" puzzled me. PMAs are not used in parallel.

**Suggested Remedy**

Change group to series, or sequence

**Response**

REJECT.

The wording is consistent with similar subclauses in multiple clauses in the base standard and is accurate as written. The proposed changes do not improve the accuracy or clarity of the text.

**Comment ID 171**

**Dawe, Piers**

**Comment Type**: E  **Comment Status**: A

As I think 120 doesn't address precoding

**Suggested Remedy**

Does 120.5.11.2 need updating or is there a place in 135 that addresses it?

**Response**

ACCEPT IN PRINCIPAL.

The base standard is ambiguous about whether precoding should be applied to the PAM4 patterns specified in 120.5.11.2. All patterns other that PRBS31Q are used only in transmitter tests and thus should be used without precoding enabled. The PRBS31Q pattern, which is specified for receiver stress testing, may be used with or without precoding based on AUI or PMD type and the receiver preference.

Implement the changes on slide 16 of the following presentation:


**Comment ID 172**

**Dawe, Piers**

**Comment Type**: T  **Comment Status**: R

"Mapping of MDIO control variables to PMA control variables is shown in Table 173–2. Mapping of MDIO status variables to PMA status variables is shown in Table 173–3." But status and control go in opposite directions.

**Suggested Remedy**

Mapping of PMA status variables to MDIO status variables is shown in Table 173–3. Similarly in next sentence.

**Response**

REJECT.

The wording is consistent with similar subclauses in multiple clauses in the base standard and is accurate as written. The proposed changes do not improve the accuracy or clarity of the text.
IEEE P802.3df D1.0 1st Task Force review comments

Cl 173 SC 173.5 P 189 L 9 # 173
Cl 120F SC 120F P 198 L 8 # 174

Dawe, Piers Nvidia

Comment Type E Comment Status A
Cl 173 SC 173.5 P 189 L 9 # 173
Dawe, Piers Nvidia

Comment Type E Comment Status A
Cl 120F SC 120F P 198 L 8 # 174

Comment Type E Comment Status A
Cl 173 SC 173.5 P 189 L 9 # 173

PRBS Tx pattern testing error counter

SuggestedRemedy

PRBS Tx pattern testing error counter

Response

ACCEPT IN PRINCIPLE.
Change "PRBS Tx pattern testing" to "PRBS Tx pattern testing error counter, lane 0 to lane 7"
Change "PRBS Rx pattern testing" to "PRBS Rx pattern testing error counter, lane 0 to lane 7"

Comment ID 174 Page 40 of 47

Comment ID 174

Response

ACCEPT IN PRINCIPLE.

The titles are indeed long and can be shortened and clarified.

The suggested remedy introduces the word "Type", which has been used for PHY but not for AUIs. Therefore a slight modification is proposed. The same form used for PMD clause titles can be used.

Change the title of Annex 120F to:
"Chip-to-chip Attachment Unit Interfaces 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C"

Change the title of Annex 120G to
"Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M"

Change the titles of 120F.5, 120F.5.4, 120G.6, 120G.6.4, the text in 120F.5.1 and 120G.6.1, and the tables in 120F.5.2.2 and 120G.6.2.2, accordingly.

Change any text affected by these title changes with editorial license.
IEEE P802.3df D1.0 1st Task Force review comments

C1 120F SC 120F.1 P 199 L 9 # 175
Dawe, Piers Nvidia
Comment Type E Comment Status A precoding (CC)
120.5.7.2 doesn't address precoding in C2C
SuggestedRemedy
Delete the reference here or change 120.5.7.2
Response Response Status C
ACCEPT IN PRINCIPLE.
The content of 120.5.7.2 is not sufficiently complete for 800 Gb/s Ethernet AUIs and PMDs.
Implement the changes on slides 14 and 15 of the following presentation:
Add references to 173.4.7.2 where appropriate.
Implement with editorial license.

C1 120G SC 120G.1 P 204 L 44 # 176
Dawe, Piers Nvidia
Comment Type E Comment Status A (bucket1)
Each 100GAUI-1, 200GAUI-2, 400GAUI-4 C2M, "and" 800GAUI-8 C2M data path contains one, two, four, "or" eight differential lanes
SuggestedRemedy
Change and to or
Response Response Status C
ACCEPT.

C1 120G SC 120G.2 P 207 L 8 # 177
Dawe, Piers Nvidia
Comment Type E Comment Status A test points
As dealing with larger numbers of lanes in compliance boards is an engineering issue...
And by the way, it might have been helpful to show that these are differential.
SuggestedRemedy
It would help to add the short diagonal lines showing n lanes. Also Figure 120G-4
Response Response Status C
ACCEPT IN PRINCIPLE.
The test points are separate for each lane. However, the clarity of the figure may be improved.
Add the label "(one per lane)" below TP1a and TP4a in Figure 120G-3, and below TP1 and TP4 in Figure 120G-4.
In the second and third paragraphs of 120G.2, change "the location of compliance points" to "the location of compliance points for each lane".

C1 FM SC FM P 8 L 12 # 178
Dawe, Piers Nvidia
Comment Type E Comment Status A (bucket1)
Task Force name Task Force
SuggestedRemedy
Task Force 3 times
Response Response Status C
ACCEPT.
Delete "Task force name", three instances
Also, add list of clause editors.
Implement with editorial license.
[Editor's note: The page/line were change from 1/8 to 8/12.]
Comment: "distributed in a round-robin fashion into two parallel transmit functions": sort of slang. Where I come from, all robins look round.

Suggested Remedy: Change "a round-robin fashion" to "an alternating fashion" here; in 172.2.4.1, change "a round robin fashion" to "an alternating fashion". Similarly in 172.2.5.8.

Response: ACCEPT IN PRINCIPLE.

This is a new function where 64B/66B blocks are distributed between or combined from two streams or flows, so "alternating" seems more appropriate here than "round-robin". The details of the distribution are not necessary in the summary, but in the detailed functional description "round-robin" should be replaced with "alternating".

In 172.2.1 on page 163 line 19...
Change: "The 66-bit blocks are then distributed in a round-robin fashion into two parallel transmit functions, referred to as flow 0 and flow 1."
To: "The 66-bit blocks are then distributed between two parallel transmit functions, referred to as flow 0 and flow 1."

In 172.2.1 on page 163, line 42
Change: "A 66-bit block collection function merges the 66-bit blocks from the two flows in a round-robin fashion into a single stream of blocks that are then 64B/66B decoded."
To: "A 66-bit block collection function merges the 66-bit blocks from the two flows into a single stream of blocks that are then 64B/66B decoded."

In 172.2.4.1 on page 164, line 23...
Change: "The 66-bit blocks are distributed to the two flows in a round robin fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue the round robin distribution procedure across the two flows."
To: "The 66-bit blocks are distributed to the two flows in an alternating fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue the distribution procedure across the two flows."

In 172.2.5.8 on page 168, line 21
Change: "The block collection reverses the block distribution done in the transmitter (see 172.2.4.1) by combining the 66-bit blocks from the two flows in a round robin fashion to form a single stream of 66-bit blocks."
To: "The block collection reverses the block distribution done in the transmitter (see 172.2.4.1) by combining the 66-bit blocks from the two flows in an alternating fashion to form a single stream of 66-bit blocks."

Comment: "Within each flow, the 66-bit blocks are transcoded to 257-bit blocks, scrambled, and alignment markers are periodically added to the data stream."

Suggested Remedy: Modify this to say that the insertion of alignment markers is not independent for each flow.

Response: ACCEPT IN PRINCIPLE.

The response to comment #90 modifies the text in 172.2.4.4 (Alignment marker mapping and insertion) to clarify the rules for the alignment marker insertion in the two flows, and makes it very clear that the alignment marker insertion is not independent for each flow.

Section 172.2.1 (the subject of this comment) is a high level functional overview of the PCS. It would be useful to introduce that the alignment marker insertion in the two flows is not independent as part of this high level overview.

With editorial license add text to section 172.2.1 to introduce that the alignment marker insertion in the two flows are not independent.
The data stream is distributed to two 5140-bit blocks and then FEC encoded. The two FEC codewords are then interleaved before data is distributed to individual PCS lanes.

**Suggested Remedy**

For each flow, the data stream is distributed to two 5140-bit blocks and then FEC encoded. For each flow, the two FEC codewords are then interleaved before data is distributed to individual PCS lanes.

**Response**

Accept in principle.

Replace

"The data stream is distributed to two 5140-bit blocks and then FEC encoded. The two FEC codewords are then interleaved before data is distributed to individual PCS lanes."

with

"For each flow, the data stream is distributed to two 5140-bit blocks and then FEC encoded. For each flow, the two FEC codewords are then interleaved before data is distributed to individual PCS lanes."

The curly brackets must be trying to tell the reader something, but I don't know what.

**Suggested Remedy**

Delete them, or define what they mean, or change to some notation that is defined.

**Response**

Reject.

The curly brackets in Tables 172-1 and 172-2 are consistent with what was used in Table 119-2 in Clause 119. Given that we are striving for consistency between this new and previous PCS specifications, retaining a common format is helpful for comparison.

The comment does not provide sufficient justification to make the suggested change nor do the proposed changes improve clarity or accuracy of the draft.

Two fifths of this table is useless clutter, and it would be good to use spaces in the normal way.

**Suggested Remedy**

Change

0x9A,0x4A,0x26,0xB6,0x65,0xB5,0xD9,0xD9,0xFE,0x71,0xF3,0x26,0x01,0x8E,0x0C

to

9A, 4A, 26, B6, 65, B5, D9, D9, FE, 71, F3, 26, 01, 8E, 0C

and so on. In the text, say that these are in hex. Similarly in Table 172-2.

**Response**

Accept in principle.

Update the format in Table 172-1 and Table 172-2 to use fixed width font.

There was no consensus to make any other changes.
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Page</th>
<th>Comment and Response</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>185</td>
<td></td>
<td>Comment Type: T, Comment Status: A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Careful, “function” has a precise meaning in PCS clauses. This can be more specific and informative.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Suggested Remedy: Change “The functions … are” to “the 64B/66B encoder … is”</td>
<td></td>
</tr>
<tr>
<td>186</td>
<td></td>
<td>Comment Type: E, Comment Status: A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>“Test-pattern generators are identical to that specified in 119.2.4.9” there is only one test pattern, and although it is generated in an analogous way to 119.2.4.9, it’s a different PCS and different bits in the pattern.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Suggested Remedy: Change to “A scrambled idle test pattern can be generated in the same way in the same way as in 119.2.4.9”.</td>
<td></td>
</tr>
<tr>
<td>187</td>
<td></td>
<td>Comment Type: E, Comment Status: A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The relation between hi_ser_0, hi_ser_1 and hi_ser appears later within a state machine variable definition, which is too obscure. More generally, I could not find where the purpose of hi_ser is introduced.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Suggested Remedy: Add something in regular text (possibly elsewhere) that says that what hi_ser for, and that it is the OR of hi_ser_0 and hi_ser_1.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Response: ACCEPT IN PRINCIPLE.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Update draft to clarify the use of hi_ser in in each flow versus at the top level.</td>
<td></td>
</tr>
<tr>
<td>188</td>
<td></td>
<td>Comment Type: E, Comment Status: A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This says “See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules” but those subclauses are titled “119.2.3.5 Idle (/I/)” and “119.2.3.8 Ordered set (/O/)” and the content isn’t there so the reader doesn’t know to look there, or follow the links from there to 83 to find the deletion and insertion rules.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Suggested Remedy: Improve the titles of those subclauses: ”Idle (/I/) and idle insertion and deletion” and ”Ordered set (/O/) and ordered set deletion”</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Response: REJECT. 119.2.3.5 and 119.2.3.8 have links to 82.2.3.6 and 82.2.3.9 respectively, which the reader can follow to access the rules for insertion/deletion. Note that this double-reference is common throughout many subclauses in Clause 172. The proposed changes do not improve the accuracy of the draft.</td>
<td></td>
</tr>
</tbody>
</table>

**Comment ID 185**

**Comment ID 186**

**Comment ID 187**

**Comment ID 188**
**IEEE P802.3df D1.0 1st Task Force review comments**

<table>
<thead>
<tr>
<th>CI 172</th>
<th>SC 172.3.5</th>
<th>P 173</th>
<th>L 31</th>
<th># 189</th>
</tr>
</thead>
<tbody>
<tr>
<td>Davie, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment Type**: TR

**Comment Status**: A

**Suggested Remedy**

I could not find FEC_cw_counter in the base document (802.3-2022 Section 8) or the PCS baseline shrhikande_3df_01a_221004, and in 802.3ck it's for RS-FEC-Int (for 100GBASE-P PHYs 100GBASE-KR1 and 100GBASE-CR1) only. It's not applicable to any 200G or 400G, which is what the 800G PCS is based on. The same applies to 172.3.5 FEC_codeword_error_bin_i, I think.

**Response**

ACCEPT IN PRINCIPLE.

The counters were added even though they are not part of the adopted PCS baseline.

Based on straw poll #3 there is consensus to retain the FEC bin counters in the draft. Based on straw poll #4 there is more support for making these counters optional rather than mandatory.

There is consensus after the straw polls to leave the counters in the draft and to make them optional.

Reword the draft to indicate that the counters are optional.

**Straw poll #3 (directional)**

I support keeping the FEC bin counters (FEC_codeword_error_bin_i) and FEC cw counter (FEC_cw_counter) currently defined in 172.3.6 and 172.3.5 respectively.

Y:61
N:1

**Straw poll #4 (directional)**

I support the FEC bin counters (FEC_codeword_error_bin_i) and FEC cw counter (FEC_cw_counter) currently defined in 172.3.6 and 172.3.5 respectively, being:

A: Mandatory
B: Optional
C: Need more information
A:25, B:36, C:7

<table>
<thead>
<tr>
<th>CI 173</th>
<th>SC 173.1.4</th>
<th>P 177</th>
<th>L 28</th>
<th># 190</th>
</tr>
</thead>
<tbody>
<tr>
<td>Davie, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment Type**: T

**Comment Status**: A

"A ... PMA is required to support an physical instantiation of the PMA service interface":

doesn't make sense, as the PMA service interface is part of the PMA. an vs. a.

**Suggested Remedy**

is used to implement a ...?

**Response**

ACCEPT IN PRINCIPLE.

Change from:

"An 8:8 PMA is required to support an physical instantiation of the PMA service interface (800GAUI-8)" to

"An 8:8 PMA is required for a physical instantiation of the PMA service interface (800GAUI-8)"

<table>
<thead>
<tr>
<th>CI 173</th>
<th>SC 173.2</th>
<th>P 178</th>
<th>L 51</th>
<th># 191</th>
</tr>
</thead>
<tbody>
<tr>
<td>Davie, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Comment Type**: T

**Comment Status**: A

"The PMA receives": confusing and incomplete.

**Suggested Remedy**

In the transmit direction, the PMA receives 32 parallel bit streams, each at the nominal signaling rate of the PCSL. In the receive direction, it delivers 32 parallel bit streams to its client. Similarly in the next paragraph for an 8-lane interface.

**Response**

ACCEPT IN PRINCIPLE.

Change from:

"The PMA receives 32 parallel bit streams, each at the nominal signaling rate of the PCSL." to

"In the transmit direction, the PMA receives 32 parallel bit streams from either the 800GBASE-R PCS or the DTE 800GXS, each at the nominal signaling rate of the PCSL. In the receive direction, the PMA sends 32 parallel bit streams to the PMA client, each at the nominal signaling rate of the PCSL."

Change from:

"The PMA receives PAM4 symbols on each of its input lanes at two times the PCSL rate, each symbol formed from two bits." to

"In the transmit direction, the PMA receives 8 parallel PAM4 symbol streams from the PMA client, each operating at a nominal signaling rate of 53.125 Gbd. In the receive direction, the PMA sends 8 parallel PAM4 symbol streams to the PMA client, each at a nominal signaling rate of 53.125 Gbd."
Table 167-7. The order of the PMDs in the "Signaling rate" row is different from what was done in Clause 124.

**Suggested Remedy**
Proposing to reorder the data in this row to put the lower speed and lower lane count PMDs first, i.e.
"Other PMDs"
"800GBASE-VR8, 800GBASE-SR8 PMDs"

**Response**
ACCEPT IN PRINCIPLE.
Change the order and associated parameters as proposed.

Table 167-8. The order of the PMDs in the "Signaling rate" row is different from what was done in Clause 124.

**Suggested Remedy**
Proposing to reorder the data in this row to put the lower speed and lower lane count PMDs first, i.e.
"Other PMDs"
"800GBASE-VR8, 800GBASE-SR8 PMDs"

**Response**
ACCEPT IN PRINCIPLE.
Change the order and associated parameters as proposed.

800GXS should be 400GXS

**Suggested Remedy**
Change
"PCS and 800GXS sublayers specified in 118.2" to
"PCS and 400GXS sublayers specified in 118.2"

**Response**
ACCEPT.
IEEE P802.3df D1.0 1st Task Force review comments

Comment Type T  Comment Status A  PMA SI
Figure 173-4 (8:32 PMA) there should be no PMA:IS_SIGNAL.indication towards the PMA (AUI is not able to transfer an out of band status signal) and possibly no "SIL" block in the block diagram.

The same comment applies to the 8:8 PMA in Figure 173-5.

Suggested Remedy
Remove the PMA:IS_SIGNAL.indication signal and the "SIL" block from Figure 173-4 and Figure 173-5.

Response  
ACCEPT IN PRINCIPLE.

Comments #196, #197, #162 and #29 (and further review by the editorial team), identified several issues related to the service interface definition (and associated diagrams) for both the PMA and XS sublayers.

Slides 44 to 54 in the following presentation were reviewed by the task force: https://www.ieee802.org/3/df/public/22_12/brown_3df_03c_2212.pdf

Implement the following changes in the draft with editorial license:

Update Figure 173-3, Figure173-4 and Figure 173-5 with the corresponding figures shown in slides 48-50 of https://www.ieee802.org/3/df/public/22_12/brown_3df_03c_2212.pdf, and update any associated text accordingly.

Update Clause 171 according to slides 51 and 52 of https://www.ieee802.org/3/df/public/22_12/brown_3df_03c_2212.pdf, add DTE 800GXS and PHY 800GX5 service interface definitions, and update any associated text accordingly.

Update Figure 169-3 based on slide 53 of https://www.ieee802.org/3/df/public/22_12/brown_3df_03c_2212.pdf, and update any associated text accordingly.

Comment Type E  Comment Status A  PMA SI
Figure 173-3/4/5/. Need to make it clear if the sublayer above or below is another PMA, that the interface is connected over a physically instantiated AUI (800GAUI-8)

SuggestedRemedy
Update Figure 173-3/4/5 to make it clear if the sublayer above or below is another PMA, that the interface is connected over a physically instantiated AUI (800GAUI-8)

Response  
ACCEPT IN PRINCIPLE.
Resolve using the response to comment #196.

Comment Status A  Response Status C
Nicholl, Gary  Cisco Systems

Comment ID 197
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