### Comment 1

**Identified**

45.2.4 PHY XS registers and 45.2.5 DTE XS registers subsections need to be brought into the 802.3df draft and modifications made to increase the number of service interface lanes specified from 20 to 32.

**Suggested Remedies**

Update "Table 45–314—PHY XS registers" and "Table 45–339—DTE XS registers" and relevant sunclauses to address this. This will include an extra "XS alignment status 5" register at location 54, adding extra "XS lane mapping" registers above 415, adding extra "FEC symbol error counter" registers above 631, and add bit 4.801.6 for "Local degraded SER received."

**Proposed Response**

PROPOSED ACCEPT.

**Response Status**

W

---

### Comment 2

**Identified**

"The alignment marker removal is identical to that of the 400GBASE-R PCS in 119.2.5.5." - but there are 32 AMs, so it can't be identical.

**Suggested Remedies**

Make the necessary changes to the text (add exceptions or "for each flow").

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

**Response Status**

W

---

### Comment 3

**Identified**

Numbers above 10 should not be spelled out.

**Suggested Remedies**

change "thirty two" to "32".

**Proposed Response**

PROPOSED ACCEPT.
The restriction for the 32:8 multiplexing is intended to improve the FEC performance with correlated errors. The analysis was done with an AB/CD muxing scheme where one UI has bits from codewords A and B (flow 0) and the following UI has bits from C and D (flow 1). This way, combined with the checkerboard scheme, spreads the errors in a burst across the four codewords with equal probabilities.

The restriction as written does not preclude a different muxing, AC/BD, where one UI has bits from A and C and the following UI has bits from B and D. For example, muxing bits from lanes 0 and 16 as MSB+LSB in one UI and bits from lanes 1 and 17 as MSB+LSB in the next UI.

Since the checkerboard pattern swaps codewords A/B on each pair of lanes in flow 0, and swaps codewords C/D on each pair of lanes in flow 1, this would result in always taking the MSB for the LSB is twice that of the MSB, this would make flow 1 have an increased BER: it would get 2/3 of the errors (33% higher BER than with the AB/CD muxing).

If this muxing is performed, the result would be an increased FLR (by 1-2 orders of magnitude) compared to 400GBASE-R, just due to sub-optimal muxing - regardless of whether errors are correlated or not!

This degradation can be prevented by adding a restriction that two bits from each flow create one PAM4 symbol.

SuggestedRemedy
Change the second item of the first list in 173.4.2.1 from "The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from PMA client lanes i = 0 to 15 and two unique PCSLs from PMA client lanes i = 16 to 31" to "The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from PMA client lanes i = 0 to 15 encoded as one PAM4 symbol, and two unique PCSLs from PMA client lanes i = 16 to 31 encoded as the subsequent PAM4 symbol (see 173.4.7)."

Make a similar change in the second item of the second list in 173.4.2.2 (which has "service interface lanes" instead of "PMA client lanes").

Also, change the second item of the list in 173.4.2.3 from "The 4 PCSLs received on any input lane shall be mapped together to an output lane. The order of PCSLs from an input lane does not have to be maintained on the output lane." to "The 4 PCSLs received on any input lane shall be mapped together to an output lane, maintaining the bit pairs encoded on each PAM4 symbol. Other than that, the order of PCSLs from an input lane does not have to be maintained on the output lane."
Comment ID: 11

Comment Type: TR/technical required

Comment Status: D/dispatched

Response Status: W/written

Comment

"Alignment marker encoding values for flow 1 are specified in Table 172–2 and the variable x in 119.2.4.4.2 takes the values of PCS lane number minus 16."

In 119.2.4.4.2, x is used as part of the variable am_. We have 32 distinct alignment markers, for lanes 0 through 31, so assigning x to "lane number minus 16" would result in am_0 through am_15 assigned twice, and am_16 through am_31 not assigned at all.

Instead, we should specify that for flow 1, AM are constructed per 119.2.4.4.2 but with x taking values from 16 to 31, and the variable j used in the mapping procedure takes values from 8 to 16 (instead of 0 to 7).

This difference may be listed as another exception, but it seems that it makes it worthwhile to have a new subclause for creating the 32 AMs.

Suggested Remedy

Replace the reference to 119.2.4.4.2 with a full specification of AM creation and insertion, based on the content (text and equations) of 119.2.4.4.2, but with AMs for lanes 16 to 31 constructed as in the comment.

Proposed Response

PROPOSED REJECT.

Each Flow is a unique "instance" of the 119.4.4.2 so the fact that there are 2 copies of variable "am_#", one in Flow0 and another in Flow1 that have different values is how it's intended to be specified.

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using response to comment #185.

Comment ID: 11

Comment Type: TR/technical required

Comment Status: D/dispatched

Response Status: W/written

Comment

In the baseline proposal https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf, slide 10, it is written that "AM insertion is aligned across the two flows".

I do not see that requirement in clause 172. The text in 172.2.4.4 does not preclude inserting AM blocks independently in each flow.

Suggested Remedy

If the subclause specifying AM creation is updated to include full text, this requirement can be included in it (a similar statement exists in 119.2.4.4.2 for the 16 lanes).

Otherwise, add this requirement as another exception, with editorial license.

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #90.
**Proposed Response #12**

**Cl 172 SC 172.2.5.4 P 168 L 5 # 12**

Ran, Adee
Cisco

**Comment Type:** TR  
**Comment Status:** D (bucket1)

"The post-FEC interleave is identical to that specified in 119.2.5.4."

But 119.2.5.4 talks specifically about two FEC codewords, and we have four.

In similar subclauses for the transmit functions, the text includes "for each flow".

Also applies to 172.2.5.6 and 172.2.5.7.

**Suggested Remedy**

Insert "for each flow" after "interleave".

Make similar changes in 172.2.5.6 and 172.2.5.7, with editorial license.

**Proposed Response**  
**Response Status:** W

PROPOSED ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.

---

**Proposed Response #13**

**Cl 124 SC 124.8.5a P 76 L 16 # 13**

Dudek, Mike
Marvell

**Comment Type:** T  
**Comment Status:** D (bucket1)

800GBASE-DR4 is not part of this specification

**Suggested Remedy**

Change to 800GBASE-DR8  Also on line 25 and page 77 line 29

**Proposed Response**  
**Response Status:** W

PROPOSED ACCEPT IN PRINCIPLE.

Change 800GBASE-DR4 to 800GBASE-DR8

---

**Proposed Response #14**

**Cl 124 SC 124.11.3.1 P 80 L 34 # 14**

Dudek, Mike
Marvell

**Comment Type:** T  
**Comment Status:** D (bucket1)

The optical lane assignments are wrong in figure 124-6.

**Suggested Remedy**

Change them to match Figure 124-6 in the base document.

**Proposed Response**  
**Response Status:** W

PROPOSED ACCEPT IN PRINCIPLE.

Check and update figure with editorial license
IEEE P802.3df D1.0  1st Task Force review comments

Cl 30  SC 30.5  P33  L 45  # 16
Dudek, Mike  Marvell

Comment Type  T  Comment Status  D  (bucket1)

The base standard and 802.3db all list the "with reach up to at least xxx." to differentiate between the various Phy’s. This draft does not.

SuggestedRemedy
Add the reach information to the new Phys.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.

change 400GBASE-DR4 description to:
"400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD with reach up to at least 500 m as specified in Clause 124"

change 400GBASE-DR4-2 description to:
"400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 124"

change 800GBASE-DR4 description to:
"800GBASE-R PCS/PMA over 8-lane single-mode fiber PMD with reach up to at least 500 m as specified in Clause 124"

change 800GBASE-DR4-2 description to:
"800GBASE-R PCS/PMA over 8-lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 124"

change 800GBASE-SR8 description to:
"800GBASE-R PCS/PMA over 8-lane multimode fiber PMD with reach up to at least 100 m as specified in Clause 167"

change 800GBASE-VR8 description to:
"800GBASE-R PCS/PMA over 8-lane multimode fiber PMD with reach up to at least 50 m as specified in Clause 167"

Implement with editorial license.

Cl 45  SC 45.2.1.8  P38  L 13  # 17
Dudek, Mike  Marvell

Comment Type  E  Comment Status  D  (bucket1)

In table 45-12 "and" is used in the list for BR but it has been deleted for KR and CR. The table should be consistent for all rows.

SuggestedRemedy
Add the "and" before 800.

Proposed Response  Response Status  W
PROPOSED ACCEPT.

Cl 45  SC 45.2.1.23  P39  L 24  # 18
Dudek, Mike  Marvell

Comment Type  T  Comment Status  D  (bucket1)

This is listing register 1.72 but 45.2.1.60b is listing the abilities in Register 1.73

SuggestedRemedy
Change to register 1.72. Also on line39

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #44

Cl 45  SC 45.2.1.161  P41  L 34  # 19
Dudek, Mike  Marvell

Comment Type  T  Comment Status  D  (bucket1)
The mapping of lanes 4-7 is not provided.

SuggestedRemedy
Add the mapping for those lanes. Also in 45.2.1.163 on line 50, 45.2.1.165 and 45.2.1.167

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #45
There are 4 cable assembly types

Change "three" to "four"

PROPOSED ACCEPT.

Should be 800GASE-KR8 not KR4

fix it.

PROPOSED ACCEPT.

should be 800GBASE-CR8 not KR8

Change it.

PROPOSED ACCEPT.

In figure 124-6 the labels are all squeezed together

Spread the TX/RX labels to the right position

PROPOSED ACCEPT IN PRINCIPLE.

"have" should be "has" ("or" makes it singular)

change it.

PROPOSED ACCEPT IN PRINCIPLE.

Replace "PMD have eight" with "PMD has eight".

"Manageable Device (MMD) addresses 1 and 8"

"Manageable Device (MMD) addresses 1, 8, 9, 10 and 11"

"1 and 8" to "1, 8, 9 and 10".

PROPOSED ACCEPT IN PRINCIPLE.

should be "a physical instantiation"

Change "an" to "a"

PROPOSED ACCEPT.

There are more than just two addresses (1 and 8) available for the MMD. (more are shown in figure 173-2)

Change from: "Manageable Device (MMD) addresses 1 and 8" to "Manageable Device (MMD) addresses 1, 8, 9, 10 and 11"

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #14
IEEE P802.3df D1.0  1st Task Force review comments

CI  172  SC  172.2.4.9  P  167  L  25  #   27   Bruckman, Leon  Huawei
   Comment Type  T   Comment Status  D   test pattern (CC)
   I assume test pattern shall be applied to both flows together
   SuggestedRemedy
   It may be beneficial to note that the test function when activated affects both flows
   Proposed Response   Response Status  W
   PROPOSED REJECT.
   The PCS has a single scrambled idle test pattern generator, same as 119.2.4.9. The
   scrambled idle test pattern is generated by the Encoder prior to 66-bit block distribution.

CI  172  SC  172.2.6.2.4  P  170  L  15  #   28   Bruckman, Leon  Huawei
   Comment Type  T   Comment Status  D   (bucket1)
   From this clause it may be implied that counters are not aggregated, but in the MDIO Table
   172-4 shows (and text indicates that) they are aggregated
   SuggestedRemedy
   Add exception indicating that counters are the aggregate of both flows
   Proposed Response   Response Status  W
   PROPOSED REJECT.
   172.2.6.2.4 is defining the counters used in the state diagrams. The definition of these
   counters is identical to that in 119.2.6.2.4. Therefore, these counters are not aggregated
   and are not the same as those defined in Table 172-4.

CI  173  SC  173.2  P  179  L  10  #   29   Bruckman, Leon  Huawei
   Comment Type  T   Comment Status  D   PMA S/
   "In the case where the sublayer below the PMA is a PHY 800GXS the PMA does not
   receive a PHY_XS:IS_SIGNAL.indication as an input to the SIL". Figure 173-4 that
   describes this interface does include the PHY_XS:IS_SIGNAL.indication
   SuggestedRemedy
   Update Figure 173-4 according to text
   Proposed Response   Response Status  W
   PROPOSED ACCEPT IN PRINCIPLE.
   Resolve using the response to comment #196.

CI  45  SC  45.2.1.165  P  42  L   8  #   30   Huber, Tom  Nokia
   Comment Type  T   Comment Status  D   (bucket1)
   While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe
   the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how
   the mapping works for all bits would be better and easier to maintain.
   SuggestedRemedy
   Change "Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to
   register 1.1322, and lane 3 maps to register 1.1323."
   to
   "Lanes 0-7 map to registers 1.1320 to 1.1327, respectively."
   Proposed Response   Response Status  W
   PROPOSED ACCEPT.

CI  45  SC  45.2.1.167  P  42  L   23  #   31   Huber, Tom  Nokia
   Comment Type  T   Comment Status  D   (bucket1)
   While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe
   the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how
   the mapping works for all bits would be better and easier to maintain.
   SuggestedRemedy
   Change "Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to
   register 1.1422, and lane 3 maps to register 1.1423."
   to
   "Lanes 0-7 map to registers 1.1420 to 1.1427, respectively."
   Proposed Response   Response Status  W
   PROPOSED ACCEPT.
While the mapping of registers to what they control is obvious, it would be better to spell it out a bit more completely to maintain similar structure to the other clauses that are specifying registers per-lane.

**Suggested Remedy**

Change "Register 1.1450 controls the PMD training pattern for PMD lane 0; register 1.1451 controls the PMD training pattern for PMD lane 1; etc." to "Registers 1.1450 to 1.1457 control the PMD training pattern for PMD lanes 0-7, respectively."

**Proposed Response**

PROPOSED ACCEPT.

---

The text "and 136.8.11.1.3" is in 802.3-2022, so it should not be identified as a change.

**Suggested Remedy**

Remove the underlining from this text.

**Proposed Response**

PROPOSED REJECT.

The reference to 136.8.11.1.3 is not in the base standard so the underlining should remain.

---

The last 3 sentences would be clearer if the order of the last two sentences is swapped, and the (current) last sentence is written more generically to apply to any situation where a polynomial identifier is being reused.

**Suggested Remedy**

Replace "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11. For 8-lane use cases different initial seeds should be used where the same polynomial is being reused." with "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function. If the same polynomial identifier is used for multiple lanes, different initial seeds should be used for each of those lanes. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11."

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #122.

---

Subclauses 45.2.3.24-26 all exist in 802.3-2022, so they should not be indicated as changes in the table.

**Suggested Remedy**

Remove the underlining from 45.2.3.24, 45.2.3.25, 45.2.3.26.

**Proposed Response**

PROPOSED REJECT.

Although these clauses are in the base standard, there are no references to them in Table 45-233. Therefore it is appropriate to add them to the table with underlining.
Comment ID 41

IEEE 802.3df D1.0 1st Task Force review comments

Cl 45 SC 45.2.3 P 43 L 50 # 36
Huber, Tom Nokia

Comment Type E Comment Status D (bucket1)

Subclause 45.2.3.50 exists in 802.3-2022, so it should not be indicated as a change in the table.

Suggested Remedy

Remove the underlining from 45.2.3.50

Proposed Response Response Status W

PROPOSED REJECT.
Although this subclause is in the base standard there is no reference to it in the table. Therefore it is appropriate to add it to Table 45-233 with underlining.

Cl 124 SC 124.1 P 59 L 24 # 37
Huber, Tom Nokia

Comment Type T Comment Status D (bucket1)

Table 124-1 was modified by 802.3ck-2022

Suggested Remedy

Change the editing instruction to add "(as modified by IEEE 802.3ck-2022)" and insert the rows for Annexes 120F and 120G into the table.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.
Implement proposed remedy with editorial license

Cl 124 SC 124.1 P 61 L 36 # 38
Huber, Tom Nokia

Comment Type E Comment Status D (bucket1)

Since there are only two items in the list, they should be separated with and rather than a comma

Suggested Remedy

Change "400GBASE-DR4, 400GBASE-DR4-2" to "400GBASE-DR4 and 400GBASE-DR4-2"

Proposed Response Response Status W

PROPOSED ACCEPT.
IEEE P802.3df D1.0 1st Task Force review comments

**Comment ID: 42**

**Cl 172 SC 172.1.3 P 161 L 6**

Huber, Tom Nokia

**Comment Type:** E **Comment Status:** D (bucket1)

missing "(to)" in the transcoding description in item b)

**Suggested Remedy**

- Change "Transcoding from 66-bit blocks to (from 257-bit blocks (25B/257B)" to "Transcoding from (to) 66-bit blocks to (from 257-bit blocks (25B/257B)"

**Proposed Response**

**Response Status:** W

PROPOSED ACCEPT IN PRINCIPLE.

Change from "Transcoding from 66-bit blocks to (from) 257-bit blocks (25B/257B)" to "Transcoding from (to) 66-bit blocks to (from) 257-bit blocks (25B/257B)"

---

**Comment ID: 43**

**Cl 45 SC 45.2.1.6 P 36 L 3**

Huber, Tom Nokia

**Comment Type:** E **Comment Status:** D (bucket1)

Since the table includes 400ZR as existing text, the editing instruction should note that the text shown is as modified by 802.3cw.

**Suggested Remedy**

- Add "(as modified by IEEE 802.3cw-202x)" after "Change Table 45-7"

**Proposed Response**

**Response Status:** W

PROPOSED ACCEPT.

---

**Comment ID: 44**

**Cl 45 SC 45.2.1.23 P 39 L 23**

Huber, Tom Nokia

**Comment Type:** T **Comment Status:** D (bucket1)

Register 1.72 is added by 802.3cz; presumably 1.73 is what was intended here

**Suggested Remedy**

- Change 1.72 to 1.73

**Proposed Response**

**Response Status:** W

PROPOSED ACCEPT.

---

**Comment ID: 45**

**Cl 45 SC 45.2.1.161 P 41 L 34**

Huber, Tom Nokia

**Comment Type:** T **Comment Status:** D (bucket1)

While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

**Suggested Remedy**

- Change "Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123." to "Lanes 0-7 map to registers 1.1120 to 1.1127, respectively."

**Proposed Response**

**Response Status:** W

PROPOSED ACCEPT.

---

**Comment ID: 46**

**Cl 45 SC 45.2.1.163 P 41 L 50**

Huber, Tom Nokia

**Comment Type:** T **Comment Status:** D (bucket1)

While the mapping of bits to registers is obvious, it seems incomplete to explicitly describe the mapping for bits 0-3 and say nothing at all about bits 4-7. A simpler statement of how the mapping works for all bits would be better and easier to maintain.

**Suggested Remedy**

- Change "Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223." to "Lanes 0-7 map to registers 1.1220 to 1.1227, respectively."

**Proposed Response**

**Response Status:** W

PROPOSED ACCEPT.
There is some repetition between the paragraph about the PCS Synchronization process and the paragraph about the PCS Receive process in terms of aligning, reordering, and deskewing. Per the state diagrams, the PCS synchronization process ensures that all the lanes are aligned and deskewed, and the receive process deals with decoding the 66b characters.

**Suggested Remedy**
Add a sentence to the end of the penultimate paragraph: "When all 32 lanes are aligned and deskewed, and reordered, the align_status flag is set to indicate that the PCS has obtained alignment."

Revise the first two sentences of the final paragraph as follows: "The PCS Receive process separates the reordered PCS lanes into two sets of 16 PCs lanes..."

**PROPOSED ACCEPT IN PRINCIPLE.**
Implement the suggested remedy with editorial license.

The OTN reference point needs further discussion - it would be preferable if the mapping point was 257b blocks rather than 66b blocks.

**Suggested Remedy**
Supporting presentation to be provided.

**PROPOSED REJECT.**
Pending Task Force review of supporting presentation.

To maintain parallel structure with the rest of the sentence, the new 800G AUI should be introduced as 800 Gb/s eight-lane Attachment Unit Interface

**Suggested Remedy**
change "and eight-lane Attachment Unit Interface" to "800 Gb/s eight-lane Attachment Unit Interface"

**PROPOSED ACCEPT IN PRINCIPLE.**
change "and eight-lane" to "and 800 Gb/s eight-lane".
IEEE P802.3df D1.0 1st Task Force review comments

Cl 173A SC 173A P226 L1 # 52
Huber, Tom Nokia
Comment Type E Comment Status D
The text should be referencing figure 173A-3.
SuggestedRemedy
Change 173A-4 to 173A-3.
Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 45 SC 45.2.4.4 P46 L54 # 53
Slavick, Jeff Broadcom
Comment Type T Comment Status D
(bucket1)
Need to add 800G capability register to PHY XS
SuggestedRemedy
Assign a bit in register 4.4 for 800G capable and create a description the same as the 400G bit replacing 400G with 800G
Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 45 SC 45.2.5.4 P46 L54 # 54
Slavick, Jeff Broadcom
Comment Type T Comment Status D
(bucket1)
Need to add 800G capability register to DTE XS
SuggestedRemedy
Assign a bit in register 5.4 for 800G capable and create a description the same as the 400G bit replacing 400G with 800G
Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 45 SC 45.2.5.15 P46 L54 # 55
Slavick, Jeff Broadcom
Comment Type T Comment Status D
(bucket1)
DTE XS AM lock registers need to be updated with 800G references and expanded to 32 AM lanes
SuggestedRemedy
Update (see 119.2.6.2.2) to (see 119.2.6.2.2 and 172.2.6.2.2) in 45.2.4.15.* and 45.2.4.16.* Add the extra 16 lanes of amps_lock as well as was done for the PCS registers.
Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 45 SC 45.2.5.17 P46 L54 # 56
Slavick, Jeff Broadcom
Comment Type T Comment Status D
(bucket1)
DTE XS lane mapping registers need to update with 800G references and expanded to 32 lanes
SuggestedRemedy
Bring in and update 45.2.5.17 and 45.2.5.18 adding references to Clause 171 and adding 16 more registers
Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 45 SC 45.2.5.19 P46 L54 # 57
Slavick, Jeff Broadcom
Comment Type T Comment Status D
(bucket1)
DTE XS symbol error counter registers needs update with 800G references and expanded to 32 lanes
SuggestedRemedy
Bring in and update 45.2.5.19 and 45.2.5.20 adding references to 172.3.4 and adding 16 more counters
Proposed Response Response Status W
PROPOSED ACCEPT.
IEEE P802.3df D1.0  1st Task Force review comments

Cl  169  SC 169.3.2  P 133  L 45  # 58
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D

800GAUI-n is not listed in the list of acronyms for Figure 169-3

SuggestedRemedy
Add 800GAUI-n to list of acronyms in Figure 169-3

Proposed Response  Response Status  W

Cl  171  SC 171.4  P 151  L 38  # 59
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D

There is no am_lock variable in Clause 172

SuggestedRemedy
Change am_lock to amps_lock in Table 171-3 and 171-5

Proposed Response  Response Status  W

Cl  172  SC 172.2.4.4  P 164  L 49  # 60
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D

Missing the relationship of the flow 0 257-bit block to the AM group

SuggestedRemedy
add "following the alignment marker group" before "in flow 0"

Proposed Response  Response Status  W

Cl  172  SC 172.3.1  P 172  L 35  # 61
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D

The variable name is amps_lock not am_lock

SuggestedRemedy
Change am_lock to amps_lock in Table 172-4

Proposed Response  Response Status  W

Cl  45  SC 45.2.3.26a  P 44  L 24  # 62
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D

Clause 172 (and 119) use a variable named amps_lock[x] for lane alignment lock status.
Which was the name used in Cl91 and 161 for the FEC sublayers.

SuggestedRemedy
Bring in 45.2.3.25.* and 45.2.3.26.*

For indexes 16 to 32 change the "(see 82.2.19.2.2)" to be "(see 82.2.19.2.2) or
amps_lock[16] (see 172.2.6.2.2)"

For indexes 0 to 15 and change the "(see 82.2.19.2.2)" to be "(see 82.2.19.2.2) or
amps_lock[16] (see 119.2.6.2.2 and 172.2.6.2.2)"

Proposed Response  Response Status  W

Cl  172  SC 172.3.5  P 173  L 32  # 63
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D

The CW counter is a RS-FEC sublayer counter in MDIO space, not a PCS counter.

SuggestedRemedy
Copy of the definition of 45.2.1.120a (802.3ck) into a set of PCS registers (45.2.3.###) and
replace the Clause 161 references with 172.

Replace the text in 172.2.3.5 with the same text from 161.6.21 updating the MDIO register
references to point to the newly created MDIO registers.

Update Table 172-4 to point to the newly created MDIO registers.

Proposed Response  Response Status  W

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn
SORT ORDER: Comment ID
The FEC_codeword_error_bin_i is a RS-FEC sublayer set of counters in MDIO space, not PCS counters.

**Suggested Remedy**

Copy of the definition of 45.2.1.131a (802.3ck) into a set of PCS registers (45.2.3.###) and replace the Clause 161 references with 172.

Replace the text in 172.2.3.6 with the same text from 161.6.17 updating the MDIO register references to point to the newly created MDIO registers.

Update Table 172-4 to point to the newly created MDIO registers.

**Proposed Response**

ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.

Resolve along with comment #189.

---

Various clause 45 registers need to some Clause 172 references added.

**Suggested Remedy**

A reference to Clause 172 needs to be added to 45.2.3.49

A reference to 172.2.5.3 needs to be added to:

- 45.2.3.60.1
- 45.2.3.60.2
- 45.2.4.61.1
- 45.2.3.61.6
- 45.2.3.64
- 45.2.3.65
- 45.2.3.66
- 45.2.4.21.1
- 45.2.4.21.2
- 45.2.4.22.2
- 45.2.4.22.3
- 45.2.4.22.4
- 45.2.4.22.5
- 45.2.4.25
- 45.2.4.26
- 45.2.4.27
- 45.2.5.21.1
- 45.2.5.21.2
- 45.2.5.22.2
- 45.2.5.22.3
- 45.2.5.22.4
- 45.2.5.22.5
- 45.2.5.25
- 45.2.5.26
- 45.2.5.27

A reference to 172.2.6.2.2 needs to be added to:

- 45.2.3.61.1
- 45.2.3.61.2
- 45.2.3.61.3
- 45.2.3.61.5
- 45.2.4.22.1
- 45.2.5.22.1

A reference to 172.3.2 needs to be added to 45.2.3.62, 45.2.4.23 and 45.2.5.23

A reference to 172.3.3 needs to be added to 45.2.3.63, 45.2.4.24 and 45.2.5.24
A reference to 172.3.4 needs to be added to 45.2.3.58

**Proposed Response**

PROPOSED ACCEPT.

---

**Comment Status:** D

**Response Status:** W

**Comment ID:** 66

**Slavick, Jeff**

**Broadcom**

**Comment Type:** T

**Comment Status:** D

**Comment:** PHY XS AM lock registers need to be updated with 800G references and expanded to 32 AM lanes

**Suggested Remedy:**

Update (see 119.2.6.2.2) to (see 119.2.6.2.2 and 172.2.6.2.2) in 45.2.4.15.* and 45.2.4.16.* Add the extra 16 lanes of amps_lock as well as was done for the PCS registers.

**Proposed Response**

PROPOSED ACCEPT.

---

**Comment Status:** D

**Response Status:** W

**Comment ID:** 67

**Slavick, Jeff**

**Broadcom**

**Comment Type:** T

**Comment Status:** D

**Comment:** PHY XS lane mapping registers need to update with 800G references and expanded to 32 lanes

**Suggested Remedy:**

Bring in and update 45.2.4.17 and 45.2.4.18 adding references to Clause 171 and adding 16 more registers

**Proposed Response**

PROPOSED ACCEPT.

---

**Comment Status:** D

**Response Status:** W

**Comment ID:** 68

**Slavick, Jeff**

**Broadcom**

**Comment Type:** T

**Comment Status:** D

**Comment:** PHY XS symbol error counter registers needs update with 800G references and expanded to 32 lanes

**Suggested Remedy:**

Bring in and update 45.2.4.19 and 45.2.4.20 adding references to 172.3.4 and adding 16 more counters

**Proposed Response**

PROPOSED ACCEPT.
The paragraph provides mapping of registers 1.1320-1.1323 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

**Suggested Remedy**

change:

"Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323."

to:

"Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, lane 3 maps to register 1.1323, lane 4 maps to register 1.1324, lane 5 maps to register 1.1325, lane 6 maps to register 1.1326, and lane 7 maps to register 1.1327."

**Proposed Response**

**Response Status** W

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #73.

The paragraph provides mapping of registers 1.1420-1.1423 to lanes [0:3] but not the additional lanes of [4:7] used for eight-lane interface types.

**Suggested Remedy**

change:

"Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423."

to:

"Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, lane 3 maps to register 1.1423, lane 4 maps to register 1.1424, lane 5 maps to register 1.1425, lane 6 maps to register 1.1426, and lane 7 maps to register 1.1427."

**Proposed Response**

**Response Status** W

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #73.

Table footnote are numbered automatically in FrameMaker and cannot be struck out. Change the editorial instruction from

"Change Table 162–5, Table 162–6, and Table 162–7 as follows:"

to

"Change Table 162–5, Table 162–6, and Table 162–7, including footnotes, as follows:"

**Proposed Response**

**Response Status** W

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #74.
IEEE P802.3df D1.0  1st Task Force review comments

### Proposed Response # 76

**Cl 162 SC 162.13 P 97 L 21 # 76**

Lusted, Kent  
Intel Corporation

**Comment Type** TR  **Comment Status** D (bucket1)

Row entry for PMA800 has incorrect status value of "CR4:M". It should be "CR8:M"

**Suggested Remedy**

Change to "CR8:M"

**Proposed Response**  
PROPOSED ACCEPT.

### Proposed Response # 77

**Cl 162 SC 162.13 P 96 L 4 # 77**

Lusted, Kent  
Intel Corporation

**Comment Type** TR  **Comment Status** D (bucket1)

In P802.3ck, Clause 162.13 is the environmental specifications and Clause 162.14 is the PICS. The 162.13 sub clause is missing from the draft and creates an issue where the PICs became sub clause 162.13.

**Suggested Remedy**

Fix editing instruction on p96, line 1 to reference the heading of 162.14

Correct the sub clause number for the PICS to 162.14 in the title and the sub clauses.

Update all editing instructions as required.

Implement with editorial license

**Proposed Response**  
PROPOSED ACCEPT IN PRINCIPLE.

### Proposed Response # 78

**Cl 163 SC 163.3 P 100 L 27 # 78**

Lusted, Kent  
Intel Corporation

**Comment Type** TR  **Comment Status** D (bucket1)

Text references "CR" PMD types in the PMD service interfaces for Clause 163, which is for backplanes.

**Suggested Remedy**

Change "100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4" to "100GBASE-KR1, 200GBASE-KR2, and 400GBASE-KR4"

**Proposed Response**  
PROPOSED ACCEPT IN PRINCIP.

The text states that the KR* service interfaces are identical to those of CR*. The addition of "KR8" was erroneous.

Resolve using the response to comment #22.

### Proposed Response # 79

**Cl 162 SC 162.13 P 105 L 4 # 79**

Lusted, Kent  
Intel Corporation

**Comment Type** TR  **Comment Status** D (bucket1)

In P802.3ck, Clause 162.13 is the environmental specifications and Clause 162.14 is the PICS. The 162.13 sub clause is missing from the draft and creates an issue where the PICs became sub clause 162.13.

**Suggested Remedy**

Fix editing instruction on p105, line 1 to reference the heading of 163.14

Correct the sub clause number for the PICS to 163.14 in the title and the sub clauses.

Update all editing instructions as required.

Implement with editorial license

**Proposed Response**  
PROPOSED REJECT.

This comment was WITHDRAWN by the commenter.

### Proposed Response # 80

**Cl 169 SC 169.5 P 136 L 10 # 80**

Lusted, Kent  
Intel Corporation

**Comment Type** ER  **Comment Status** D (bucket1)

Figure 169-4 variable "q" should be italics like 'n' and 'p'. Both in middle and bottom of figure

**Suggested Remedy**

consider changing 'q' to italics types

**Proposed Response**  
PROPOSED ACCEPT IN PRINCIPLE.

Change font to italic for variable q.

Implement with editorial license.
IEEE P802.3df D1.0 1st Task Force review comments

**Comment ID**

# 81

**Comment Type:** T  **Comment Status:** D  **(bucket1)**

**Comment Text:**

Paragraph omits the eight-lane 800GAUI-8.

**Response:**

Proposed Response

PROPOSED ACCEPT.

**Comment ID**

# 82

**Comment Type:** TR  **Comment Status:** D  **(bucket1)**

**Comment Text:**

The mapping of the differential voltage level to the PAM4 symbol is missing in Annex 120F. It is also not present in Annex 120F in IEEE Std. 802.3ck-202x. The mapping of the differential voltage level to the PAM4 symbol level is important for interoperability.

**Response:**

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

In the sixth paragraph, change "The C2C transmitter and the receiver use PAM4 signaling" to: "The C2C transmitter and receiver use PAM4 signaling. The highest differential level corresponds to the tx_symbol or rx_symbol value three, and the lowest differential level corresponds to the tx_symbol or rx_symbol value zero."

**Comment ID**

# 83

**Comment Type:** ER  **Comment Status:** D  **(bucket1)**

**Comment Text:**

At end of first line of paragraph, 800GBASE-KR4 (wraps to line 28), "-KR4" should probably be "-KR8".

**Response:**

Proposed Response

PROPOSED ACCEPT.

**Comment ID**

# 84

**Comment Type:** ER  **Comment Status:** D  **(bucket1)**

**Comment Text:**

"State diagrams are identical to those specified in 119.2.6.3 ... ." State diagrams in Figure 119-14 "Transmit state diagam" and Figure 119-15 "Receive state diagram" can cause logic implementation issues at high rate port speeds (i.e. 800GbE) as shown in opsasnick_3df_01a_221005.pdf. A "stateless" encode/decode option to these state diagrams could be allowed since the state diagrams were originally designed for non-FEC interfaces. Interfaces with required FEC should have sufficient protection to allow for the stateless coding. An updated presentation showing the error analysis will be forthcoming.

**Response:**

Proposed Response

PROPOSED REJECT.

Pending Task Force review of supporting presentation.
IEEE P802.3df D1.0 1st Task Force review comments

Proposed Response

# 87
Cl 120G SC 120G.3.2.1 P 209 L 21 # 87
Opsasinck, Eugene Broadcom

Comment Type ER Comment Status D (bucket1)
In Table 120G-4, four instances of "800GAUI-4" in last two rows of the table should likely be "800GAUI-8"

Suggested Remedy
Replace "800GAUI-4" with "800GAUI-8"

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Change 800GAUI-4 to 800GAUI-8 in the bottom two rows of the table (4 instances).

# 88
Cl 124 SC 124.8.5a P 76 L 15 # 88
Opsasinck, Eugene Broadcom

Comment Type ER Comment Status D (bucket1)
In second line of paragraph, "800GBASE-DR4" should probably be "...-DR8". Same text appears on line 25 in 124.8.5b, and on page 77, line 29, section 124.8.9.2.

Suggested Remedy
Replace "800GBASE-DR4" with "800GBASE-DR8".

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #13.

# 89
Cl 124 SC 124.3.1 P 63 L 13 # 89
He, Xiang Huawei

Comment Type ER Comment Status D (bucket1)
Looks like a typo. "16834 bit times" should be "16384 bit times"

Suggested Remedy
Change 16834 to 16384.

Proposed Response Response Status W
PROPOSED ACCEPT.

Rechtman, Zvi Nvidia

Comment Type T Comment Status D AM sync
Figure 172–2—Functional block diagram
The block diagram includes two flows for TX and Rx.
Both TX flows are supposed to insert the alignment markers in sync with each other. This does not appear explicitly in the diagram.

Suggested Remedy
Possible improvement #1:
Add arrow with the word synchronization between the "Alignment insertion" blocks.
Possible improvement #2:
Add a footnote that the two "Alignment insertion" should operate in synchronized manner.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
The insertion location of the AM pattern in both flows must be done at the same point in the 66-bit block stream prior to the block distribution.
The intent of the third bullet in the exception list in 172.2.4.4 is to enforce the synchronization of the AM insertion between the two flows, without defining a specific implementation.
There will be an editorial presentation proposing an update to the text used in the third bullet in the exception list in 172.2.4.4 to make the intent clearer.

Rechtman, Zvi Nvidia

Comment Type T Comment Status D AM sync
"The first 66-bit block of the 257-bit transcoded block .. from the 64B/66B encoder."
This sentence implicitly means that the alignment insertion process of the two flows should be synchronized.
To avoid mistakes, it would be preferable to explicitly state that the two alignment insertion are synchronized.

Suggested Remedy
Add the following sentence before "The first 66-bit... " sentence:
"The marker insertion functions of the two flows must insert their markers at the exact same time (block unit), i.e. in a synchronized manner"

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #90.

Comment ID 91 Page 19 of 45
TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn SORT ORDER: Comment ID
2022-11-28 1:47:12 PM
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<td></td>
<td></td>
<td>ER</td>
<td>D</td>
<td>Change &quot;400GBASE-R&quot; to &quot;800GBASE-R&quot;</td>
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<td></td>
<td>PROPOSED ACCEPT.</td>
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<td>30</td>
<td>30.5.1.1.2</td>
<td>ER</td>
<td>D</td>
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<td>D</td>
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<td>W</td>
<td></td>
<td>PROPOSED ACCEPT.</td>
</tr>
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<td>124</td>
<td>124.11.3.1.1</td>
<td>ER</td>
<td>D</td>
<td>The positions of &quot;Rx&quot; in figure 124-6 is inconsistent with the text at line 27, which is depicted as the right-most four positions.</td>
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<td>The space after &quot;these&quot; should be underlined.</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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<td>124.2</td>
<td>ER</td>
<td>D</td>
<td>The space after &quot;these&quot; should be underlined.</td>
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<td>ER</td>
<td>D</td>
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</tr>
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<td>W</td>
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<td>Change the title of Figure 124-2 from &quot;Block diagram for 400GBASE-DR4 transmit/receive paths&quot; to &quot;Block diagram for 400GBASE-DR4 or 400GBASE-DR4-2 transmit/receive paths&quot;</td>
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<td>Comment ID</td>
<td>P</td>
<td>L</td>
<td>SuggestedRemedy</td>
<td>Proposed Response</td>
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<td>98</td>
<td>P65</td>
<td>49</td>
<td>Missing comma after &quot;400GBASE-DR4-2&quot;</td>
<td>PROPOSED ACCEPT.</td>
<td>(W)</td>
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<td>P68</td>
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<td>(W)</td>
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<td>(W)</td>
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<td>P71</td>
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<td>PROPOSED ACCEPT.</td>
<td>(W)</td>
</tr>
</tbody>
</table>
Comment ID: 104

Proposed Response

The comma after "400GBASE-DR4" should be underlined.

Suggested Remedy

Underline the comma after "400GBASE-DR4".

Comment ID: 105

Proposed Response

Table 124.11. Why would the optical return loss be any different between DR4/DR8 and DR4-2/DR8-2? Don’t they both use the same MPO connector. The value of 25dB for DR4-2/DR8-2 appears to have been copied over from 100GBASE-FR1 in 802.3cu, but isn’t FR1 using a different optical connector (LC versus MPO).

Suggested Remedy

This is more of a question for clarification.

Comment ID: 106

Proposed Response

Figure 124-6 indicates a different lane assignment for 400GBASE-DR4 than is in Clause 124 of the published version of the 802.3 standard. This would appear to make 400GBASE-DR4 incompatible with the current published standard.

Suggested Remedy

Change the lane assignment in Figure 124-6 in 802.3df D1.0 to match the lane assignment in Figure 124-6 of "P802.3_D3p2".

Comment ID: 107

Proposed Response

The NOTE says "The stream of 66-bit blocks generated by this process". However, there are two streams generated in the above process. It would be clearer if the end of the subclause represented the end of the process and aligned with the OTN reference point in the note.

Also, it would be clearer for the text related to tx_coded<65:0> to coincide with the end of the sub-clause (i.e. for that text to follow any discussion related to rate compensation).

Also, where possible it is helpful to re-use text from 802.3-2022 Clause 119.2.4.1 as it enhances readability (i.e. simplifies compare/contrast between Clause 119 and Clause 172).

Suggested Remedy

Propose the following text:

172.2.4.1 Encode and rate matching

The transmit PCS generates 66-bit blocks based upon the TXD<63:0> and TXC<7:0> signals received from the 800GMII. One 800GMII data transfer is encoded into one 66-bit block. If the transmit PCS spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle control characters.

Idle control characters or sequence ordered sets are removed, if necessary, to accommodate the insertion of the alignment markers. See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules, and 172.2.4.5 for more details on alignment markers.

The transmit PCS generates blocks as specified in the transmit state diagram as shown in Figure 119-14. The contents of each 66-bit block are contained in a vector tx_coded<65:0>. tx_coded<1:0> contains the sync header and the remainder of the bits contain the payload.

NOTE: The stream of tx_coded<65:0> 66-bit blocks generated by this process, together with the FEC_degraded_SER and rx_local_degraded bits should be used as the reference signal for mapping to OTN.

172.2.4.1 66B/66B block distribution

The stream of tx_coded<65:0> 66-bit blocks are distributed to the two flows in a round robin fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue in a round robin distribution procedure across the two flows. This forms two streams, tx_coded_flow0<65:0> and tx_coded_flow1<65:0>.

172.2.4.3 64B/66B to 256B/257B transcoder
The 64B/66B to 256B/257B transcoder in each flow is identical to that specified in 119.2.4.2. The transcoder for flow 0 uses the stream of tx_coded_flow0<65:0> 66-bit blocks. The transcoder for flow 1 uses the stream of tx_coded_flow1<65:0> 66-bit blocks.

172.2.4.4 Scrambler

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.
The suggested remedy inserts a subclause for the 66-bit block distribution into 172.2.4 resulting in subclause numbering within 172.2.4 that does not align with the subclause numbers in CL119. This impacts the readability when comparing/constrasting CL172 with CL119. Hence, the 66-bit block distribution was incorporated into 172.2.4.1 keeping the rest of the subclause numbering the same as in CL119. The functions defined by subclauses 172.2.4.2 are identical to those performed by each flow in 800GbE PCS, and hence 172.2.4.1 was intentionally kept unchanged and references back to 119.2.4.2.

The first sentence of the comment points out a potential source of confusion regarding the 66-bit stream that is used for mapping to OTN and the proposed response below address that concern.

Change NOTE from
"NOTE—The stream of 66-bit blocks generated by this process, together with the FEC_degraded_SER and rx_local_degraded bits should be used as the reference signal for mapping to OTN."

to

"NOTE—The stream of 66-bit blocks generated by the encode and rate matching process (see Figure 172-2) prior to 66-bit block distribution, together with the FEC_degraded_SER and rx_local_degraded bits should be used as the reference signal for mapping to OTN."

172.2.4.5 Alignment marker mapping and insertion

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Let tx_coded_j<65:0> and tx_coded_k<65:0> represent two consecutive blocks in the tx_coded<65:0> stream. Notably, tx_coded_j<65:0> belongs to tx_coded_flow0<65:0> stream. And, tx_coded_k<65:0> belongs to tx_coded_flow1<65:0> stream.

Let tx_coded_j<65:0> represent the first 66-bit block of the 257-bit transcoded block following the alignment marker group in flow 0. It is required that tx_coded_k<65:0> shall be the first 66-bit block of the 257-bit transcoded block following the alignment marker group in flow 1.

172.2.6.2.2 AML sync

Proposed Response Response Status W

PROPOSED REJECT.
The proposed change is not necessary since Clause 172 is only for 800GBASE-R. CL119 specified 200GBASE-R or 400GBASE-R because the same clause includes the PCS for both 200GE and 400GE.
The superscript 3 should follow IEEE Xplore, not "contact IEEE."

Get the template at https://standards.ieee.org/develop/drafting-standard/resources/ fixed and implement the change.

PROPOSED ACCEPT IN PRINCIPLE.

The group of text starting with "When the IEEE-SA Standards Board:“ is repeated twice. Remove one instance.

Implement with editorial license.
Comment Type: E  Comment Status: D  (bucket1)
3bj and 3bk!! They were approved in 2013 and 2014. 3cy uses 3cx and 3cz as its examples, 3cz uses 3dd, 3cs, 3db, 3ck, 3de and 3cx

Suggested Remedy
Instead of or as well as this bad example, list all the exact amendments and drafts that this draft is built against, as P802.3cz does. Also, say which drafts affect this draft and which are believed not to, preferably clause by clause. The editors must have and agree this information; no reason not to share it with the volunteers who do the review work, and the staff editors.

PROPOSED ACCEPT IN PRINCIPLE.
The example projects listed are indeed obsolete. This example list from the FrameMaker template needs to be updated for each project and may again change as previous amendments are incorporate into a revision. The examples are not really required so these examples should be deleted here and in the template. Delete "(e.g., IEEE P802.3bj and IEEE P802.3bk)"

Comment ID 115
Page 25 of 45
2022-11-28  1:47:12 PM

Comment Type: E  Comment Status: D  (bucket1)
This project is adding another page of definitions to a very long section that lacks the usual level of subdivision (somewhere around one subclause per page would be normal)

Suggested Remedy
To mitigate the deterioration of document structure and usability, divide 1.4 Abbreviations into several subclauses

PROPOSED REJECT.
The comment is asking for broad changes to the base standard that are not related directly to the new content that is being added by this amendment. Such sweeping changes should be addressed using the Base Standard maintenance process.

Comment ID 118
Page 25 of 45
2022-11-28  1:47:12 PM
IEEE P802.3df D1.0 1st Task Force review comments

---

**Comment ID 119**

**Cl 45 SC 45.2.1.161 P 41 L 34 # [119]**

Dawe, Piers Nvidia

Comment Type E Comment Status D (bucket1)

Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.

Suggested Remedy

Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, and so on, up to lane 7 and register 1.1127.

Similarly in 45.2.1.163, 45.2.1.165, 45.2.1.167

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #45.

---

**Comment ID 120**

**Cl 45 SC 45.2.1.168 P 42 L 38 # [120]**

Dawe, Piers Nvidia

Comment Type E Comment Status D (bucket1)

"for PMD lane 1; etc.: a bit terse and informal

Suggested Remedy

Suggested rewording: Register 1.1450 controls the PMD training pattern for PMD lane 0, register 1.1451 controls the PMD training pattern for PMD lane 1, and so on, up to register 1.1457 and PMD lane 7.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #32.

---

**Comment ID 121**

**Cl 45 SC 45.2.1.168 P 42 L 41 # [121]**

Dawe, Piers Nvidia

Comment Type E Comment Status D (bucket1)

92.7.12 and 136.8.11.1.3

Suggested Remedy

92.7.12, 136.8.11.1.3, or 162.8.11.1 as appropriate

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change the first sentence of the second paragraph of 45.2.1.168 so it reads as "Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training a particular PMD lane as described in 92.7.12, 136.8.11.1.3, or 162.8.11.1."

---

**Comment ID 122**

**Cl 45 SC 45.2.1.168 P 42 L 24 # [122]**

Dawe, Piers Nvidia

Comment Type TR Comment Status D PRBS seed (bucket1)

This says "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function."

This is in a section defining the meanings of bits in a memory map. The memory map serves the sublayer, not the other way round. Advice about signal integrity should be in the clause concerned.

With only four polynomials and eight lanes, the polynomials themselves can't all be different, but that's OK. Impairment is very unlikely unless adjacent lanes use the same polynomial AND the PRBS13Qs in the training pattern are aligned in time with each other.

We have written generations of PMD and AUI clauses that use the same pattern on multiple lanes, but they should be skewed, e.g. 120G.3.2.2: "For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated." The training frame is 98.3% PRBS13Q. In principle, one could incur the risk warned against with a lane carrying "identifier_i = 0 and an adjacent lane carrying "identifier_i = 4, with an unlucky timing offset between lanes. As "The PMD shall implement one instance of the PMD control function described in 136.8.11 for each lane", the state machine for each lane can be started and restarted asynchronously to adjacent lanes, so starting the training pattern with a different seed won't solve the issue. The text "For 8-lane use cases different initial seeds should be used where the same polynomial is being reused" recommends a course of action that, on investigation, doesn't address the issue. We should tell the reader what to avoid, not how to avoid it.

Also, the ETC spec has already covered this ground. It uses the same four polynomials and seeds, twice over. No implementation can follow the ETC spec AND this draft (because the default seeds differ) but there is no benefit in the difference.

Suggested Remedy

1. Put signal integrity recommendations in the spec, not in the register definitions for a memory map!
2. Change "The polynomial identifier for each lane should be unique; two physically adjacent lanes having the same identifier could impair operation of the PMD control function" to "The polynomial identifier for adjacent lanes should be unique to avoid a risk of impairment of the PMD control function".
3. Change "For 8-lane use cases different initial seeds should be used where the same polynomial is being reused." to "For 8-lane use cases, see 162.8.11.1."
4. Make the default seeds in Table 162-10a the same as in the ETC spec (seeds 4 to 7 are the same as seeds 0 to 3).
5. ETC say "it is recommended to ensure that physically adjacent lanes do not use the same polynomial". Recommend this.
6. Also, suggest that when there are more lanes than polynomials to use, significant correlation between any lanes can be avoided by a combination of seed and timing offset. Leave it to the implementer to choose how to do this.
PROPOSED ACCEPT IN PRINCIPLE.

The polynomial identifier for adjacent lanes should be unique to avoid a risk of impairment of the PMD control function. If the same polynomial identifier is used for multiple lanes, different initial seeds should be used for each of those lanes. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11. Therefore it is not appropriate to change Table 162-10a.

See also the response to comment #139.

**Comment ID**

124

**Page 27 of 45**

2022-11-28  1:47:12 PM
The unlikely case of defective transition density is far more significant than the very modest difference between 2-way and 4-way RS-FEC interleaving. If we are going to break precedent and abandon unrestricted bit-multiplexing, transition density is the first thing to get right, always. With 100G AUI lanes, the Tx silicon can ensure the problem doesn't happen, and we are not mandating 50G/lane AUIs for 800G. We have had some years after this problem was discovered before 800G designs, so it should not be happening now. Let's say so.

SuggestedRemedy
Change "See NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate." to "For 400GBASE-DR4 and 400GBASE-DR4-2, see NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate. For 800GBASE-DR8 and 800GBASE-DR8-2, see 173.4.2."

Similarly in 124.7.2.
In 173.4.2, say that unlike in 120, it is the transmit side PCS and PMA's responsibility to avoid the defective transition density, and give some recommendations.

See other comments.

Proposed Response
Response Status W
PROPOSED REJECT.
Resolve using the response to comment #167.

SuggestedRemedy
As elsewhere: change "See NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate."

This says "The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel that meets the requirements for 100GBASE-FR1 in 140.7.5.2" but these PMDs have an optical return loss tolerance of 21.4 while 100GBASE-FR1 uses an optical return loss of 17.1 dB. The cable plant is different (array connectors are angled).

SuggestedRemedy
Change
The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel that meets the requirements for 100GBASE-FR1 in 140.7.5.2.

to
The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel with dispersion and insertion loss as for 100GBASE-FR1 in 140.7.5.2, and optical return loss at the maximum for optical return loss tolerance in Table 124-6.

Proposed Response
Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.
These fiber optic cabling characteristics for 400GBASE-DR4-2 and 800GBASE-DR8-2 are not in the baseline, but are the same as for 100GBASE-FR1. The optical return loss should not follow FR1, as the optical return loss tolerance is significantly different and the table of discrete reflectances is different.

**Suggested Remedy**

Adjust the optical return loss as necessary to be consistent with the adopted optical return loss tolerance and table of discrete reflectances.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #132.

---

Part of the baselines is missing. Both baselines have a table of discrete reflectances above 55 dB.

**Suggested Remedy**

Add this (these) as a new column(s) in Table 124-9.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

A presentation will be provided for task force discussion.

---

It seems odd that the table of discrete reflectances above 55 dB for 800GBASE-DR8 in the baseline is not the same as the existing table for 400GBASE-DR4, but it is the same as 400GBASE-DR4-2 and 800GBASE-DR8-2.

**Suggested Remedy**

Reconcile the tables for 400GBASE-DR4 and 800GBASE-DR8.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #132.

---

This says to use a single-row 16-fiber interface. But this is not in welch_3df_01a_220222, and 8 x100G SMF modules already exist with 2 x 12-way angled connectors.

**Suggested Remedy**

Change to 2 x 12-way angled connectors.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Members of the task force have indicated that only 16-fiber connectors are being used and the connectors are angled. The editor's note states that this addition connection information was added by the editorial team for completeness. In 124.11.3.3 replace the second paragraph with:

"The MDI adapter or receptacle shall meet the dimensional specifications for interface 7-4-7: MPO adaptor interface – Opposed keyway configuration or interface 7-4-9: MPO active device receptacle, angled interface for 16 fibers, as defined in IEC 61754-7-4. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-4-1: MPO female plug, down-angled interface for 16 fibers. The MPO-16 female plug connector and MDI are structurally similar to those depicted in Figure 124–7, but with an angled end facet, 16 fibers, an offset keyway, and different pin diameters and locations." Implement with editorial license.
IEEE P802.3df D1.0 1st Task Force review comments

Comment ID 136
124 SC 124.11.3.1.2 P 80 L 50
Dawe, Piers Nvidia

Comment Type E  Comment Status D fiber connector (CC)
"The transmit optical lanes occupy the leftmost eight positions. The receive optical lanes occupy the rightmost eight positions": as there are only 12 positions, "most" is not really applicable.

Suggested Remedy
Change to "The transmit optical lanes occupy the eight positions on the left. The receive optical lanes occupy the eight positions on the right.

PROPOSED REJECT.
The proposed changes do not improve the accuracy or clarity of the draft. There are 16 positions.

Comment ID 137
162 SC 162.8.11.1 P 92 L 8
Dawe, Piers Nvidia

Comment Type T  Comment Status D PRBS seed
the state of the PRBS generator shall be set to a value in the variable - eh? If the variable is a 13-bit seed, it contains 0s and 1s.

Suggested Remedy
Rewrite for clarity

PROPOSED REJECT.
The text referred to by the comment is based on existing text in clause 136: "At the start of the training pattern, the state of the PRBS generator shall be set to the value seed_i." This text provides sufficient information for correct implementation the PMD control function. The suggested remedy does not provide sufficient detail to implement.

Comment ID 138
162 SC 162.8.11.1 P 92 L 9
Dawe, Piers Nvidia

Comment Type T  Comment Status D PRBS seed
The variable seed_i is not defined. 136.8.11.1.3 says "The default value of seed_i shall be the value given in Table 136-8 for p = I," but neither p nor Table 136-8 apply here. Maybe they should?

Suggested Remedy
If the seed bits in Table 162-10a are the defaults for seed_i, say so.

PROPOSED ACCEPT IN PRINCIPLE.
In the third paragraph of 162.8.11.1, change "the default seed for each lane" to "the default value of seed_i for each lane i". In Table 162-10a, change the heading of the fourth column from "Default seed bits" to "Default seed_i".
IEEE P802.3df D1.0  1st Task Force review comments

### Comment 139

**Comment Type:** TR  
**Comment Status:** D  
**Dawe, Piers**  
**Nvidia**

**Comment ID:** 139

**Rate Range:** PRBS seed

Default seeds 4 to 7 are different to seeds 0 to 3, contrary to the ETC 800G spec. No implementation can follow the ETC spec AND this draft (because the default seeds differ) but there is no benefit in the difference.

We have written generations of PMD and AUI clauses that use the same pattern on multiple lanes, but they should be skewed, e.g. 120G.3.2.2: “For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated.” The training frame is 98.3% PRBS13Q. In principle, one could incur the risk warned against with a lane carrying “identifier_i” = 0 and an adjacent lane carrying “identifier_i” = 4, with an unlucky timing offset between lanes. As “The PMD shall implement one instance of the PMD control function described in 136.8.11 for each lane”, the state machine for each lane can be started and restarted asynchronous to adjacent lanes, so starting the training pattern with a different seed won’t solve the issue.

**Suggested Remedy**

1. Make the default seeds in Table 162-10a the same as in the ETC spec (seeds 4 to 7 are the same as seeds 0 to 3).
2. ETC say “it is recommended to ensure that physically adjacent lanes do not use the same polynomial”. Recommend this.
3. Also, point out that significant correlation between any lanes can be avoided by a combination of seed and timing offset. Leave it to the implementer to choose how to do this.

**Proposed Response**

PROPOSED REJECT.

Aligning an IEEE standard with a previously published document may be preferable where possible, but it is not always done.

The default seed values were explicitly set by the adopted baseline proposal https://www.ieee802.org/3/df/public/22_09/lusted_3df_01a_2209.pdf, which included a detailed description, and was approved by unanimous consent.

The seed values are not normative, and using non-default values is permitted, so there is no compliance concern.

The content of item 2 and 4 of the suggested remedy is covered by text in 45.2.1.168 ("should" is a recommendation).

Resolve with #122.

### Comment 140

**Comment Type:** E  
**Comment Status:** D  
**Rate Range:** PRBS seed

“For an 800GBASE-CR8 PMD or for a 100GBASE-CR1, 200GBASE-CR2, or 400GBASE-CR4 PMD in the same package as the PCS sublayer": it’s very easy to misunderstand this.

**Suggested Remedy**

At least put a comma after “CR8 PMD”. Also in 163.9.2.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

The text intentionally distinguishes between 800GAIU-8, for which the range is always +/- 50 PPM, and the other interfaces, for which it is conditional.

Therefore the suggested remedy would not be correct. However, the text can be clarified.

In Table 162-11 change the first sentence in footnote a to the following:

“For 100GBASE-CR1, 200GBASE-CR2, or 400GBASE-CR4 PMD with a PMA in the same package as the PCS sublayer or for any 800GBASE-CR8 PMD.”

In Table 163-5 change the first sentence in footnote a to the following:

“For 100GBASE-KR1, 200GBASE-KR2, or 400GBASE-KR4 PMD with a PMA in the same package as the PCS sublayer or for any 800GBASE-KR8 PMD.”

Resolve with comment #50.

### Comment 141

**Comment Type:** E  
**Comment Status:** D  
**Dawe, Piers**  
**Nvidia**

**Comment ID:** 141

**Rate Range:** (bucket1)

This text is an informative NOTE in the standard in force, as below. While I can see the reason to make it normative for the transmitter, for the receiver this information about transmmitter behaviour is explanation, not something the receiver does.

**Suggested Remedy**

Change it from a normative table footnote to an informative table note. Similarly for 163.9.3.

**Proposed Response**

PROPOSED ACCEPT.
Strange to talk about 800G before 100G and 200G: not the usual order (slow MAC to fast MAC).

SuggestedRemedy

The block diagrams for 100GBASE-VR1 and 100GBASE-SR1 are equivalent to Figure 167-2, but for one lane per direction. The block diagrams for 200GBASE-VR2 and 200GBASE-SR2 are equivalent to Figure 167-2, but for two lanes per direction. The block diagrams for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for eight lanes per direction.

PROPOSED ACCEPT IN PRINCIPLE.

Change editing instruction to “Replace the first paragraph in 167.5.1 with the following:”

The block diagrams for 100GBASE-VR1 and 100GBASE-SR1, for 200GBASE-VR2 and 200GBASE-SR2, and for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167-2, but for one, two and eight lanes per direction respectively.

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.
Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Members of the task force have indicated that both 16 and 24 fiber connectors are being used and the 16 fiber connectors are angled and the 24 fiber connectors are flat. The editor's note states that this addition connection information was added by the editorial team for completeness.

Replace the existing text in 167.10.3.4 with

"The MDI shall optically mate with the compatible plug on the optical fiber cabling. 600GBASE-VR8 and 800GBASE-SR8 have two optical lanes assignment options (see 167.10.3.1a)."

For option A, the MDI adapter or receptacle shall meet the dimensional specifications for interface 7-2-3: MPO active device receptacle, angled interface for 16 fibers, as defined in IEC 61754-7-2.

Replace the existing text in 167.10.3.4 with

"The MDI active device receptacle, angled interface for 16 fibers, as defined in IEC 61754-7-2, is required to meet the dimensional specifications for IEC 63267-1. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-2-1: MPO female plug connector, down-angled interface for 2 to 24 fibers, as defined in IEC 61754-7-1."

IEC 63267-1 with performance grade 1m specification is expected to be available in 2023.

Proposed Response

PROPOSED REJECT.

The description provided in Clause 116 was overly verbose with repeated details that are listed in the reference PMA clause. The PMA description in Clause 169 provides the general function of a PMA with similar detail provided in the other sublayer descriptions which reference the relevant PMA subclauses where the reader may find all of the details relevant to each PMA type.

Type: RE/presented

Comment Type: TR/technical required

Comment Status: D/dispatched

Response Status: W/written

Delete the existing text in 167.10.3.4 with

"The MDI shall optically mate with the compatible plug on the optical fiber cabling. 600GBASE-VR8 and 800GBASE-SR8 have two optical lanes assignment options (see 167.10.3.1a)."

For option A, the MDI adapter or receptacle shall meet the dimensional specifications for interface 7-2-3: MPO active device receptacle, angled interface for 16 fibers, as defined in IEC 61754-7-2.
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<td></td>
<td>Is a &quot;linked device&quot; defined or explained anywhere”? The definition and use of &quot;link&quot; is a delicate area.</td>
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<td><strong>SuggestedRemedy</strong></td>
<td>Delete &quot;linked&quot;. In the next line, change &quot;the link&quot; to &quot;a link&quot;.</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE. The language in this paragraph is consistent with similar subclause 80.2.6 (802.3-2022) and 116.2.5a (802.3ck-2022). However, the term &quot;linked device&quot; rather than just &quot;device&quot; does not seem to provide any useful information. However, the other device is the one on the same link as the local device so &quot;the link&quot; rather than &quot;a link&quot; is correct.</td>
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<td>Change &quot;linked device&quot; to &quot;link&quot;.</td>
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<td>In Figure 116-2, multiple lanes are shown explicitly: PMA:IS_UNITDATA_0.request PMA:IS_UNITDATA_1.request ... PMA:IS_UNITDATA_7.request</td>
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<td><strong>SuggestedRemedy</strong></td>
<td>As a compromise, follow e.g. Figure 120G-2; add the short diagonal lines &quot;n&quot; to show n lanes, not n requests on one lane with a constant ordering. Several figures, including Fig 172-2 where showing the numbers, 16 and 32, will be helpful.</td>
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<td>PROPOSED REJECT. A single line with an SI parameter with vector notation clearly conveys the fact that there are multiple lanes 0 to n-1. This approach is used to reduce the clutter compared to similar diagrams in Clause 116. This approach is used consistently in various figures in 802.3df. The proposed changes do not improve the accuracy or clarity of the draft.</td>
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<td>116.5 says &quot;Skew (or relative delay) can be introduced between lanes&quot;. This says &quot;Skew (or relative delay) can be introduced between PCS lanes&quot; which gives a false impression that PMA and PML lanes don't get skewed.</td>
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<td>PROPOSED REJECT. Skew is constrained for each sublayer to limit the net skew between PCS lanes so that the cumulative skew between PCS lanes does not exceed the ability of the specified PCS deskew function.</td>
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<td><strong>Comment Status</strong></td>
<td><strong>D</strong></td>
<td><strong>(bucket1)</strong></td>
</tr>
<tr>
<td></td>
<td>This has got so little to say it's a waste of a clause number. The 100/200/400/800GMII is like the MAC: almost identical apart from rates, timing and optional EEE.</td>
<td></td>
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<td></td>
<td><strong>SuggestedRemedy</strong></td>
<td>Merge 170 into 117 or better, merge 170 and 117 into 81.</td>
<td></td>
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<tr>
<td></td>
<td><strong>Proposed Response</strong></td>
<td><strong>Response Status</strong></td>
<td><strong>W</strong></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>PROPOSED REJECT. The comment does not provide sufficient justification to support the suggested remedy. The current structure of the draft is consistent with the approach taken by previous projects.</td>
<td></td>
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</tr>
</tbody>
</table>
IEEE P802.3df D1.0  1st Task Force review comments

Cl  171  SC  171.4  P  152  L  18  #  [153]
Dawe, Piers  Nvidia
Comment Type  E  Comment Status  D
activate_t
threshold  (bucket1)

SuggestedRemedy
Make these tables full width, make the right hand columns wider, also in Clause 172. It may be necessary to set break points in these long "words". In maintenance we might change to shorter names, e.g. FEC_degraded_SER_thresh_on

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Improve appearance of the variable names with editorial license.

CI  171  SC  171.4  P  153  L  11  #  [154]
Dawe, Piers  Nvidia
Comment Type  T  Comment Status  D

Under "MDIO status variable" there is an entry "Lane 0 to 31 aligned" but this isn't a variable that indicates if lanes 0 to 31 are aligned. Table 45-350 has "Name's Lane 0 aligned, Lane 1 aligned, and so on. Is there such a thing as an "MDIO variable" anyway? Clauses such as PCS have variables, MDIO has registers. The way of talking about such multiline things was solved long ago; e.g. "84.7.5 PMD lane-by-lane signal detect function"

SuggestedRemedy
Because a "variable" must be talking about one lane not the pair of registers recording 16 or 32 lanes, change "Lane 0 to 31 aligned" back to how it is in 117: "Lane x aligned" or "Lane i aligned" or better, "Lane aligned". "Lane-by-lane aligned" seems odd, but "DTE XS FEC symbol errors lane 0 to lane 31" below can be "DTE XS FEC symbol errors by lane" Similarly in several tables, also in other clauses such as 172, PCS.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Change "Lane 0 to 31 aligned" to "Lane aligned, lane 0 to 31"

Cl  172  SC  172.1.1  P  160  L  11  #  [155]
Dawe, Piers  Nvidia
Comment Type  T  Comment Status  D

The paragraph of introduction in 119.1.1 is missing: "Both 200GBASE-R and 400GBASE-R are based on a 64B/66B code. The 64B/66B code supports transmission of data and control characters. The 64B/66B code is then transcoded to 256B/257B encoding to reduce the overhead and make room for forward error correction (FEC). The 256B/257B encoded data is then FEC encoded before being transmitted. Data distribution is introduced to support multiple lanes in the Physical Layer. Part of the distribution includes the periodic insertion of an alignment marker, which allows the receive PCS to align data from multiple lanes."

SuggestedRemedy
At least refer to 172.1.3 as an introduction.

Proposed Response  Response Status  W
PROPOSED REJECT.
172.1.1 is the scope and the current text is a sufficient description of the scope of the clause. All of the information noted in the comment is provided in 172.1.3 and there is no need to duplicate it in the scope.

Cl  172  SC  172.1.5  P  162  L  12  #  [156]
Dawe, Piers  Nvidia
Comment Type  E  Comment Status  D

"66B Block distribution": bits not bytes, rogue capital, style

SuggestedRemedy
66-bit block distribution
also 66-bit block collection

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Replace 66B by 66-bit in Fig 172-2 in two places.
IEEE P802.3df D1.0 1st Task Force review comments

### Comment #158

**Comment Type:** Transcode

**Comment Status:** (bucket1)

**Suggested Remedy:**

- transcode - 4 times
- Also in this figure: Encode, Decode, Interleave, Lane

**Proposed Response:**

- **Response Status:** W
- **PROPOSED ACCEPT IN PRINCIPLE.
- Correct the capitalization with editorial license.**

**Comment Status:** D

**Response Status:** W

- **(bucket1) Dawe, Piers**
- **Nvidia**

**Proposed Response:**

- **Response Status:** W
- **PROPOSED ACCEPT IN PRINCIPLE.**
- Change from "169.3" to "169.3.1" **(bucket1)**

### Comment #160

**Comment Type:** E

**Suggested Remedy:**

- **defined in 169.3" but 173.2 says "defined in 169.3.1"**

**Proposed Response:**

- **Response Status:** W
- **PROPOSED ACCEPT IN PRINCIPLE.**
- Change from "169.3" to "169.3.1" **(bucket1)**

### Comment #163

**Comment Type:** E

**Suggested Remedy:**

- **Reconcile**

**Proposed Response:**

- **Response Status:** W
- **PROPOSED ACCEPT.**

**Comment Status:** D

**Response Status:** W

- **(bucket1) Dawe, Piers**
- **Nvidia**

**Proposed Response:**

- **Response Status:** W
- **PROPOSED ACCEPT IN PRINCIPLE.**
- Resolve using the response to comment #196. **(bucket1)**
IEEE P802.3df D1.0 1st Task Force review comments

Proposed Response
# 164
Cl 173 SC 173.4 P 180 L 10 # 164
Dawe, Piers Nvidia
Comment Type E Comment Status D
32.8 PMA Functional Block Diagram
SuggestedRemedy
32.8 PMA functional block diagram - 3 figures

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
In the titles for Figure 173-3, 173-4 and 173-5, change from:
"Functional Block Diagram"
to
"functional block diagram"

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
This additional constraint provides a very modest benefit that is judged not necessary in
400G Ethernet. However, the rare but much more harmful "clock content" (transition
density) issue that was discovered late in P802.3bs should now be outlawed. There are
many easy ways to do this.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Replace the text in 173.4.1 with the following splitting the text into two paragraphs:
"If the interface between the PMA client and the PMA is physically instantiated as 800GAUI-
8, the PMA shall meet the electrical and timing specifications as specified in Annex 120F
or Annex 120G as appropriate at the service interface below the PMA."
If the interface between the sublayer below the PMA and the PMA is physically instantiated
as 800GAUI-8, the PMA shall meet the electrical and timing specifications as specified in
Annex 120F or Annex 120G as appropriate at the service interface below the PMA."

[Editor's note: page was changed from 180 to 183.]
This is a PMA. On the receive side, it doesn't know and can't control the PCSLs of the signals it carries.

**Suggested Remedy**

Replace this with a practical criterion to ensure that the reduced transition density doesn't happen, if any is needed, e.g. that each of the 8 outputs is derived from four contiguous lanes in the set of 32 incoming PMA lanes. There is negligible benefit in the 4-FEC multiplexing on the receive side because there are only PMAs that can make more errors after this, and their maximum error ratios are far lower than the PMD's.

**Proposed Response**

PROPOSED REJECT.

Subclause 173.4.2.2 is specifically referring to the 8:32 PMA. The 8:32 PMA is always required to be co-located with a PHY 800GXS below it (see 173.1.4). In the receive direction, this PMA receives 32 parallel bit streams from the PHY 800GXS. Each one of the 32 bit streams is a specific PCSL. The PMA is therefore able to identify the specific PCSLs it is receiving from the PHY 800GXS (from the "PHY_XS:IS_UNITDATA_0:31.indication" service interface primitive). This is identical to the transmit direction of the 32:8 PMA where this PMA receives 32 parallel bit streams from the 800GBASE-R PCS above it.

The interleaving can thus perform the constrained PCSL multiplexing in accordance with slides 17 and 18 in the adopted PCS/PMA baseline (https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf).

The clock content mentioned in the suggested remedy are addressed in comments #166, 169, 126, and 127.

**Comment Status**

D

**Response Status**

W

**Proposed Response**

PROPOSED REJECT.

Subclause 173.4.2.3 is specifically referring to the 8:32 PMA. The 8:32 PMA is always required to be co-located with a PHY 800GXS below it (see 173.1.4). In the receive direction, this PMA receives 32 parallel bit streams from the PHY 800GXS. Each one of the 32 bit streams is a specific PCSL. The PMA is therefore able to identify the specific PCSLs it is receiving from the PHY 800GXS (from the "PHY_XS:IS_UNITDATA_0:31.indication" service interface primitive). This is identical to the transmit direction of the 32:8 PMA where this PMA receives 32 parallel bit streams from the 800GBASE-R PCS above it.

The interleaving can thus perform the constrained PCSL multiplexing in accordance with slides 17 and 18 in the adopted PCS/PMA baseline (https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf).

The clock content mentioned in the suggested remedy are addressed in comments #166, 169, 126, and 127.

**Comment Status**

D

**Response Status**

W

**Proposed Response**

PROPOSED REJECT.

"The order of PCSLs from an input lane does not have to be maintained on the output lane" is this enough to exclude the reduced transition density issue? If not, it can be tightened to require the lanes remain in the same or reversed order, not re-ordered about any old how.

**Proposed Response**

PROPOSED REJECT.

Resolve using the response to comment #167.

"group of PMAs" puzzled me. PMAs are not used in parallel.

**Proposed Response**

PROPOSED REJECT.

The text is consistent with subclauses 120.5.3.5 and 83.5.3.6 in the base standard and is accurate as written. The proposed changes do not improve the accuracy or clarity of the text.

**Comment Status**

D

**Response Status**

W

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

The base standard is ambiguous about whether precoding should be applied to the PAM4 patterns specified in 120.5.11.2. All patterns other that PRBS31Q are used only in transmitter tests and thus should be used without precoding enabled. The PRBS31Q pattern, which is specified for receiver stress testing, may be used with or without precoding based on AUI or PMD type and the receiver preference.

An editorial presentation will be provided showing the proposed changes. Note that comment #175 address missing control bit to enable precoding on the PMA receive output and transmit input.
IEEE P802.3df D1.0 1st Task Force review comments

**Comment Type** T  Comment Status D (bucket1)

"Mapping of MDIO control variables to PMA control variables is shown in Table 173–2. Mapping of MDIO status variables to PMA status variables is shown in Table 173–3." But status and control go in opposite directions.

**Suggested Remedy**
Mapping of PMA status variables to MDIO status variables is shown in Table 173–3. Similarly in next sentence.

**Proposed Response**

**Response Status** W

PROPOSED REJECT.
The wording is consistent with similar subclauses in multiple clauses in the base standard and is accurate as written. The proposed changes do not improve the accuracy or clarity of the text.

**Comment Type** E

**Comment Status** D (bucket1)

PRBS Tx pattern testing

**Suggested Remedy**
PRBS Tx pattern testing error counter

**Proposed Response**

**Response Status** W

PROPOSED ACCEPT IN PRINCIPLE.
Change "PRBS Tx pattern testing" to "PRBS Tx pattern testing error counter, lane 0 to lane 7"
Change "PRBS Rx pattern testing" to "PRBS Rx pattern testing error counter, lane 0 to lane 7"

**Comment Type** E

**Comment Status** D (bucket1)

This project is lengthening this title but a five-line title is too long. If we had 16 x 100G AUs it would be even worse.

**Suggested Remedy**
Name it the way we name PMD clauses: Chip-to-chip 100 Gb/s/lane Attachment Unit Interfaces type 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C
Similarly for 120G

**Proposed Response**

**Response Status** W

PROPOSED ACCEPT IN PRINCIPLE.
The titles are indeed long and can be shortened and clarified.
The suggested remedy introduces the word "Type", which has been used for PHY but not for AUIs. Therefore a slight modification is proposed.
The same form used for PMD clause titles can be used.

Change the title of Annex 120F to:
"Chip-to-chip Attachment Unit Interfaces 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C"
Change the title of Annex 120G to
"Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M"
Change the titles of 120F.5, 120F.5.4, 120G.6, 120G.6.4, the text in 120F.5.1 and 120G.6.1, and the tables in 120F.5.2.1 and 120G.6.2.1, accordingly.
Change any text affected by these title changes with editorial license.
120.5.7.2 doesn't address precoding in C2C

Suggested Remedy
Delete the reference here or change 120.5.7.2

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.

It appears that 120.5.7.2 was not updated to include support for 100GBASE-1, 200GAUI-2, and 400GAUI-4. The subclause needs to be updated to support optional precoding on all inputs and outputs including control registers. An editorial presentation will be provided showing the proposed changes.

100GAUI-1, 200GAUI-2, 400GAUI-4 C2M data path contains one, two, four, "or" eight differential lanes

Suggested Remedy
Change and to or

Proposed Response
PROPOSED ACCEPT.

As dealing with larger numbers of lanes in compliance boards is an engineering issue... And by the way, it might have been helpful to show that these are differential.

Suggested Remedy
It would help to add the short diagonal lines showing n lanes. Also Figure 120G-4

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.

The test points are separate for each lane. However, the clarity of the figure may be improved. Add the label "(one per lane)" below TP1a and TP4a in Figure 120G-3, and below TP1 and TP4 in Figure 120G-4. In the second and third paragraphs of 120G.2, change "the location of compliance points" to "the location of compliance points for each lane".
"distributed in a round-robin fashion into two parallel transmit functions": sort of slang. Where I come from, all robins look round.

Suggested Remedy

Change "a round-robin fashion" to "an alternating fashion" here; in 172.2.4.1, change "a round robin fashion" to "an alternating fashion". Similarly in 172.2.5.8.

PROPOSED ACCEPT IN PRINCIPLE.

This is a new function where 64B/66B blocks are distributed between or combined from two streams or flows, so "alternating" seems more appropriate here than "round-robin". The details of the distribution are not necessary in the summary, but in the detailed functional description "round-robin" should be replaced with "alternating".

In 172.2.1 on page 163 line 19...

Change:
"The 66-bit blocks are then distributed in a round-robin fashion into two parallel transmit functions, referred to as flow 0 and flow 1."
To:
"The 66-bit blocks are then distributed between two parallel transmit functions, referred to as flow 0 and flow 1."

In 172.2.1 on page 163, line 42
Change:
"A 66-bit block collection function merges the 66-bit blocks from the two flows in a round-robin fashion into a single stream of blocks that are then 64B/66B decoded."
To:
"A 66-bit block collection function merges the 66-bit blocks from the two flows into a single stream of blocks that are then 64B/66B decoded."

In 172.2.4.1 on page 164, line 23...

Change:
"The 66-bit blocks are distributed to the two flows in a round robin fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue the round robin distribution procedure across the two flows."
To:
"The 66-bit blocks are distributed to the two flows in an alternating fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue the distribution procedure across the two flows."

In 172.2.5.8 on page 168, line 21
Change: "The block collection reverses the block distribution done in the transmitter (see 172.2.4.1) by combining the 66-bit blocks from the two flows in a round robin fashion to form a single stream of 66-bit blocks."
To: "The block collection reverses the block distribution done in the transmitter (see 172.2.4.1) by combining the 66-bit blocks from the two flows in an alternating fashion to form a single stream of 66-bit blocks."

In 172.2.4.1 on page 163, line 42
Change:
"Within each flow, the 66-bit blocks are transcoded to 257-bit blocks, scrambled, and alignment markers are periodically added to the data stream."
To:
"Within each flow, the 66-bit blocks are transcoded to 257-bit blocks, scrambled, and alignment markers are periodically added to the data stream."

Suggested Remedy

Modify this to say that the insertion of alignment markers is not independent for each flow.

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #90.

In 172.2.1 on page 163, line 22
Change:
"The data stream is distributed to two 5140-bit blocks and then FEC encoded. The two FEC codewords are then interleaved before data is distributed to individual PCS lanes."
To:
"For each flow, the data stream is distributed to two 5140-bit blocks and then FEC encoded. For each flow, the two FEC codewords are then interleaved before data is distributed to individual PCS lanes."

PROPOSED ACCEPT IN PRINCIPLE.

Replace
"The data stream is distributed to two 5140-bit blocks and then FEC encoded. The two FEC codewords are then interleaved before data is distributed to individual PCS lanes."
with
"For each flow, the data stream is distributed to two 5140-bit blocks and then FEC encoded. For each flow, the two FEC codewords are then interleaved before data is distributed to individual PCS lanes."

Comment ID 181 Page 41 of 45 2022-11-28 1:47:13 PM
Use of blocks - ambiguous: there are 257-bit blocks as well as FEC blocks, even if we call those "codewords". This title dates from 49.2.3 Use of blocks, before 257-bit blocks and FEC.

**Suggested Remedy**

Change "blocks" to "66-bit blocks" here and at line 49.

**Proposed Response**

Proposed Accept in Principle.

Implement the suggested remedy with editorial license.

The curly brackets must be trying to tell the reader something, but I don't know what.

**Suggested Remedy**

Delete them, or define what they mean, or change to some notation that is defined.

**Proposed Response**

Proposed Reject.

The curly brackets in Tables 172-1 and 172-2 are consistent with what was used in Table 119-2 in Clause 119. Given that we are striving for consistency between this new and previous PCS specifications, retaining a common format is helpful for comparison.

The comment does not provide sufficient justification to make the suggested change nor do the proposed changes improve the accuracy or clarity of the draft.

The format used in Table 172-1 and Table 172-2 is consistent with the format used in Table 119-2 in Clause 119. Given that we are striving for consistency between this new and previous PCS specifications, retaining a common format is helpful for comparison.

The comment does not provide sufficient justification to make the suggested change nor do the proposed changes improve the accuracy or clarity of the draft.

The comment does not provide sufficient justification to make the suggested change nor do the proposed changes improve the accuracy or clarity of the draft.

The functions above the "64B/66B to 256B/257B transcoder" are excluded.

**Proposed Response**

Proposed Accept in Principle.

Change from "The functions above the "64B/66B to 256B/257B transcoder" are excluded." to "The portion of the figure above the "64B/66B to 256B/257B transcoder" is excluded".

Comment ID: 185  Page: 42 of 45  Date: 2022-11-28 1:47:13 PM

**Comment Status**:

- **TYPE**: TR/technical required
- **ER**: editorial required
- **GR**: general required
- **T**: technical
- **E**: editorial
- **G**: general
- **Comment Status**: D/dispatched A/accepted R/rejected
- **RESPONSE STATUS**: O/open W/written C/closed Z/withdrawn
- **SORT ORDER**: Comment ID
Comment Type: E  Comment Status: D  test pattern (CC)

"Test-pattern generators are identical to that specified in 119.2.4.9" there is only one test pattern, and although it is generated in an analogous way to 119.2.4.9, it's a different PCS and different bits in the pattern.

Suggested Remedy
Change to "A scrambled idle test pattern can be generated in the same way in the same way as in 119.2.4.9".

Proposed Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Change from
"Test-pattern generators are identical to that specified in 119.2.4.9" to
"The scrambled idle test pattern functionality is identical to that specified in 119.2.4.9".

Comment Type: E  Comment Status: D  bucket1
The relation between hi_ser_0, hi_ser_1 and hi_ser appears later within a state machine variable definition, which is too obscure. More generally, I could not find where the purpose of hi_ser is introduced.

Suggested Remedy
Add something in regular text (possibly elsewhere) that says that what hi_ser for, and that it is the OR of hi_ser_0 and hi_ser_1.

Proposed Response  Response Status: W
PROPOSED REJECT.
172.2.5.3 notes the exception that each flow has a unique hi_ser generated by its FEC decoder (hi_ser_0 and hi_ser_1). The purpose of hi_ser is defined in 119.2.5.3.
Comment ID 190

Dawe, Piers  
Nvidia

Comment Type T  
Comment Status D (bucket1)

“A ... PMA is required to support an physical instantiation of the PMA service interface”: doesn’t make sense, as the PMA service interface is part of the PMA. an vs. a.

Suggested Remedy

is used to implement a ...?

Proposed Response  
Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change from:
“An 8:8 PMA is required to support an physical instantiation of the PMA service interface (800GAUI-8)”

to
“An 8:8 PMA is required for a physical instantiation of the PMA service interface (800GAUI-8)”

Comment ID 191

Dawe, Piers  
Nvidia

Comment Type T  
Comment Status D (bucket1)

“The PMA receives”: confusing and incomplete.

Suggested Remedy

In the transmit direction, the PMA receives 32 parallel bit streams, each at the nominal signaling rate of the PCSL. In the receive direction, it delivers 32 parallel bit streams to its client. Similarly in the next paragraph for an 8-lane interface.

Proposed Response  
Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change from
“The PMA receives 32 parallel bit streams, each at the nominal signaling rate of the PCSL.”

to
“In the transmit direction, the PMA receives 32 parallel bit streams from either the 800GBASE-R PCS or the DTE 800GXS, each at the nominal signaling rate of the PCSL. In the receive direction, the PMA sends 32 parallel bit streams to the PMA client, each at the nominal signaling rate of the PCSL.”

Change from
“The PMA receives PAM4 symbols on each of its input lanes at two times the PCSL rate, each symbol formed from two bits.”

to
“In the transmit direction, the PMA receives 8 parallel PAM4 symbol streams from the PMA client, each at a nominal signaling rate of 53.125 Gb/s. In the receive direction, the PMA sends 8 parallel PAM4 symbol streams to the PMA client, each at a nominal signaling rate of 53.125 Gb/s.”

Comment ID 192

Nicholl, Gary  
Cisco Systems

Comment Type E  
Comment Status D (bucket1)

Table 167-7. The order of the PMDs in the “Signaling rate” row is different from what was done in Clause 124.

Suggested Remedy

Proposing to reorder the data in this row to put the lower speed and lower lane count PMDs first, i.e.
“800GBASE-VR8, 800GBASE-SR8 PMDs”

Proposed Response  
Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change the order and associated parameters as proposed.

Comment ID 193

Nicholl, Gary  
Cisco Systems

Comment Type E  
Comment Status D (bucket1)

Table 167-8. The order of the PMDs in the “Signaling rate” row is different from what was done in Clause 124.

Suggested Remedy

Proposing to reorder the data in this row to put the lower speed and lower lane count PMDs first, i.e.
“Other PMDs”
“800GBASE-VR8, 800GBASE-SR8 PMDs”

Proposed Response  
Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change the order and associated parameters as proposed.
Proposed Response  

**Comment Type**  E  
**Comment Status**  D  
**Cl**  167  SC  167.8.6  P  118  L  6  
Nicholl, Gary  Cisco Systems  

Table 167-12. The font for the text in the "PMD Type" column looks incorrect. Also the editing instruction is "change this table", but then no underline or strickthrough. Perhaps the editing instruction should have been "Replace Table 167-12 with the following:"  

SuggestedRemedy  

Change the font in the "PMD Type" column to use the standard table font and update the editing instruction to "Replace Table 167-12 with the following:"  

PROPOSED ACCEPT IN PRINCIPLE.  

Comment Status  D  
Response Status  W  

Nicholl, Gary  Cisco Systems  

---  

**Comment Type**  E  
**Comment Status**  D  
**Cl**  171  SC  171.2  P  150  L  4  
Nicholl, Gary  Cisco Systems  

800GXS should be 400GXS  

SuggestedRemedy  

Change "PCS and 800GXS sublayers specified in 118.2" to "PCS and 400GXS sublayers specified in 118.2"  

PROPOSED ACCEPT.  

---  

**Comment Type**  E  
**Comment Status**  D  
**Cl**  173  SC  173.4  P  182  L  38  
Nicholl, Gary  Cisco Systems  

Figure 173-4 (8:32 PMA) there should be no PMA:IS_SIGNAL.indication towards the PMA (AUI is not able to transfer an out of band status signal) and possibly no "SIL" block in the block diagram.  

The same comment applies to the 8:8 PMA in Figure 173-5.  

SuggestedRemedy  

Remove the PMA:IS_SIGNAL.indication signal and the "SIL" block from Figure 173-4 and Figure 173-5.  

PROPOSED ACCEPT IN PRINCIPLE.  

The editors noted this error during the implementation of D1.0, but discovered it too late to address it properly.  

A presentation will be provided for task force discussion.  

---  

**Comment Type**  E  
**Comment Status**  D  
**Cl**  173  SC  173.4  P  181  L  40  
Nicholl, Gary  Cisco Systems  

Figure 173-3/4/5. Need to make it clear if the sublayer above or below is another PMA , that the interface is connected over a physically instanitated AUI (800GAUI-8)  

SuggestedRemedy  

Update Figure 173-3/4/5 to make it clear if the sublayer above or below is another PMA , that the interface is connected over a physically instanitated AUI (800GAUI-8)  

PROPOSED ACCEPT IN PRINCIPLE.  

Resolve using the response to comment #196.