Cl **124** *SC* **124.5.4** *P* **106** *L* **10** # 84

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **R** *launch power*

The same modules will be capable of any of 100GBASE-DR, 400GBASE-DR4, 800GBASE-DR8, 100GBASE-FR1, 400GBASE-DR4-2, 800GBASE-DR8-2. Nominal nearly-compliance for a virtually unusable 0.2 dB on an unimportant spec would make the market more complicated and add procedural cost.

SuggestedRemedy

In the longer term, the average launch power (min) for 100GBASE-FR1 should be increased from -3.1 to -2.9 dBm to bring it in line with 100GBASE-DR/400GBASE-DR4. In the meantime: add a recommendation that the SIGNAL_DETECT power criterion for 800GBASE-DR8, 400GBASE-DR4-2 and 800GBASE-DR8-2 (which is: >= average receive power, each lane (min) in Table 124-7) should be -7.1 dBm.
In practice, module implementers will set it lower than this anyway. See other comments for Tx and Rx specs, and for interoperability text.

Response *Response Status* **U**

REJECT.

The fact that modules meet several compatible specifications simultaneously is a choice of the implementer, not a requirement from the standard.

The suggested remedy refers to a modification of 100GBASE-FR1 which is outside the scope of this project.

Furthermore insufficient justification is provided why the proposed remedy is an improvement of the draft.

The following presentation was reviewed by the comment resolution group:
https://www.ieee802.org/3/df/public/23_0523/dawe_3df_01_230523.pdf

Cl **124** *SC* **124.7.1** *P* **108** *L* **23** # 85

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **R** *launch power*

The minimum OMA for 400GBASE-DR4-2 and 800GBASE-DR8-2 is 0.7 dB higher than for 400GBASE-DR4/100GBASE-DR and 800GBASE-DR8, so setting the average launch power 0.2 dB lower is not helpful. Any transmitter with an extinction ratio lower than 9.8 dB, which is very high, will exceed the 400GBASE-DR4 limit anyway. Modules will be made multi-compliant for convenience in interoperability and breakout - let us document that.
There is a minor benefit in improving the clearance between Rx min power and Tx off max power, which should be very wide to accomodate better-than-worst receivers and intentional signal detect hysteresis.

SuggestedRemedy

Change Average launch power, each lane (min) from -3.1 to -2.9 dBm
Change Average receive power, each lane (min) from -7.1 to -6.9 dBm.
See another commen for interoperability text.

Response *Response Status* **U**

REJECT.

There is a historical background why the minimum average power does not seem consistent across PMD types. This is related to the assumption of an extinction ratio of 10 dB for the calculation of minimum average power from minimum OMA for 400GBASE-DR4 (and 800GBASE-DR8), while for the 400GBASE-DR4-2 and 800GBASE-DR8-2 the extinction ratio is assumed to be infinity.

There is no interoperation issue. The requirements for interoperation are provided in 124.11a.1 and 124.11a.2.

The following presentation was reviewed by the comment resolution group:
https://www.ieee802.org/3/df/public/23_0523/dawe_3df_01_230523.pdf

Cl **124** *SC* **124.11a.1** *P* **122** *L* **21** # 86

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **R** *average power*

We have a nuisance exception "provided that ... the 400GBASE-DR4-2 transmitter average power is greater than or equal to the value for average launch power (min) for 400GBASE-DR4 in Table 124-6" that adds procedural cost for no technical benefit.

SuggestedRemedy

Having made the minimum 400GBASE-DR4-2 transmitter average power the same as for 400GBASE-DR4 (see another comment), delete "and the 400GBASE-DR4-2 transmitter average power is greater than or equal to the value for average launch power (min) for 400GBASE-DR4 in Table 124-6."
Similarly in 124.11a.2.

Response *Response Status* **U**

REJECT.

See response to comment #85.

Since comment #85 was rejected this comment is no longer relevant.

The following presentation was reviewed by the comment resolution group:
https://www.ieee802.org/3/df/public/23_0523/dawe_3df_01_230523.pdf

Cl **169** *SC* **169.5** *P* **180** *L* **9** # 96

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **A** *skew (CC)*

As discussed, the Skew and Skew Variation limits were based on a digital clock rate that is slow by modern standards, and CWDM over 40 km which is not going to happen for 800G. Also they were heavily sandbagged. It is important to sort this out for 800G so that the future 200G/lane-based Ethernet is not locked into decisions made long ago for technology that doesn't apply in this case.

SuggestedRemedy

Continue the investigation, revise the numbers according to relevant technology, take out some of the padding.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #81.