Cl **172A**   *SC* **172A**   *P***282**   *L***51**   # R1-39

Dawe, Piers J G   NVIDIA

Comment Type **TR**   *Comment Status* **R**   *(bucket2)*

Experience with Annex 172A shows us how valuable it is. But more complexity follows: twice "Mux and 10-bit symbol distribution" as in 119.2.4.8 Figure 119-11 (with an order reversal that doesn't seem to be mentioned in the text), then 32:8 bit mux as in 173.5.2.1 where the two flows get interleaved, which is a new thing and worth an example.

SuggestedRemedy

Show some of the 16+16-lane output of the PCS for these cxA and cxB. It may be enough to show e.g. the beginnings of lanes 1 and 31, enough to include some differences between four codewords.
Also show some of the 8-lane output of an 32:8 bit mux from that (which could go in a NOTE in 173). Again, showing a couple of lanes would be enough to resolve most or all misinterpretations or ambiguities. Add a cross-reference from here.
If only a few hundred bits are needed, it could go in text. But if a more complete example is preferred, tables could be added and plain-text equivalents uploaded.

Response   *Response Status* **U**

REJECT.

The example patterns are provided to help the implementer confirm correct interpretation of the encoding funcitonality which is complex.

Figure 119-11 provides sufficient guidance to correctly implement "Mux and 10-bit symbol distribution". Therefore adding the suggested additional patterns is not necessary.

There is no consensus to make the proposed changes.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Comment ID

Comment ID **R1-39**   Page 1 of 1
11/15/2023 8:57:05 AM