Cl **45** *SC* **45.2.5.15** *P* **79** *L* **4** # R2-15

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

Putting "bit" on a new line looks odd

SuggestedRemedy

The text box for the figure title should be full width. Same issue on next page.

Proposed Response *Response Status* **O**

Cl **124** *SC* **124.7** *P* **110** *L* **22** # R2-5

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

Table title is strangely offset to the right. This might be related to the formatting in the base document for multiple tables in Clause 124.

SuggestedRemedy

The text box for the figure titles should be full width. Same issue on next page.

Proposed Response *Response Status* **O**

Cl **124** *SC* **124.7.1** *P* **111** *L* **49** # R2-7

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

Bottom border of a table to be continued

SuggestedRemedy

should be thin.

Proposed Response *Response Status* **O**

Cl **124** *SC* **124.7.1** *P* **112** *L* **40** # R2-2

Dudek, Michael Marvell

Comment Type **E** *Comment Status* **X**

In the .pdf version of the draft and also the .pdf version of the compare draft the axis labelling of Figure 124-2a is unreadable. It was correct in draft 3.1.

SuggestedRemedy

Replace this figure with the one from draft 3.1

Proposed Response *Response Status* **O**

Cl **124** *SC* **124.7.2** *P* **114** *L* **46** # R2-3

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

For 400GBASE-DR

SuggestedRemedy

For 400GBASE-DR4

Proposed Response *Response Status* **O**

Cl **124** *SC* **124.7.2** *P* **114** *L* **46** # R2-4

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

"For 400GBASE-DR receiver sensitivity (OMAouter), each lane (max) is optional" but the lanes are not optional.

SuggestedRemedy

Insert a comma after DR. For consistency, insert a comma in Table 124-6 footnote c.

Proposed Response *Response Status* **O**

Cl **124** *SC* **124.7.2** *P* **115** *L* **9** # R2-10

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

Font or character problem, axes values and labels

SuggestedRemedy

Fix. Also Figure 124-2c and 2d.

Proposed Response *Response Status* **O**

Cl **169** *SC* **169.1.2** *P* **176** *L* **36** # R2-17

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **X**

We show the sublayer stack in the first figure of each "Introduction to <MAC rate>" clause and the first figure of each sublayer clause in its overview. Usually we include all relevant sublayers, which this gives the reader a familiar map to give the clause context. See figures 69-1, 80-1, 81-1, 82-1, 83-1, 91-1, for example. Also 105 106 107 108 109 for 25G, 131 132 133 134 135 for 50G.
This consistency should be maintained unless changed through the maintenance process. There are few exceptions: when 116, 117, 118, 119 and 120 for 200 Gb/s and 400 Gb/s were written, the first wave of PHYs had no AN, and 3ck did not add them to these diagrams, although AN is included in Figure 161-1 (RS-FEC-Int).

SuggestedRemedy

Add the missing AN sublayer to Figure 169-1 (introduction to 800 Gb/s), like 80, 105, 131. It may be advisable to revert "800GBASE" to "800GBASE-R" for consistency; any future project with a non-BASE-R 800G PHY may choose its own layer stack.
Add the missing AN sublayer to Figure 170-1 (RS and 800GMII), like 81, 106, 132.
Add the missing AN sublayer to figures 171-1 and 3 (800GMII Extender and 800GXS) for consistency.
Add the missing AN sublayer to Figure 172-1 (PCS), like 82, 107, 133.
Add the missing AN sublayer to Figure 173-1 (PMA), like 83, 109, 134.
Either now or via maintenance, (maybe to be implemented in 3dj), insert the missing AN in figures 1 of 116, 117, 118, 119 and 120.

Proposed Response *Response Status* **O**

Cl **171** *SC* **171.6.1** *P* **200** *L* **35** # R2-6

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

"where ... are defined in 172.2.6.2.2 and + ..." could be improved. If this were a formal equation, each "where" item would go on a separate line.

SuggestedRemedy

Insert a comma after 172.2.6.2.2. Also in 172.2.4.6.

Proposed Response *Response Status* **O**

Cl **172** *SC* **172.2.4.1** *P* **219** *L* **10** # R2-22

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **X**

Figure 119-11, 400GBASE-R Transmit bit ordering and distribution, is not consistent.

SuggestedRemedy

There should be a box with tx_scrambled_am in it as there is for tx_xcoded and tx_scrambled, with the two ends numbered and an arrow coming out of one end to "10-bit round robin distribution" so that the order is clear.

Proposed Response *Response Status* **O**

Cl **172** *SC* **172.2.4.1** *P* **219** *L* **10** # R2-24

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **X**

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. Figure 119-11 implies that bit 0 (rather than 9) of a 10-bit symbol in a FEC codeword goes to the PMA first but there is no indication of what that means, and whether it corresponds to a bit 0 or a bit 9 of tx_scrambled_am.

SuggestedRemedy

Define the bit ordering.

Proposed Response *Response Status* **O**

Cl **172** *SC* **172.2.4.1** *P* **219** *L* **10** # R2-23

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **X**

As this Figure 119-11 is called "Transmit bit ordering..."

SuggestedRemedy

The arrows from "10-bit round robin distribution" should not go to the middles of the FEC messages but to the appropriate end to show which way the FEC messages are filled.

Proposed Response *Response Status* **O**

Cl **172** *SC* **172.2.4.1** *P* **219** *L* **10** # R2-18

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **X**

In Figure 119-11 400GBASE-R Transmit bit ordering and distribution, c_A29 = m_A0

SuggestedRemedy

This should say c_A30 = m_A0, as in Figure 119-10 200GBASE-R Transmit bit ordering and distribution.

Proposed Response *Response Status* **W**

Cl **172** *SC* **172.2.4.1** *P* **219** *L* **10** # R2-19

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **X**

Figure 119-11, 400GBASE-R Transmit bit ordering and distribution

SuggestedRemedy

should show am_mapped as another box under tx_scrambled, with an arrow indicating input to "AM Insertion" (indicating the order).

Proposed Response *Response Status* **W**

Cl **172** *SC* **172.2.4.1** *P* **219** *L* **35** # R2-14

Dawe, Piers J G NVIDIA

Comment Type **T** *Comment Status* **X**

Unlike Figure 119-10, there is nothing about bit ordering in Figure 172-4. It's all by reference to Figure 119-10.

SuggestedRemedy

Move the arrow beside "66-bit blocks" to show which end of a 66-bit block goes first, or change the figure title from "800GBASE-R PCS transmit bit ordering and distribution" to "800GBASE-R PCS transmit distribution"

Proposed Response *Response Status* **W**

Cl **172** *SC* **172.2.4.6** *P* **215** *L* **28** # R2-20

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

Figure 119-7, 400GBASE-R alignment marker mapping to PCS lanes, shows "A = from FEC codeword A B = from FEC codeword B". But this is AM creation, part of the Transmit function. AMs are not from the FEC codewords here, they go into them.

SuggestedRemedy

"from" should be "to", twice.

Proposed Response *Response Status* **W**

Cl **172** *SC* **172.2.4.8** *P* **218** *L* **50** # R2-13

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **X**

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. It turns out that the order of the bits in each 10-bit FEC symbol going into the FEC and coming out of it is not specified in 119. The examples in 172A show what is given to the FEC and what two FEC-coded codeword within the FEC are, but not what is just after the FEC - and it's only informative.
For example, here is what Clause 91 says:
The message symbols are composed of the bits of the transcoded blocks tx_scrambled (including a mapped group of alignment markers when appropriate) such that bit 0 of the first transcoded block in the message (or am_txmapped<0>) is bit 0 of m_k–1 and bit 256 of the last transcoded block in the message is bit 9 of m_0.

SuggestedRemedy

Define the order the bits in each 10-bit FEC symbol going into the FEC and coming out of it.
Provide an example of the output of the FEC after 10-bit interleaving "tx_out", which is after translation from the ordering/numbering that the FEC uses to what most of the PCS uses.

Proposed Response *Response Status* **W**

Cl **172** *SC* **172.2.4.9** *P* **219** *L* **3** # R2-21

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **X**

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. Confusion between tx_out the 1088 x 10 array in 119.2.4.7 and tx_out<0:16> the contents of the 16 PCS lanes in Figure 119-11.

SuggestedRemedy

As these seem to be different things, they should have different names.

Proposed Response *Response Status* **O**

Cl **172** *SC* **172.2.4.10** *P* **219** *L* **22** # R2-25

Ran, Adee Cisco Systems, Inc.

Comment Type **E** *Comment Status* **X**

The label "tx_coded<0>" on the left overlaps the block.

SuggestedRemedy

Move the label leftward so that it does not overlap.

Proposed Response *Response Status* **O**

Cl **172** *SC* **172.3.2** *P* **230** *L* **13** # R2-1

Rannow, R K IEEE member / Self Employed

Comment Type **T** *Comment Status* **X**

Inconsistent use of the term "both". Used as an adverb and predeterminer, and this may create ambiguity.

172.3.2 FEC_corrected_cw_counter FEC_corrected_cw_counter is identical to 119.3.2 with the clarification that the count includes both flows.
172.3.3 FEC_uncorrected_cw_counter FEC_uncorrected_cw_counter is identical to 119.3.3 with the clarification that the count includes both flows.

SuggestedRemedy

Recommend consistency throughout to document as an adverb.

Proposed Response *Response Status* **O**

Cl **172A** *SC* **172A** *P* **287** *L* **22** # R2-9

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

Another reference would make this easier to use, so the reader can find what "am_mapped" and "tx_scrambled_am" at lines 29, 30 are (am_mapped does not appear in this amendment anywhere else, and while values for tx_scrambled_am are given in the tables, there is no indication of what it is).

SuggestedRemedy

Please insert (see 172.2.4.6) after alignment marker.

Proposed Response *Response Status* **O**

Cl **172A** *SC* **172A** *P* **287** *L* **52** # R2-12

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **X**

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. This says that 10 bits of cx_A (in reverse order) is one symbol of c_A. It is not clear whether the reverse order is telling the reader to reverse the order, or it is just weird notation. Also the order of the bits in a symbol of C_A is not given.

SuggestedRemedy

Explain the bit and symbol ordering using words.

Proposed Response *Response Status* **W**

Cl **172A** *SC* **172A** *P* **288** *L* **19** # R2-8

Dawe, Piers J G NVIDIA

Comment Type **E** *Comment Status* **X**

tx_scrambled

SuggestedRemedy

Should be tx_scrambled_am as in the column header. Fig 119-11 shows that these are different things. Also for Table 172A-2.
Annex 119A is the same, by the way, and should be fixed sometime.

Proposed Response *Response Status* **O**

Cl **172A** *SC* **172A** *P* **292** *L* **28** # R2-11

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **X**

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS, particularly as the numbering/ordering in the PCS generally and in the FEC (which is different) is confusing, as was recognised in 3bs.

SuggestedRemedy

Add a table here for the start of Flow 0 tx_out (16 lanes x 80 hex characters would be more than enough). Upload a plain text file to go with the others, and reference it with a NOTE here.

Proposed Response *Response Status* **O**

Cl **173** *SC* **173.5.2.1** *P* **241** *L* **28** # R2-16

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **X**

Unsatisfied D3.1 comment 39: show some of the 8-lane output of an 32:8 bit mux.

SuggestedRemedy

In a NOTE, show some of the 8-lane output of a 32:8 bit mux for the beginning of the example in Annex 172A. 8 lanes x 80 hex characters should be more than enough. Cross-reference to 172A. In 172A, cross-reference to here.

Proposed Response *Response Status* **O**