IEEE P802.3df D3.2 2nd Sponsor recirculation ballot comments

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**Cl 45 SC 45.2.5.15 P79 L4** # [R2-15]

Dawe, Piers J G NVIDIA

**Comment Type E Comment Status X**

Putting "bit" on a new line looks odd

**Suggested Remedy**

The text box for the figure title should be full width. Same issue on next page.

**Proposed Response Response Status O**

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**Cl 124 SC 124.7 P110 L22** # [R2-5]

Dawe, Piers J G NVIDIA

**Comment Type E Comment Status X**

Table title is strangely offset to the right. This might be related to the formatting in the base document for multiple tables in Clause 124.

**Suggested Remedy**

The text box for the figure titles should be full width. Same issue on next page.

**Proposed Response Response Status O**

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**Cl 124 SC 124.7.1 P111 L49** # [R2-7]

Dawe, Piers J G NVIDIA

**Comment Type E Comment Status X**

Bottom border of a table to be continued

**Suggested Remedy**

should be thin.

**Proposed Response Response Status O**

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**Cl 124 SC 124.7.1 P112 L40** # [R2-2]

Dudek, Michael Marvell

**Comment Type E Comment Status X**

In the .pdf version of the draft and also the .pdf version of the compare draft the axis labelling of Figure 124-2a is unreadable. It was correct in draft 3.1.

**Suggested Remedy**

Replace this figure with the one from draft 3.1

**Proposed Response Response Status O**

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**Cl 124 SC 124.7.2 P114 L46** # [R2-3]

Dawe, Piers J G NVIDIA

**Comment Type E Comment Status X**

For 400GBASE-DR

**Suggested Remedy**

For 400GBASE-DR4

**Proposed Response Response Status O**

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**Cl 124 SC 124.7.2 P114 L46** # [R2-4]

Dawe, Piers J G NVIDIA

**Comment Type E Comment Status X**

"For 400GBASE-DR receiver sensitivity (OMAouter), each lane (max) is optional" but the lanes are not optional.

**Suggested Remedy**

Insert a comma after DR. For consistency, insert a comma in Table 124-6 footnote c.

**Proposed Response Response Status O**
### Comment Type: E/Editorial Required

**Comment Status:** X

**Font or character problem, axes values and labels**

**Suggested Remedy:** Fix. Also Figure 124-2c and 2d.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**We show the sublayer stack in the first figure of each "Introduction to <MAC rate>" clause and the first figure of each sublayer clause in its overview. Usually we include all relevant sublayers, which this gives the reader a familiar map to give the clause context. See figures 69-1, 80-1, 81-1, 82-1, 83-1, 91-1, for example. Also 105 106 107 108 109 for 25G, 131 132 133 134 135 for 50G.**

This consistency should be maintained unless changed through the maintenance process. There are few exceptions: when 116, 117, 118, 119 and 120 for 200 Gb/s and 400 Gb/s were written, the first wave of PHYs had no AN, and 3ck did not add them to these diagrams, although AN is included in Figure 161-1 (RS-FEC-Int).

**Suggested Remedy:**

- Add the missing AN sublayer to Figure 169-1 (introduction to 800 Gb/s), like 80, 105, 131.
- Define the bit ordering.

**Proposed Response**

<table>
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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**Non-BASE-R 800G PHY may choose its own layer stack.**

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS.**

**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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**Comment Status:** X

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**Figure 119-11, 400GBASE-R Transmit bit ordering and distribution, is not consistent.**

**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS.**

**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

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**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

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**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS.**

**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS.**

**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA

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### Comment Type: TR/Technical Required

**Comment Status:** X

**Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS.**

**Suggested Remedy:**

- Define the bit ordering.

**Proposed Response**

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**Response Status:** O

**Dawe, Piers J G**
NVIDIA
Comment Type: T  Comment Status: X  
As this Figure 119-11 is called "Transmit bit ordering..."

Suggested Remedy
The arrows from "10-bit round robin distribution" should not go to the middles of the FEC messages but to the appropriate end to show which way the FEC messages are filled.

Proposed Response

Response Status: O

Proposed Response

Comment Type: T  Comment Status: X
In Figure 119-11 400GBASE-R Transmit bit ordering and distribution, c_A29 = m_A0

Suggested Remedy
This should say c_A30 = m_A0, as in Figure 119-10 200GBASE-R Transmit bit ordering and distribution.

Proposed Response

Response Status: W

Proposed Response

Comment Type: E  Comment Status: X
Figure 119-7, 400GBASE-R alignment marker mapping to PCS lanes, shows "A = from FEC codeword A B = from FEC codeword B". But this is AM creation, part of the Transmit function. AMs are not from the FEC codewords here, they go into them.

Suggested Remedy
"from" should be "to", twice.

Proposed Response

Response Status: W

Proposed Response

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Clause, Subclause, page, line
Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. It turns out that the order of the bits in each 10-bit FEC symbol going into the FEC and coming out of it is not specified in 119. The examples in 172A show what is given to the FEC and what two FEC-coded codeword within the FEC are, but not what is just after the FEC - and it's only informative. For example, here is what Clause 91 says:

The message symbols are composed of the bits of the transcoded blocks tx_scrambled (including a mapped group of alignment markers when appropriate) such that bit 0 of the first transcoded block in the message (or am_txmapped<0>) is bit 0 of m_k–1 and bit 256 of the last transcoded block in the message is bit 9 of m_0.

**Suggested Remedy**

Define the order the bits in each 10-bit FEC symbol going into the FEC and coming out of it.

Provide an example of the output of the FEC after 10-bit interleaving "tx_out", which is after translation from the numbering/wording that the FEC uses to what most of the PCS uses.

---

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. Confusion between tx_out the 1088 x 10 array in 119.2.4.7 and tx_out<0:16> the contents of the 16 PCS lanes in Figure 119-11.

**Suggested Remedy**

As these seem to be different things, they should have different names.

---

Another reference would make this easier to use, so the reader can find what "am_mapped" and "tx_scrambled_am" at lines 29, 30 are (am_mapped does not appear in this amendment anywhere else, and while values for tx_scrambled_am are given in the tables, there is no indication of what it is).

**Suggested Remedy**

Please insert (see 172.2.4.6) after alignment marker.

---

The label "tx_coded<0>" on the left overlaps the block.

**Suggested Remedy**

Move the label leftward so that it does not overlap.
Comment Type: E
Comment Status: X
Suggested Remedy:
Should be tx_scrambled_am as in the column header. Fig 119-11 shows that these are different things. Also for Table 172A-2.
Annex 119A is the same, by the way, and should be fixed sometime.

Proposed Response
Response Status: O

Comment Type: TR
Comment Status: X
Suggested Remedy:
Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS, particularly as the numbering/ordering in the PCS generally and in the FEC (which is different) is confusing, as was recognised in 3bs.

Proposed Response
Response Status: O

Comment Type: TR
Comment Status: X
Suggested Remedy:
In a NOTE, show some of the 8-lane output of a 32:8 bit mux for the beginning of the example in Annex 172A. 8 lanes x 80 hex characters should be more than enough. Cross-reference to 172A. In 172A, cross-reference to here.

Proposed Response
Response Status: O