Cl **172A** *SC* **172A** *P* **292** *L* **28** # R2-11

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **R** *bit ordering*

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS, particularly as the numbering/ordering in the PCS generally and in the FEC (which is different) is confusing, as was recognised in 3bs.

SuggestedRemedy

Add a table here for the start of Flow 0 tx_out (16 lanes x 80 hex characters would be more than enough). Upload a plain text file to go with the others, and reference it with a NOTE here.

Response *Response Status* **U**

REJECT.
This comment is a restatement of comment R1-39. The resolution to comment R1-39 is recorded in the following file:
https://www.ieee802.org/3/df/comments/D3p1/8023df_D3p1_comments_final_id.pdf
The response to R1-39 is:

"REJECT.
The example patterns are provided to help the implementer confirm correct interpretation of the encoding funcitonality which is complex.
Figure 119-11 provides sufficient guidance to correctly implement "Mux and 10-bit symbol distribution". Therefore adding the suggested additional patterns is not necessary.
There is no consensus to make the proposed changes."

No new evidence has been provided to support the proposed changes.There is no consensus to make the proposed changes.

Cl **172A** *SC* **172A** *P* **287** *L* **52** # R2-12

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **R** *bit ordering*

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. This says that 10 bits of cx_A (in reverse order) is one symbol of c_A. It is not clear whether the reverse order is telling the reader to reverse the order, or it is just weird notation. Also the order of the bits in a symbol of C_A is not given.

SuggestedRemedy

Explain the bit and symbol ordering using words.

Response *Response Status* **U**

REJECT.
This comment does not apply to the substantive changes between IEEE P802.3df D3.1 and D3.2 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
The mapping is defined by the algorithm on page 287 lines 49 to 54. If this algorithm is misinterpreted by the implementer, the error would be evident by comparing the outcome to the examples provided in Annex 172A.

Cl **172** *SC* **172.2.4.8** *P* **218** *L* **50** # R2-13

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **R** *bit ordering*

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS.
It turns out that the order of the bits in each 10-bit FEC symbol going into the FEC and coming out of it is not specified in 119. The examples in 172A show what is given to the FEC and what two FEC-coded codeword within the FEC are, but not what is just after the FEC - and it's only informative.
For example, here is what Clause 91 says:
The message symbols are composed of the bits of the transcoded blocks tx_scrambled (including a mapped group of alignment markers when appropriate) such that bit 0 of the first transcoded block in the message (or am_txmapped<0>) is bit 0 of m_k–1 and bit 256 of the last transcoded block in the message is bit 9 of m_0.

SuggestedRemedy

Define the order the bits in each 10-bit FEC symbol going into the FEC and coming out of it.
Provide an example of the output of the FEC after 10-bit interleaving "tx_out", which is after translation from the ordering/numbering that the FEC uses to what most of the PCS uses.

Response *Response Status* **U**

REJECT.

This comment is a restatement of comment R1-39. The resolution to comment R1-39 is recorded in the following file:
https://www.ieee802.org/3/df/comments/D3p1/8023df_D3p1_comments_final_id.pdf
The response to R1-39 is:

"REJECT.
The example patterns are provided to help the implementer confirm correct interpretation of the encoding funcitonality which is complex.
Figure 119-11 provides sufficient guidance to correctly implement "Mux and 10-bit symbol distribution". Therefore adding the suggested additional patterns is not necessary.
There is no consensus to make the proposed changes."

No new evidence has been provided to support the proposed changes.
Note that comment R2-24 relates to a similar concern.
The distribution and mapping of bits from tx_scrambled_am to the codeword message symbols is defined explicitly in 119.2.4.5.
If this algorithm is misinterpreted the error would be evident by comparing the outcome to the examples provided in Annex 172A.
There is no consensus to make the proposed changes.

Cl **173** *SC* **173.5.2.1** *P* **241** *L* **28** # R2-16

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **R** *bit ordering*

Unsatisfied D3.1 comment 39: show some of the 8-lane output of an 32:8 bit mux.

SuggestedRemedy

In a NOTE, show some of the 8-lane output of a 32:8 bit mux for the beginning of the example in Annex 172A. 8 lanes x 80 hex characters should be more than enough. Cross-reference to 172A. In 172A, cross-reference to here.

Response *Response Status* **U**

REJECT.

This comment is a restatement of comment R1-39. The resolution to comment R1-39 is recorded in the following file:
https://www.ieee802.org/3/df/comments/D3p1/8023df_D3p1_comments_final_id.pdf
The response to R1-39 is:

"REJECT.
The example patterns are provided to help the implementer confirm correct interpretation of the encoding funcitonality which is complex.
Figure 119-11 provides sufficient guidance to correctly implement "Mux and 10-bit symbol distribution". Therefore adding the suggested additional patterns is not necessary.
There is no consensus to make the proposed changes."

No new evidence has been provided to support the proposed changes.

Subclause 173.5.2.1 provides sufficient guidance to correctly implement the intended functionality.

There is no consensus to make the proposed changes.

Cl **169** *SC* **169.1.2** *P* **176** *L* **36** # R2-17

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **R** *figure*

We show the sublayer stack in the first figure of each "Introduction to <MAC rate>" clause and the first figure of each sublayer clause in its overview. Usually we include all relevant sublayers, which this gives the reader a familiar map to give the clause context. See figures 69-1, 80-1, 81-1, 82-1, 83-1, 91-1, for example. Also 105 106 107 108 109 for 25G, 131 132 133 134 135 for 50G.
This consistency should be maintained unless changed through the maintenance process. There are few exceptions: when 116, 117, 118, 119 and 120 for 200 Gb/s and 400 Gb/s were written, the first wave of PHYs had no AN, and 3ck did not add them to these diagrams, although AN is included in Figure 161-1 (RS-FEC-Int).

SuggestedRemedy

Add the missing AN sublayer to Figure 169-1 (introduction to 800 Gb/s), like 80, 105, 131. It may be advisable to revert "800GBASE" to "800GBASE-R" for consistency; any future project with a non-BASE-R 800G PHY may choose its own layer stack.
Add the missing AN sublayer to Figure 170-1 (RS and 800GMII), like 81, 106, 132.
Add the missing AN sublayer to figures 171-1 and 3 (800GMII Extender and 800GXS) for consistency.
Add the missing AN sublayer to Figure 172-1 (PCS), like 82, 107, 133.
Add the missing AN sublayer to Figure 173-1 (PMA), like 83, 109, 134.
Either now or via maintenance, (maybe to be implemented in 3dj), insert the missing AN in figures 1 of 116, 117, 118, 119 and 120.

Response *Response Status* **U**

REJECT.

This comment does not apply to the substantive changes between IEEE P802.3df D3.1 and D3.2 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

Although this Figure was modified in Draft 3.2, the only modication was changing the label "800GBASE-R" to "800BASE" per comment R1-1 in the following:
https://www.ieee802.org/3/df/comments/D3p1/8023df_D3p1_comments_final_id.pdf
The concerns expressed in this comment (R2-17) are not related to this change in label.

The reference to the figure states "relationships among 800 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 169–1." The figure is not intended to provide all of the details within all 800 Gb/s PHYs that might be defined.

There are many sublayers and structures that are not included in addition to the AN including the 800GMII Extender, 800GXS, 800GAUI-n, and additional sublayers might be added in the future. Its not practical or necessary to include all of these additional sublayers.

There is no consensus to make the proposed changes.

Cl **172** *SC* **172.2.4.1** *P* **219** *L* **10** # R2-24

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **R** *bit ordering*

Unsatisfied D3.1 comment 39: need examples to show some of the output from the PCS. Figure 119-11 implies that bit 0 (rather than 9) of a 10-bit symbol in a FEC codeword goes to the PMA first but there is no indication of what that means, and whether it corresponds to a bit 0 or a bit 9 of tx_scrambled_am.

SuggestedRemedy

Define the bit ordering.

Response *Response Status* **U**

REJECT.
This comment does not apply to the substantive changes between IEEE P802.3df D3.1 and D3.2 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
Note that comment R2-13 relates to a similar concern.
The distribution and mapping of bits from tx_scrambled_am to the codeword message symbols is defined explicitly in 119.2.4.5.
If this algorithm is misinterpreted the error would be evident by comparing the outcome to the examples provided in Annex 172A.

Cl **172A** *SC* **172A** *P* **282** *L* **51** # R1-39

Dawe, Piers J G NVIDIA

Comment Type **TR** *Comment Status* **R** *(bucket2)*

Experience with Annex 172A shows us how valuable it is. But more complexity follows: twice "Mux and 10-bit symbol distribution" as in 119.2.4.8 Figure 119-11 (with an order reversal that doesn't seem to be mentioned in the text), then 32:8 bit mux as in 173.5.2.1 where the two flows get interleaved, which is a new thing and worth an example.

SuggestedRemedy

Show some of the 16+16-lane output of the PCS for these cxA and cxB. It may be enough to show e.g. the beginnings of lanes 1 and 31, enough to include some differences between four codewords.
Also show some of the 8-lane output of an 32:8 bit mux from that (which could go in a NOTE in 173). Again, showing a couple of lanes would be enough to resolve most or all misinterpretations or ambiguities. Add a cross-reference from here.
If only a few hundred bits are needed, it could go in text. But if a more complete example is preferred, tables could be added and plain-text equivalents uploaded.

Response *Response Status* **U**

REJECT.

The example patterns are provided to help the implementer confirm correct interpretation of the encoding funcitonality which is complex.

Figure 119-11 provides sufficient guidance to correctly implement "Mux and 10-bit symbol distribution". Therefore adding the suggested additional patterns is not necessary.

There is no consensus to make the proposed changes.