State of IEEE P802.3df

IEEE P802.3df Task Force
May 2022 Session

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Agenda

- Current status
  - Baseline Status Review
  - April 2022 Ad hocs
- Working Towards P802.3df Draft 1.0
- Proposed Next Steps
- Summary

Baseline Status as of May 17th

Ethernet Rate	Assumed Signaling Rate	AUI	BP	Cu Cable	MMF 50m	MMF 100m	SMF 500m	SMF 2km	SMF 10km	SMF 40km
200 Gb/s	200 Gb/s	Over 1 lane 200GAUI-1		Over 1 pair 200GBASE-CR1			Over 1 Pair TBD	Over 1 Pair TBD		
400 Gb/s	100 Gb/s							Over 4 Pair TBD		
	200 Gb/s	Over 2 lanes 400GAUI-2		Over 2 pairs 400GBASE-CR2			Over 2 Pair TBD			
800 Gb/s	100 Gb/s	Over 8 lanes 800GAUI-8	Over 8 lanes 800GBASE-KR8	Over 8 pairs 800GBASE-CR8	Over 8 pairs 800GBASE-VR8	Over 8 pairs 800GBASE-SR8	Over 8 pairs TBD	Over 8 pairs TBD		
	200 Gb/s	Over 4 lanes 800GAUI-4		Over 4 pairs 800GBASE-CR4			Over 4 pairs TBD	1) Over 4 pairs TBD 2) Over 4 λ's TBD		
	TBD								Over single SMF in each direction TBD	Over single SMF in each direction TBD
1.6 Tb/s	100 Gb/s	Over 16 lanes 1.6TAUI-16								
	200 Gb/s	Over 8 lanes 1.6TAUI-8		Over 8 pairs 1.6TBASE-CR8			Over 8 pairs TBD	Over 8 pairs TBD		

Adopted baselines

April 2022 Ad Hoc Meetings Progress and Key Findings

- **Architecture & Logic Ad hoc**
  - **Architecture needs to support up to 2 AUIs per line card (see https://www.ieee802.org/3/df/public/adhoc/logic/22_0411/dambrosia_3df_logic_220411a.pdf)**
  - **Need input on error model (FEC Gain / BER Target) for 200 Gb/s electrical interfaces & PMDs and optical PMDs**
- **Electrical Ad hoc**
  - **Straw Poll - I am interested in C2M AUIs that would support the following form factors: a. PCB host front panel pluggable b. cabled-host front panel pluggable c. co-package d. near-package (chicago rules)**
    - **Results: A: 50, B: 47, C: 38, D: 38**
  - **No objections to Clause 73 (CU PMD) related AN proposal (see https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/lusted_3df_elec_01_220502.pdf)**
  - **New channel data contributed**
- **Optical Ad hoc**
  - **No 200Gbps/lane optical proposals or input to architecture**
  - **FWM (four wave mixing) penalty needs to be considered for narrow-wavelength spaced PMDs that might be proposed**
  - **Support on Optical nomenclature (see https://www.ieee802.org/3/df/public/adhoc/optics/0422_OPTX/lusted_3df_optx_01a_220428.pdf)**

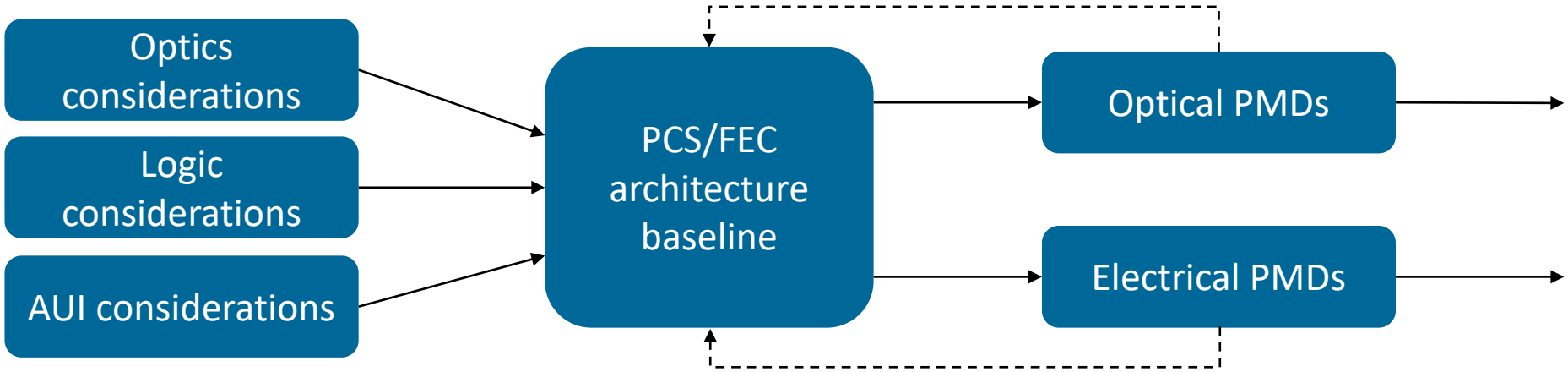
802.3df Baseline Status Summary

Item	Status	Notes
Architecture	Not Adopted	Baseline Proposal May 2022 Interim
Logic (PCS/FEC/PMA) for 100 Gbps/lane 800 GbE PMDs	Not Adopted	Baseline Proposal Update May 2022 Interim
all 100 Gbps/lane based AUIs for 800 GbE	**Adopted**	
all 100 Gbps/lane PMDs except 400GBASE-DR4-2	**Adopted**	
400GBASE-DR4-2	**Anticipated Adoption**	**Baseline Proposal May 2022 Interim**
8 x 100 Gbps/lane Cu MDIs	**Anticipated Adoption**	**Baseline Proposal May 2022 Interim**
8 x 100 Gbps/lane Optical MDIs	Not Adopted	No Baseline Proposal
Auto negotiation	**Anticipated Adoption**	**Baseline Proposal May 2022 Interim**
Logic (PCS/FEC/PMA) for 200 Gbps/lane based and LR / ER PMDs	Not Adopted	
all 200 Gbps/lane AUIs and 1.6 TbE (16x100 Gbps/lane) AUIs	Not Adopted	No Baseline Proposals
all 200 Gbps/lane Cu PMDs	Not Adopted	No Baseline Proposals
All 200 Gbps/lane Optical PMDs (DR, DR-x-2, FR)	Not Adopted	Baseline Proposal May 2022 Interim
800GBASE-LRx/ERx	Not Adopted	• 800G LR4 (PAM4 IMDD) Proposal submitted Mar 2022 Plenary • 800G-LR4 optical PMD based on 53-Gbaud dual-polarization PAM4 – May 2022 Interim

Observations

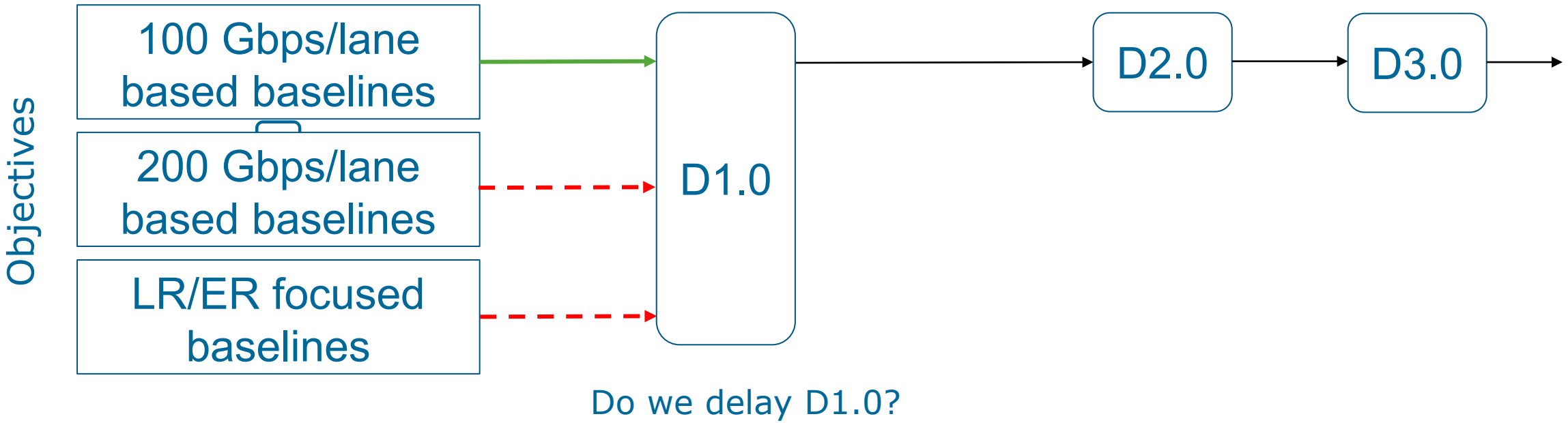
- FEC is key!
  - 100 Gbps/lane leverages work of 802.3bs, 802.3ck, 802.3cu, and 802.3db
  - 200 Gbps/lane AUI / PMD needs unknown
  - If adopted for LR and/or ER, it is assumed a coherent based approach would use a FEC scheme with more coding gain than the 2km and below PMDs
- Coding gain needed for a 200 Gbps/lane are related to the AUI channel(s)
  - 802.3ck C2M channel budget took an estimated 1 year from submission of C2M channel data
  - 200 Gbps/lane channel data submission beginning (C2M channels, 200 Gb/s CR / KR)
  - FEC developed for 100 Gbps/lane **may or may not** support 200 Gbps/lane
- There is risk in selection of FEC for 200 Gbps/lane AUIs / PMDs prior to in-depth analysis

Working Towards a P802.3df Draft 1.0



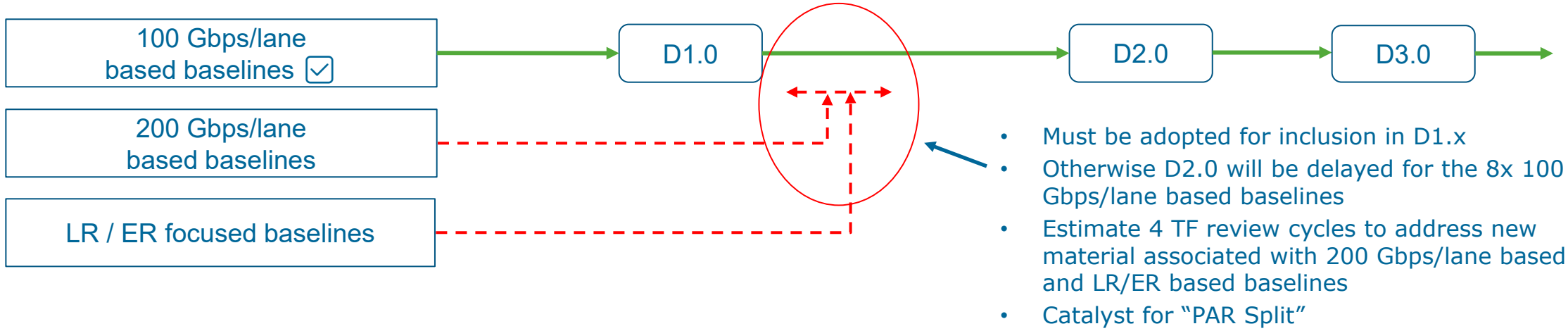
- Strong interest to start defining PMD baseline specifications
- Need to define PCS/FEC architecture first
  - FEC needs for 100 Gbps/lane known
  - Channel / FEC needs for 200 Gbps/lane unknown
- But locking this down depends on inputs around the AUI's and PMDs
  - 100 Gbps/lane – significant progress
  - 200 Gbps/lane – limited progress

Traditional Project Progress



Potential Paths Forward

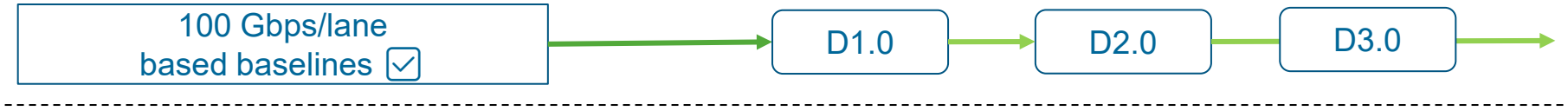
Objectives



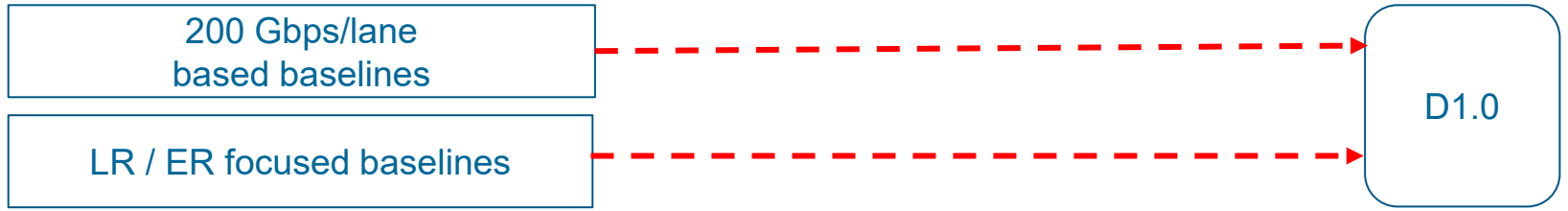
- Must be adopted for inclusion in D1.x
- Otherwise D2.0 will be delayed for the 8x 100 Gbps/lane based baselines
- Estimate 4 TF review cycles to address new material associated with 200 Gbps/lane based and LR/ER based baselines
- Catalyst for "PAR Split"

Objectives

Modified P802.3df (100 Gbps/lane 800 GbE AUIs & PMDs, 400GBASE-DR4-2)



New Project (All 200 Gbps/lane AUIs & PMDs, 800 GbE LR / ER PMDs), and 100 Gbps/lane 1.6 TbE AUIs)



Proposed Next Steps – Generate D1.0 based on 100 Gbps/lane progress

- See slides #3 and #5 for summary of what we have.
- What could D1.0 address at this time?
  - 800 GE introduction
  - 800 GE logic stack from RS to PMA, including FEC defined for 100 Gb/s per lane
  - all 100 Gbps/lane based PMDs for 400 GbE and 800GbE
  - 100 Gbps/lane AUIs for 800GbE
- What is missing at this time for the proposed D1.0?
  - For 800 GbE
    - logic stack, including FEC for 100 Gb/s per lane
      - Decision on FEC form, 2x Clause 119 or sped up Clause 119 ?
    - 100 Gb/s per lane KR/CR training details
    - 100 Gb/s per lane KR/CR auto-negotiation details
    - 100 Gb/s per lane CR MDI details
    - 100 Gb/s per lane Optical PMD MDI details
  - For 400 GbE
    - 400GBASE-DR4-2 PMD

Summary

- Adoption of an architecture that allows the two signaling rate technologies to coexist is a key decision point
- Emerging baseline status indicates that 100 Gbps/lane , 200 Gbps/lane, and LR / ER objectives are on different timelines
- Based on prior experience it seems unlikely that baselines for 200 Gbps/lane and LR / ER objectives will be adopted before a D2.0 based on 100 Gbps/lane objectives could be developed.
- Consider development of the following (note – exact language to be considered during development) –
  - PAR Modification of P802.3df (100 Gbps/lane 800 GbE AUIs & PMDs, 400GBASE-DR4-2)
  - New PAR to address all 200 Gbps/lane AUIs & PMDs, 800 GbE LR / ER PMDs, and 100 Gbps/lane 1.6 TbE AUIs
- Continue work on baseline selection and developing proposed D1.0