800GbE PCS/FEC/PMA Baseline Proposal for PHYs using 8 x 100G PMD lanes - Update

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May 17, 2022
IEEE 802.3df May 2022 session
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Outline

• Introduction
• PCS/FEC/PMA Baseline proposal
• Implementation considerations
• Architecture considerations
• Conclusion
Goals

• Fast time to an 800GbE PCS/FEC/PMA specification for PMDs using 100G/lane
  • Re-use 400GbE PCS/FEC (CL119) as much as possible
  • Support 800GbE with simple modification to the 400GbE PCS/FEC
  • Leverage 802.3bs Cl120 PMA; leverage 802.3ck 100G/lane PMA and AUI specifications

• Maximize the re-use of existing logic sub-blocks used in 400GbE PCS/FEC
  • Leverage industry investment in 400GbE technology

• Enable systems using current 8-lane 800G connectors (OSFP / QSFP-DD) to also support 800GbE
  • E.g. 8-lane C2M AUIs used as: 8 x 100GAUI-1 / 4 x 200GAUI-2 / 2 x 400GAUI-4 and 1 x 800GAUI-8
Scope

802.3df Adopted PHY Objectives*

<table>
<thead>
<tr>
<th>Ethernet Rate</th>
<th>Assumed Signaling Rate</th>
<th>AUI</th>
<th>BP</th>
<th>Cu Cable</th>
<th>MMF 50m</th>
<th>MMF 100m</th>
<th>SMF 500m</th>
<th>SMF 2km</th>
<th>SMF 10km</th>
<th>SMF 40km</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 Gb/s</td>
<td>200 Gb/s</td>
<td>Over 1 lane</td>
<td>Over 1 pair</td>
<td>Over 1 Pair</td>
<td>Over 1 Pair</td>
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<tr>
<td>400 Gb/s</td>
<td>200 Gb/s</td>
<td>Over 2 lanes</td>
<td>Over 2 pairs</td>
<td>Over 2 Pair</td>
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<tr>
<td>800 Gb/s</td>
<td>100 Gb/s</td>
<td>Over 6 lanes</td>
<td>Over 6 pairs</td>
<td>Over 6 pairs</td>
<td>Over 8 pairs</td>
<td>Over 8 pairs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200 Gb/s</td>
<td>400 Gb/s</td>
<td>Over 4 lanes</td>
<td>Over 4 pairs</td>
<td>Over 4 pairs</td>
<td>1) Over 4 pairs</td>
<td>2) Over 4 pairs</td>
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<td></td>
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<tr>
<td>TBO</td>
<td>200 Gb/s</td>
<td>Over 8 lanes</td>
<td>Over 8 pairs</td>
<td>Over 8 pairs</td>
<td>Over 8 pairs</td>
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<td></td>
<td></td>
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<tr>
<td>1.6 Tb/s</td>
<td>100 Gb/s</td>
<td>Over 16 lanes</td>
<td>Over 16 pairs</td>
<td>Over 16 pairs</td>
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<td></td>
</tr>
<tr>
<td>200 Gb/s</td>
<td>Over 8 lanes</td>
<td>Over 8 pairs</td>
<td>Over 8 pairs</td>
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</tbody>
</table>

Technology Reuse

- Leverage existing or work-in-progress 100 Gb/s per lane (e.g. 3cu, 3ck, 3db) to higher lane counts
- Develop 200 Gb/s per lane electrical signaling for 1/2/4/8 lane variants of AUIs and electrical PMDs
- Develop 200 Gb/s per optical fiber for 1/2/4/8 fiber based optical PMDs and 4 lambda WDM optical PMD
- Potential for either direct detect and / or coherent signaling technology

Making it all work together

Scope of this Baseline: 800GbE PCS/FEC/PMA for all PHY objectives that use 8 x 100G PMDs and AUIs

* Table from https://www.ieee802.org/3/B400G/public/21_1028/B400G_overview_c_211028.pdf
AUI and PMD assumptions

• 802.3df Task Force has adopted 800GbE 8-lane AUI baseline proposals leveraging existing 100G/lane AUI specs, drafts
  • https://www.ieee802.org/3/df/public/22_03/lusted_3df_01a_220315.pdf

• 802.3df Task Force has adopted 800GbE 8-lane PMD baseline proposals leveraging existing 100G/lane PMD specs, drafts
  • https://www.ieee802.org/3/df/public/22_03/lusted_3df_01a_220315.pdf
  • https://www.ieee802.org/3/df/public/22_02/welch_3df_01a_220222.pdf
  • https://www.ieee802.org/3/df/public/22_03/murty_3df_01a_220315.pdf

• 802.3bs CL119 PCS works for all 100G/lane AUIs and PMDs for 400GbE

• Similarly, this PCS/FEC Baseline (leveraging CL119) works for all adopted 800GbE 8-lane AUIs and PMDs
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Architecture

*Update: PCS and FEC functions proposed to be located in the PCS sub-layer (same as CL119). See Logic Baseline, M. Gustlin, May’22 interim

Note: Not showing layering diagram for Cu PMD (will be same as other Cu PMD layering diagrams in 802.3)
End-End PCS/FEC scheme for 800GbE (8 x 100G) PMDs

Note: This End-End PCS/FEC works with optional Chip to Chip AUIs and a combination of Chip to chip and Chip to module (same as 400GAIU-4 in 802.3ck)

* PCS sub-layer is proposed to contain the FEC
Tx PCS/FEC Data Flow

- Based on two 802.3bs, CL119 sub-layers in parallel
  - Two 400G FEC flows (flow-0 and flow-1)
- 66b round robin distribution into two 400G flows after 64B/66B encode
- Sub-blocks shown within each flow are identical to CL119, except:
  - AM values are made unique across the two flows
  - AM insertion is aligned across the two flows
- 32 PCS lanes per 800GbE PCS
  - 16 PCS lanes per 400G flow
- Any 4 PCS lanes to any PMA output lane
  - 4:1 bitmuxing
Tx 66b Block Distribution

• Round Robin among two ‘400G Flows’
Alignment Marker Insertion

- **802.3bs 400G AM structure**
  - AM size = 8 x 257b
  - Spacing = 160k x 257b = 8192 CWs
- **AM total sizing for 800G = 2x400G**
  - AM size = 16 x 257b
  - Spacing = 320k x 257b = 16384 CWs
- **Markers inserted at consecutive 257b blocks across both 400G flows**
  - Flow-0 is first in time carrying the even encoded 4x66b blocks
  - Flow-1 carries odd encoded 4x66b blocks
AM Marker Encoding

- CM0-CM5 and UP0-UP2 are unchanged from 400GbE CL119
- UM0/UM3 for PCS lanes 0-15 are inverted from 400GbE
- UM1/UM2/UM4/UM5 for PCS lanes 16-31 are inverted from 400GbE
- Prevents lock with 400GbE ports
- Maintains DC balance

Note: in table above, bolded text indicates changes from CL 119 AM values
Rx PCS/FEC Data Flow

• Alignment Lock and Deskew
  • AM lock: per lane, same as CL119
  • De-skew: across 32 PCS lanes

• Lane reorder (and split)
  • Reorder and split 32 PCS lanes into 2 groups of 16
    • Lanes 0-15: Flow-0
    • Lanes 16-31: Flow-1

• FEC decode, de-scramble, transcode decode – same as CL119

• Round robin block collection must be aligned across Flow-0/1 based on Alignment Marker location
Rx 66b Block Collection

• Round Robin 66b Block Collection is opposite of Tx Block Distribution
Re-use CL119 State Diagrams

• Re-use all of the following
  • Figure 119–12—Alignment marker lock state diagram
  • Figure 119–13—PCS synchronization state diagram
  • Figure 119–14—Transmit state diagram
  • Figure 119–15—Receive state diagram

• Minor modification to the following
  • Add restart_lock<y> variable per 400G flow
    • restart_lock = restart_lock<0> OR restart_lock<1>
  • Add hi_ser<y> variable per 400G flow
    • hi_ser = hi_ser<0> OR hi_ser<1>
PMA

- PMA functions as defined in CL120, with latest 802.3ck updates for 100G/lane
  - Bit-multiplexing (4:1)
  - Modulation (PAM4)
  - AUI Physical lane instantiation (8 lane)
  - Signaling lane rate (106.25Gb/s)
  - Coding (Gray, precoding)
  - Clock and data recovery
  - Loopbacks
  - Test patterns

- Per lane AUI specifications from 802.3ck
PMA Muxing

- Any 32 PCS Lanes to Any 8 PMA Lanes
  - 4:1 Bit-multiplexing of data from any 4 PCS lanes to any 1 PMA lane
  - The receiver can receive PMA lanes in any order and has a full 32 lane reorder block
  - Expect Clock content to be similar to a 400GE Cl119 stream
    - Further work ongoing on this
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Latency considerations

• Two 400GbE FEC encode/decode engines in parallel
• FEC latency for this baseline proposal same as 400GbE FEC latency
**PCS lanes for 8 x 100G**

- Many 800G implementations will support 100/200/400/800GbE Ethernet ports
  - 32 PCS lanes already exist to support 2 x 400GbE / 4 x 200GbE / 8 x 100GbE!
  - Reuse of per lane PCS alignment logic

<table>
<thead>
<tr>
<th>800Gb/s Block config</th>
<th>PCS/FEC lanes per Ethernet port</th>
<th>Total PCS/FEC lanes per 800Gb/s block</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 x 800GbE port</td>
<td>32 lanes @ 25G</td>
<td>32</td>
</tr>
<tr>
<td>2 x 400GbE ports</td>
<td>16 lanes @ 25G</td>
<td>32</td>
</tr>
<tr>
<td>4 x 200GbE ports</td>
<td>8 lanes @ 25G</td>
<td>32</td>
</tr>
<tr>
<td>8 x 100GbE ports</td>
<td>4 lanes @ 25G</td>
<td>32</td>
</tr>
</tbody>
</table>

- Choice of 32 PCS lanes can enable implementations over 16 x 50G AUI lanes
  - If needed (e.g. test equipment)
Other Implementation Considerations

• This baseline benefits from the use of two 400GbE PCSs in parallel
  • Reuse of logic blocks from 400GbE PCS possible
  • FEC engines, transcoder, scramblers running at same bandwidth as 400GbE
  • Per lane alignment lock running at same speed as 400GbE
  • Minimizes new development and verification

• This baseline follows the approach taken by the adopted 800GbE 8-lane AUIds and PMD baselines
  • 800GbE 8-lane AUIds and PMDs are doubling number of lanes from 400GbE
    • Example 1: 800GAUI-8 is 2 x 400GAUI-4 in parallel
    • Example 2: 800GBASE-DR8 is 2 x 400GBASE-DR4 in parallel
  • Allows re-use of specifications, maximize use of technology and investment from 400GbE
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IEEE P802.3df Architecture : FEC schemes

End-to-End FEC scheme
(FEC1 used for AUIs and PMD)

Concatenated FEC scheme
(FEC2 is added on top of FEC1.
FEC1 for AUIs, FEC1+FEC2 for PMD)

Segmented FEC scheme
(FEC2 replaces FEC1. FEC1 used for local AUI only. FEC2 for PMD only)
800GbE Architecture: FEC schemes over AUI-8

**End-to-End FEC scheme**
- Targeted by this Baseline

**800GAUI-8**
- 800GBASE-CR8/KR8, 800GBASE-VR8/SR8, 800GBASE-DR8/DR8+

**Concatenated FEC scheme**
- Other FEC schemes / evolution remains open

**Segmented FEC scheme**
- Included in this baseline

End-to-End to End FEC scheme
- MAC/RS
- PCS
- PMA (32:8)
- PMA (8:8)
- PMD
- MDI

800GAUI-8

Other PMDs (TBD)

Concatenated FEC scheme
- MAC/RS
- PCS
- PMA (32:8)
- PMA (8:32)
- FEC
- FEC2
- PMD
- MDI

Medium

Other PMDs (TBD)

Segmented FEC scheme
- MAC/RS
- XS
- PMA (32:8)
- PMA (8:32)
- XS
- PCS
- FEC1
- FEC2
- PMD
- MDI

Medium

Other PMDs (TBD)
800GbE Architecture: FEC schemes over AUI-4

End-to-End FEC scheme

- MAC/RS
- PCS
- PMA
- PMA
- PMD

Medium → MDI

AUI-4

Other PMDs (TBD)

Concatenated FEC scheme

- MAC/RS
- PCS
- PMA
- PMA
- FEC
- PMD

Medium → MDI

AUI-4

Other PMDs (TBD)

Segmented FEC scheme

- MAC/RS
- XS
- PMA
- PMA
- PCS

Medium → MDI

AUI-4

Other PMDs (TBD)

*FEC1 could be the FEC proposed in this Baseline or could be a different FEC – pending analysis*
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Conclusions

• This Baseline: 800GbE PCS, FEC and PMA for 8 x 100G PMDs and 8 x 100G AUls
• Supports all adopted 802.3df copper and optical PMDs baselines using 100G/lane
• Highly leverages existing 400GbE specifications
  • 2 x 400GbE (Clause 119) with minor modifications to the specifications
• Highly leverages existing 400GbE implementations
  • Enable re-use of per-lane AM lock, FEC interleaving, FEC encode/decode, scrambler, transcoder
• Enables faster time-market for 800GbE (8 x 100G/lane) implementations
  • Maximizing technology reuse and existing industry investments
• Fits into an overall 800GbE Logic Architecture, and does not constrain future FEC schemes using 200G/lane AUls and PMDs and/or Coherent PMDs
• 1.6TbE PCS/FEC can be chosen independently of 800GbE
  • Decisions made in this baseline will not restrict options / choices for 1.6TbE
Thanks !
Straw Poll

• I would support adopting the 800GbE PCS/FEC/PMA baseline for PHYs using 8x100G PMD lanes as described in this presentation
  • Yes :
  • No :
  • Need more information :