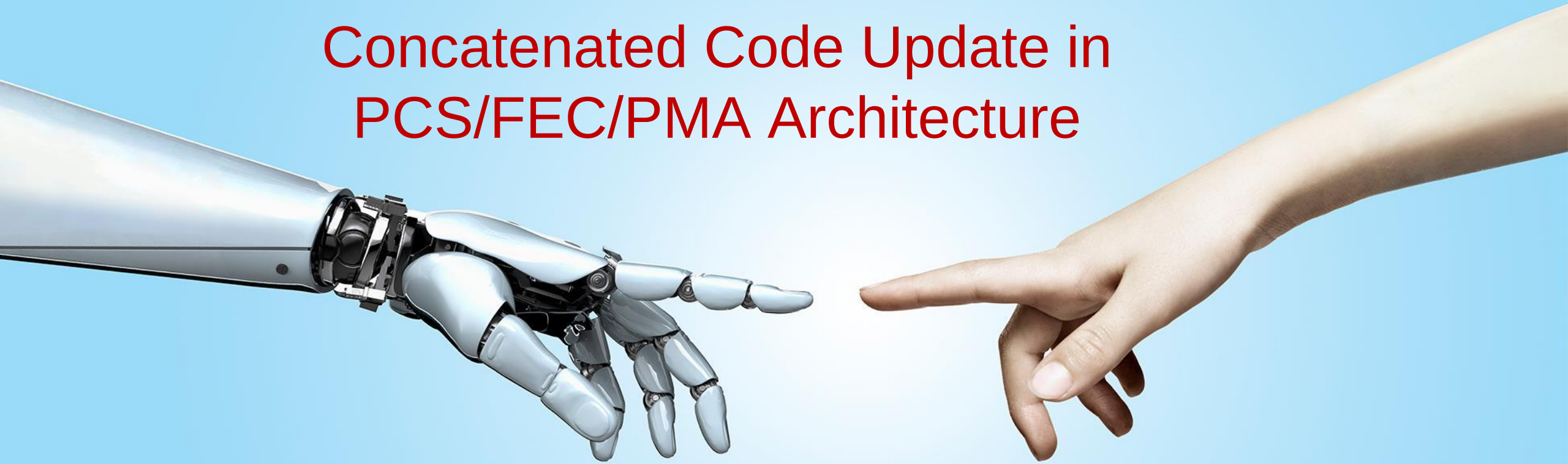
Concatenated Code Update in PCS/FEC/PMA Architecture



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Background: Holistic FEC Architecture to Enable FEC Schemes

- During wang_3df_logic_220411 presentation, encapsulated scheme got more discussions and interests as a solution with moderate CG, low latency and power, breakout support and simplified optical modules to lower cost.

	FEC Codes	Overhead Ratios of AUIs	Overhead Ratios of AUIs and PHY PMD	High NCG Capability	Latency/ Power	Simiplifed Optical Module	Breakout
End-to-End	1	Identical	Identical	Restricted	Potential Lower	Yes	Yes
Encapsulated (Concatenated)	1 with 2 sub code	Identical or Different	Identical or Different	Potential Higher	Potential Lower	Yes	Yes
Segmented	at least 2	Identical or Different	Identical or Different	Potential Higher	Potential Higher	No	Challenge

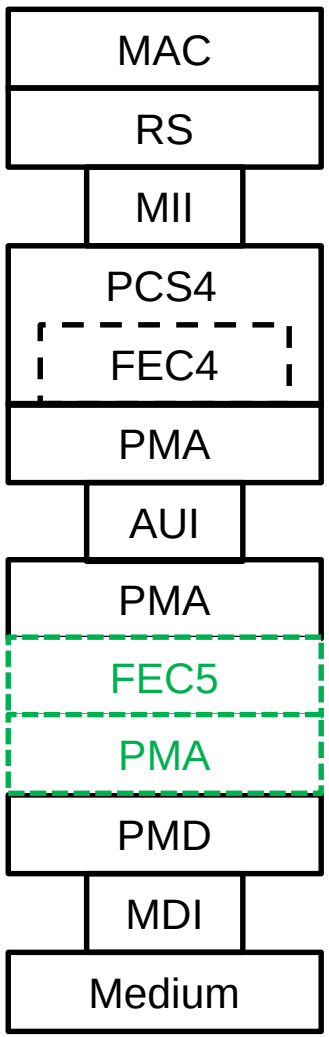
- Motivation: Investigate feasibility and capability of concatenated code to be integrated in PCS/FEC/PMA architecture to enable AUIs and PMDs.

Take Full Advantage of Concatenated Code Capability in 800G/1.6TbE

- Outer code example: 2-way interleaved RS(544,514) for backward compatibility.
  - NCG=6.4dB with ~2.4E-4 optical and 1E-5 AUI pre-FEC BER capability of End-to-End scheme.
- Inner code example: BCH(144,136), eBCH(76,68), forward looking of 200 Gb/s per lane.
  - Lower PMD pre-FEC BER with ~100X reduction from ~2.4E-3 or ~4.8E-3 to ~3.5E-5 or 5.6E-5.
  - Overhead ratio 18/17 or 19/17 for simple PLL design from data rate of outer code.
  - Hard-Decision or Soft-Decision, implementation dependent.
  - Bit transparent in optical module acting as a black box for outer coded data.
- Overall NCG of concatenated code is 8.11/8.69dB for Soft-Decision (he_3df_01a_220308)
- Tradeoff on viable pre-FEC BER for AUIs (equivalent to X0.1 FEC symbol error ratio from Annex 120) and optical PMDs.
  - Start from ~1E-5 for AUI and ~2.4E-3 for optical PMD based on further available information.

https://www.chipestimate.com/An-Insight-into-the-World-of-224Gbps-Electrical-Interface/Synopsys/Technical-Article/2022/02/15

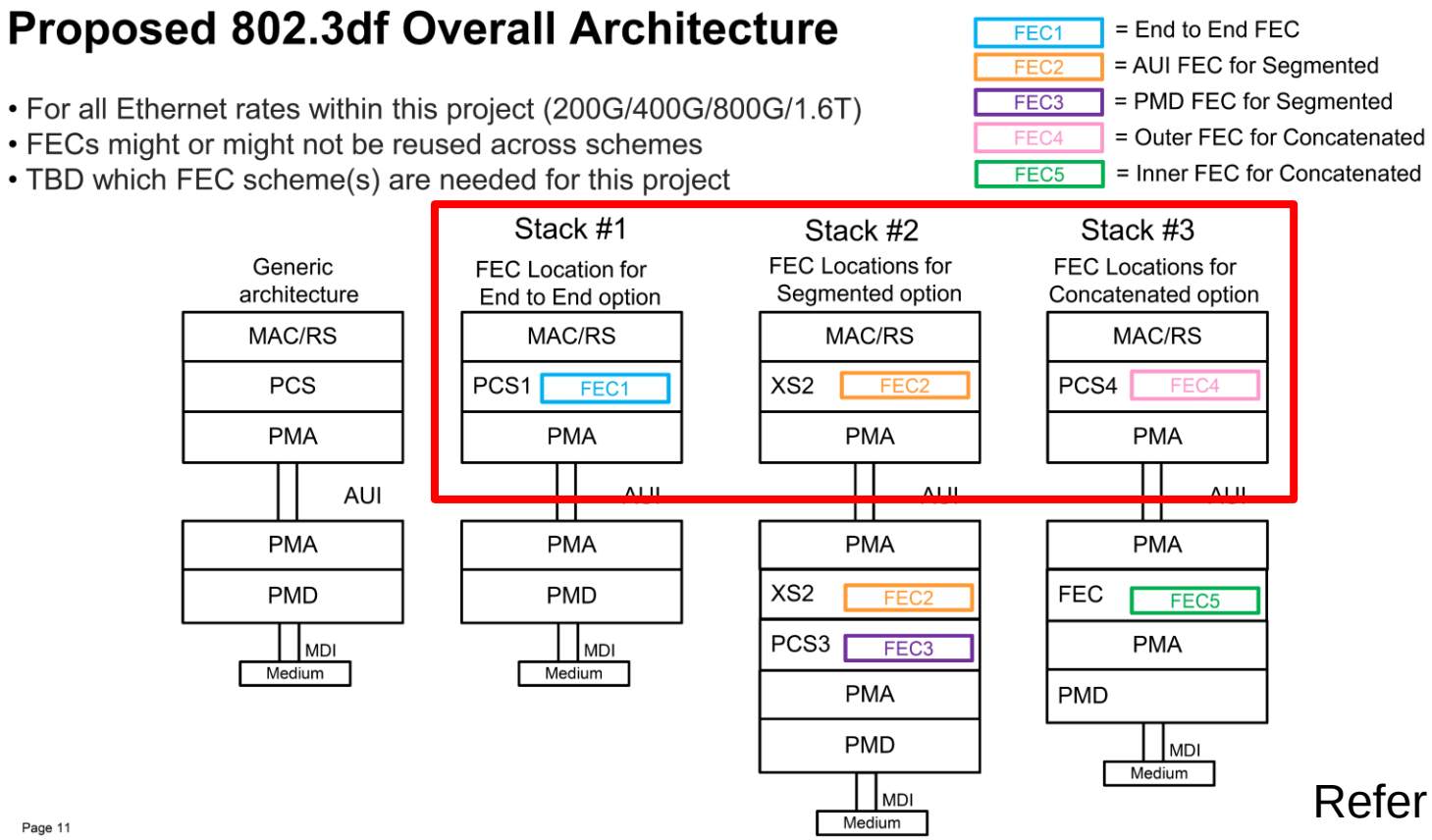
Discussions at Ad Hoc for Concatenated Code in Logic Layer



- **MII:** Role of extended sublayer from IEEE 802.3bs in proposed IEEE P802.3df MAC/PHY logic architecture.
- **PCS:** Encode and decode, rate matching, etc.
- **Overall FEC capability:** Utilizing the concatenated two sub-codes, outer code FEC4 and inner code FEC5.
- **PMA:** Bit multiplexing, boundary alignment of outer code and inner code, which is key factor to enable bit transparency, breakout and simple optical module (oDSP) implementation to lower cost.
- **FEC5:** UCR and UMR of inner code.
- **FEC5:** Error marking for inner code is necessary? Why?

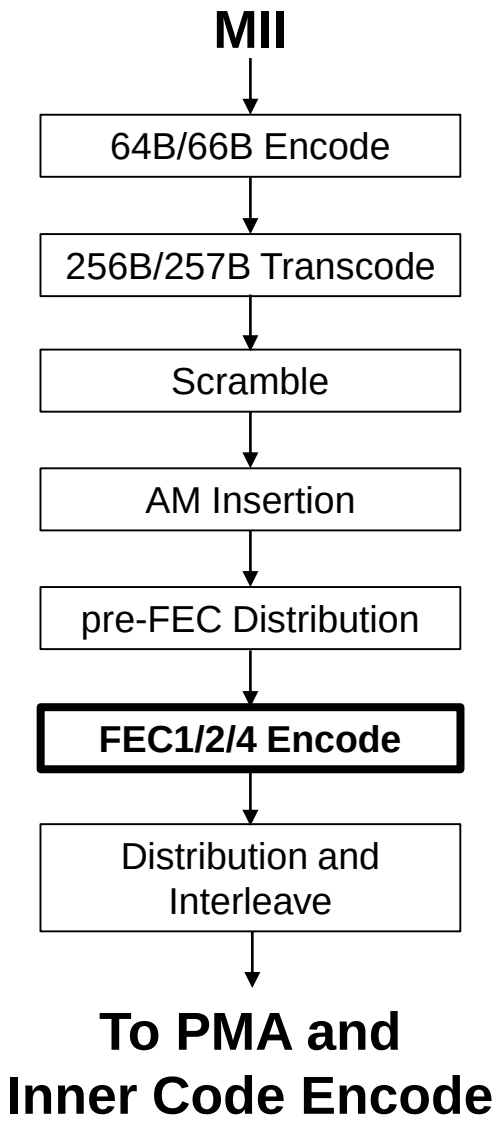
MII: Extend Sublayer

- The MII extender sublayer is needed for PCS including FEC architecture, such as FEC2.
- For encapsulated scheme, the MII extender is not necessary for FEC5 (inner code) sublayer as it can be **wrap** over PMA data stream from AUI.



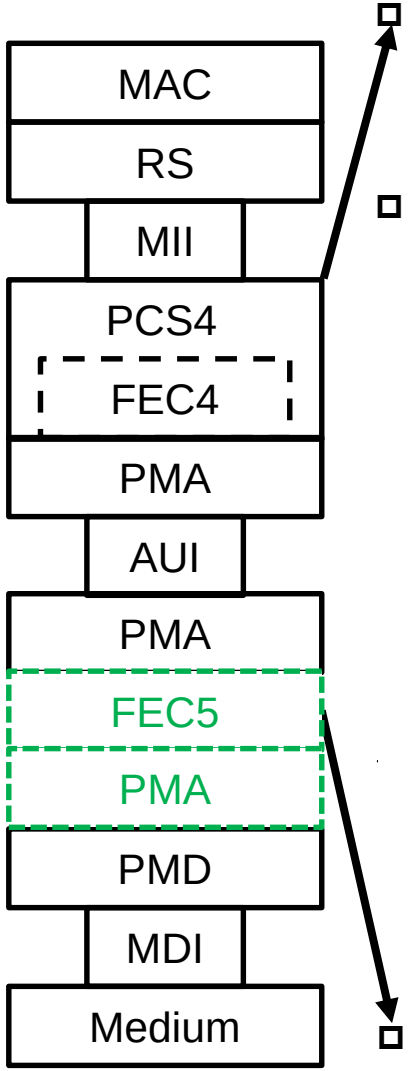
Refer to: [Logic Architecture Baseline]

PCS: 64B/66B and 256B/257B Encode and Decode



- Identical PCS with potential **RS(544,514) as FEC1/2/4** for all FEC schemes.
  - No additional PCS of inner code for encapsulated scheme.
- 64B/66B related functions in Clause 82/119 PCS can be fully reused.
  - Same RS(544,514) based error marking mechanism for all FEC schemes.
  - One-step error marking at outer code only for concatenated code.
- Transcoding or direct encoding to 256B/257B can be supported.
  - RS(544,514) work at 256B/257B data flow.
- Inner code works bit-transparently and does not affect upper sublayers shown here.

PCS: Rate Matching Mechanism



- One-step rate matching with **RS(544,514) as FEC1/2/4** for all of FEC schemes.
  - No idle insertion/deletion allowed below PCS sublayer.
- Challenges of additional rate matching from slavick_3by_01a_0515 in 802.3by.

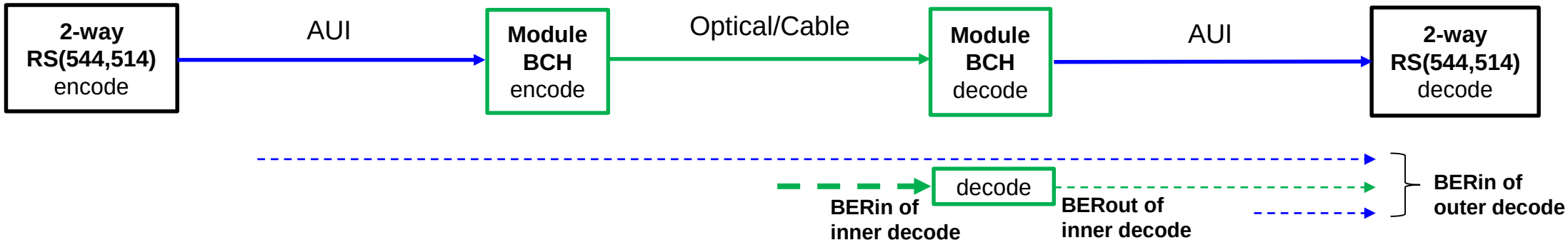
	With CWM	No CWM
OTN	Must de-transcode & rate compensate when using RS-FEC on entry/exit of OTN network, which includes descrambling of data stream.	Must de-transcode only when using RS-FEC. similar to 802.3bj
IEEE 1588	Packet delay variation, due to rate compensation being done below PCS, makes it difficult to optimally support this standard	Supportable
Flex-Ethernet	Breaks frame construction; RS-FEC operation only to minimize exceptions defined	Supportable for all 3 25G operating modes
EEE	constant pattern search (Rapid CWM); down count for tracking Rapid -> normal CWM interval; data always scramble	Constant pattern search; data always scrambled
32GFC	Same RS-FEC engine	Entire data path
Lock Time (<5ms requirement)	Mean: 300us WC: 800us	Mean: 500us WC: 3ms
Area of CR PHY	~500k gates	~480k gates

- With uncertainties of new PMDs and FECs, a 2nd rate matching point can be enabled if required in a similar mechanism as in P802.3cx.

PCS: Rate Matching Mechanism(Cont'd)

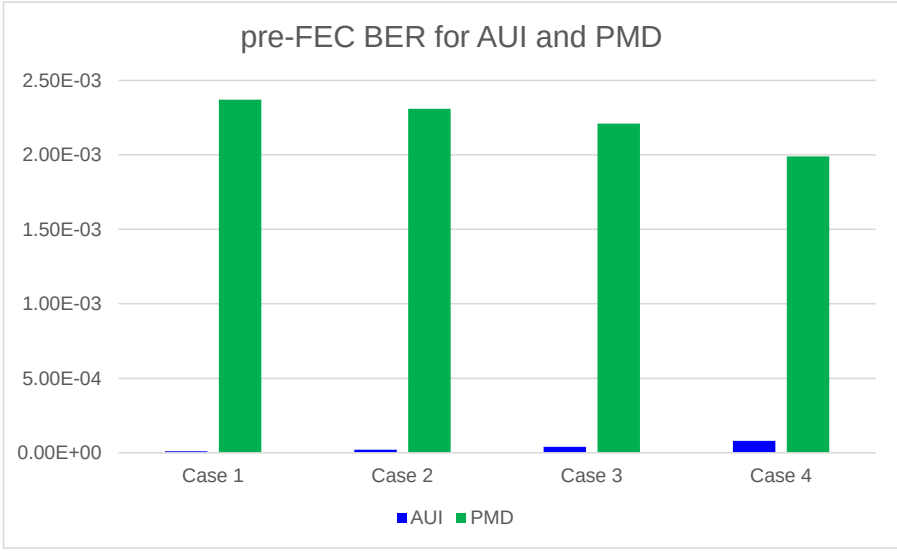
- As rate matching in PCS sublayer reserves room for Alignment Markers for FEC1/2/4 only, which is most likely identical as IEEE 802.3bs definition, the frame synchronization for FEC5, the inner code, can be achieved with the following options:
  - **Option A:** Fully re-use outer code AM patterns, mapping, insertion and removal mechanism. It will require the inner codeword length to be proportional to the outer codeword length. Bit-transparent optical module and breakout will not be supported.
  - **Option B:** Additional new AM for inner code, lead to additional overhead for PLL ratio from 18/17 or 19/17.
  - **Option C:** Blind FEC frame synchronization, similar as Clause 74.7.4.7: FEC block synchronization. **No issue comparing to the above two options. Preferred.**

Overall FEC Capability and pre-FEC BER Requirement Tradeoff



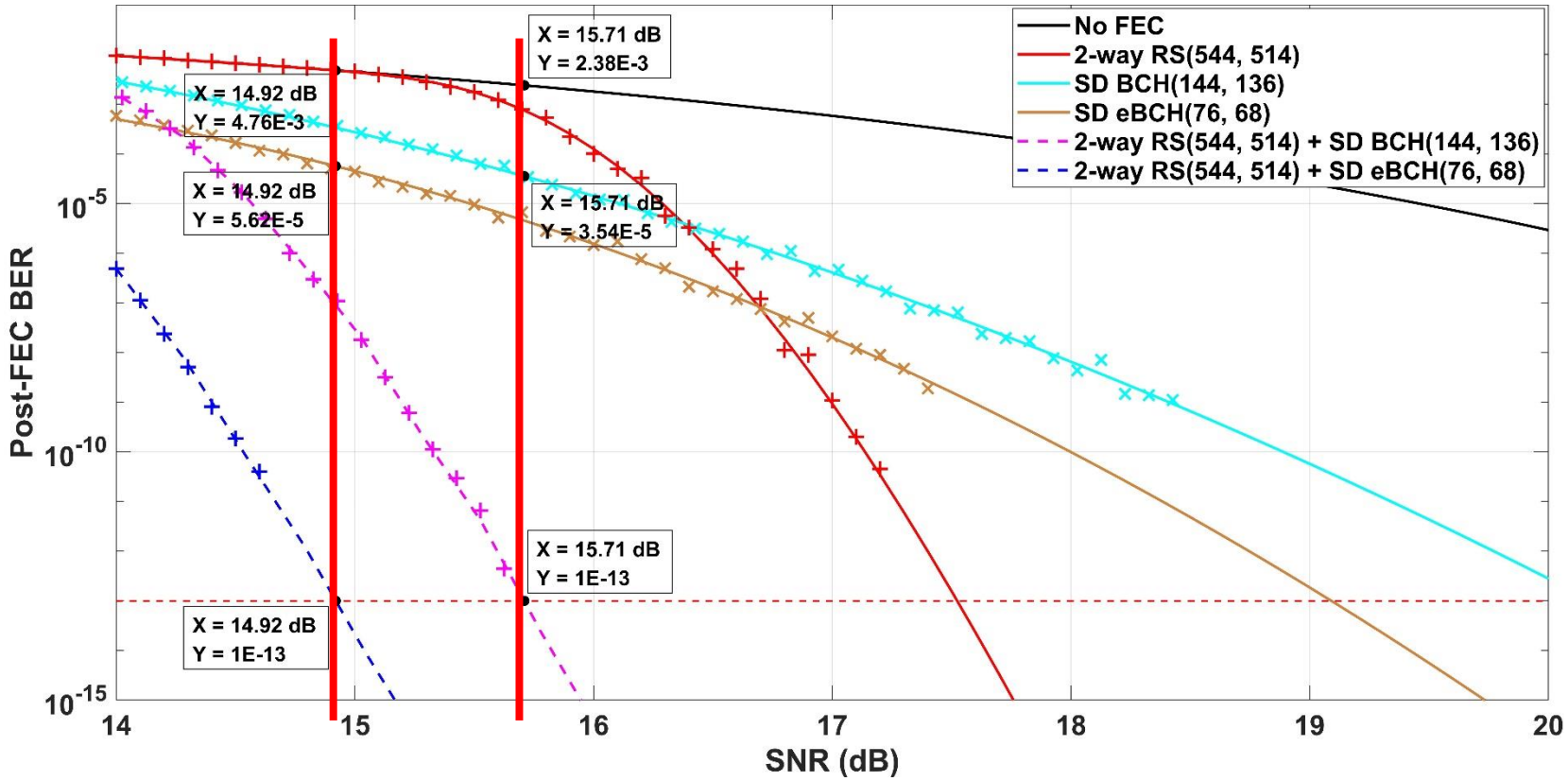
- Examples of viable pre-FEC BER for AUI and optical PMD to meet 1E-13 objective with Soft-Decision BCH(144,136) as inner code. eBCH(76,68) can further relax these pre-FEC BERs.

Concatenated Code Example Outer code: 2-way interleaved RS(544,514) Inner code: SD BCH(144,136)				
	pre-FEC BER for AUI @ $bb_{max}(1)=0.4$			
	1E-5	2E-5	4E-5	8E-5
pre-FEC BER for PMD	2.37E-3	2.31E-3	2.21E-3	1.99E-3



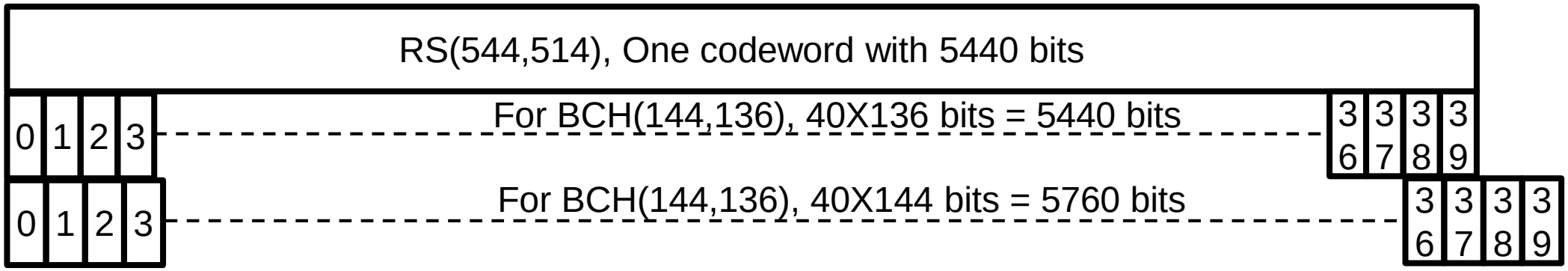
Overall FEC Capability to Tradeoff pre-FEC BER Requirement

- The left-over errors of inner code output, for example SD BCH(144,136), is around ~3.54E-5 with non-Poisson distribution when input BER is at ~2.38E-3.
- Overall NCG of 8.11 dB can be achieved with outer RS(544,514) code as the main contributor of error correction for errors from both AUIs and PMD to meet 1E-13 objective and MTTFPA.

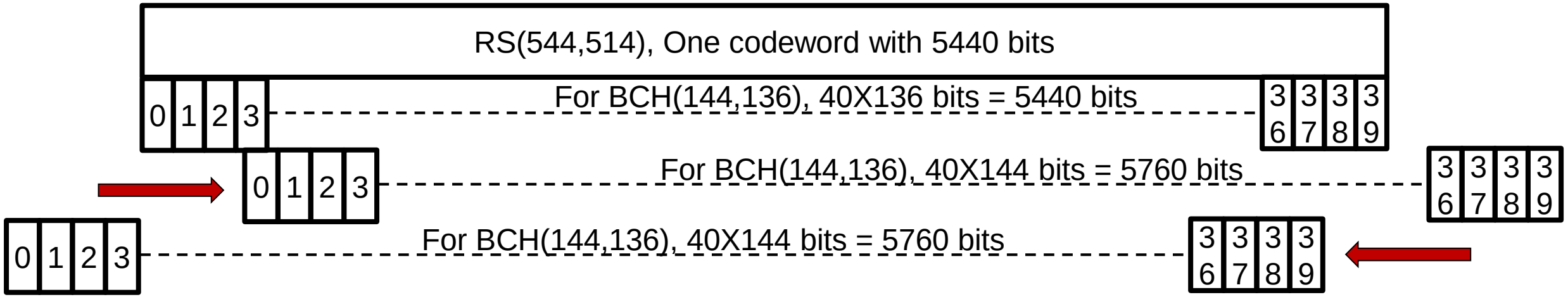


PMA Bit Multiplexing: Floating Outer Code and Inner Code

- Boundary aligned outer code RS(544,514) and inner code BCH(144,136)

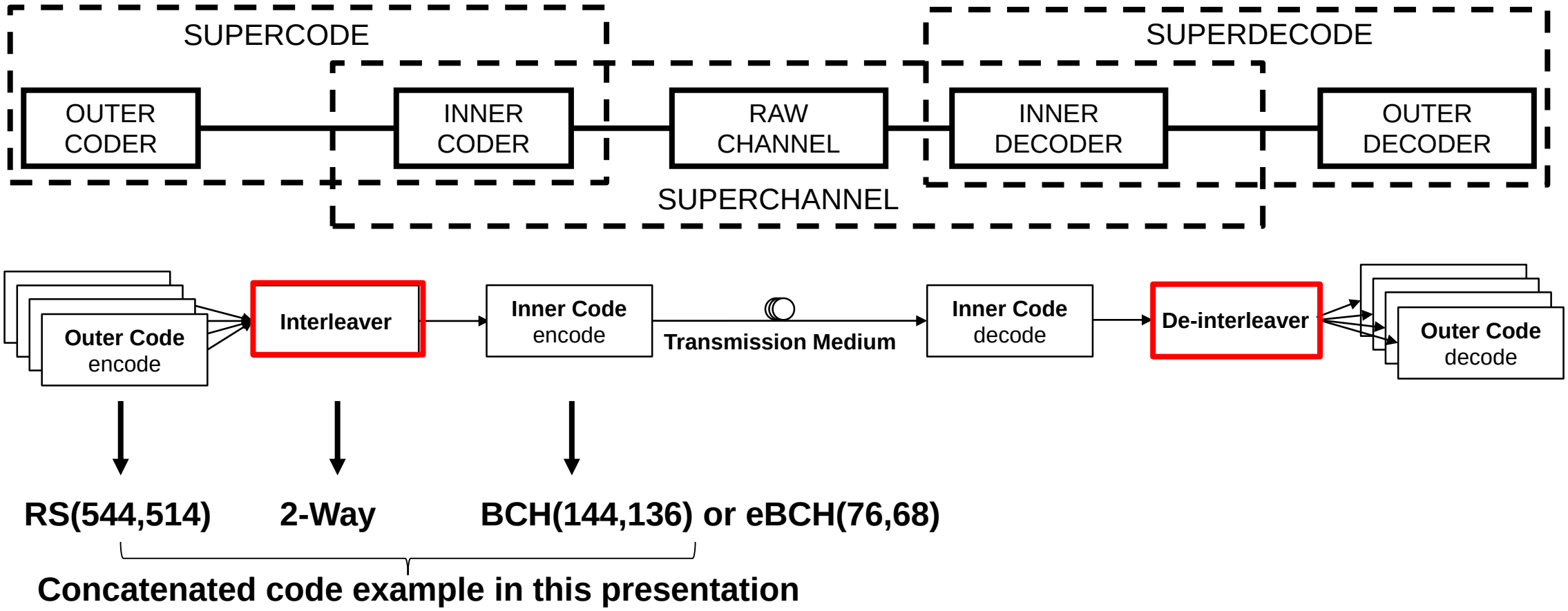


- Arbitrary floated outer code RS(544,514) and inner code BCH(144,136)



PMA Bit Multiplexing: Floating Outer Code and Inner Code(Cont'd)

- The interleaver between outer and inner code already eliminates the aligned boundary comparing to original academia research by G.D Forney in "Concatenated Codes" in 1965.



FEC5: UCR and UMR of Inner Code

- From FEC capability and MTTFPA of Ethernet standard perspective, the output codewords of any FEC code can be categorized as follows:
  - **Correctable codeword:** “good data”.
  - **Uncorrectable codeword:** “bad data”, but the decoder may know it is bad, which can be error marked and discarded refer to Clause 119.2.5.3 and 81.3.3.1; Otherwise,
  - **UnMarked uncorrectable codeword:** “bad data”, and the decoder does not know. Aka: False-decoding or Mis-correction. Relying on CRC32 check to discard or not at MAC.
- Slide 10 of wang_b400g_01a_210315 calculate post-FEC BER and MTTFPA for RS code.

$$\mathrm{BER_{out}} = \sum_{i=t+1}^{n} \frac{i}{n} UCR_i \approx \frac{t+1}{n*m} * UCR$$

$$\mathrm{UMR} \approx (2^m - 1)^{-(d-t-1)} \binom{n-d+t}{t}$$

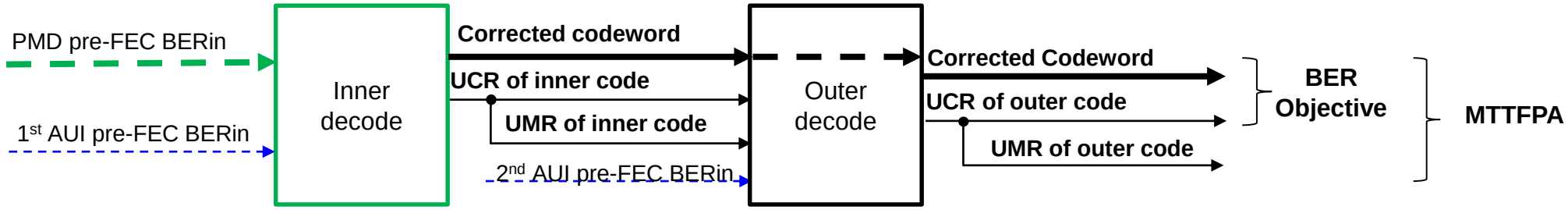
$$\mathrm{MTTFPA} > \frac{N * T_{bit}}{UCR * UMR * (1 + \frac{N}{k})} * 2^{32}$$

$\mathrm{BER_{out}}$:	Post-FEC BER.
UCR:	Uncorrectable Codeword Ratio (Related to Pre-FEC BER).
UMR:	Unmarked Uncorrectable Codeword Ratio.
T_{bit}:	Bit time.
t:	FEC error correction capability.
d:	Number of erroneous symbols in a codeword.
n:	FEC codeword size in symbols.
m:	Galois Field index.
k:	Number of message bits in a FEC codeword.
N:	Ethernet MAC frame size in bits.

Note:
1. The calculation is based on RS FEC.
2. For UMR calculation method please refer to cideciyan_01_0112.pdf.

FEC5: UCR and UMR of Inner code (Cont'd)

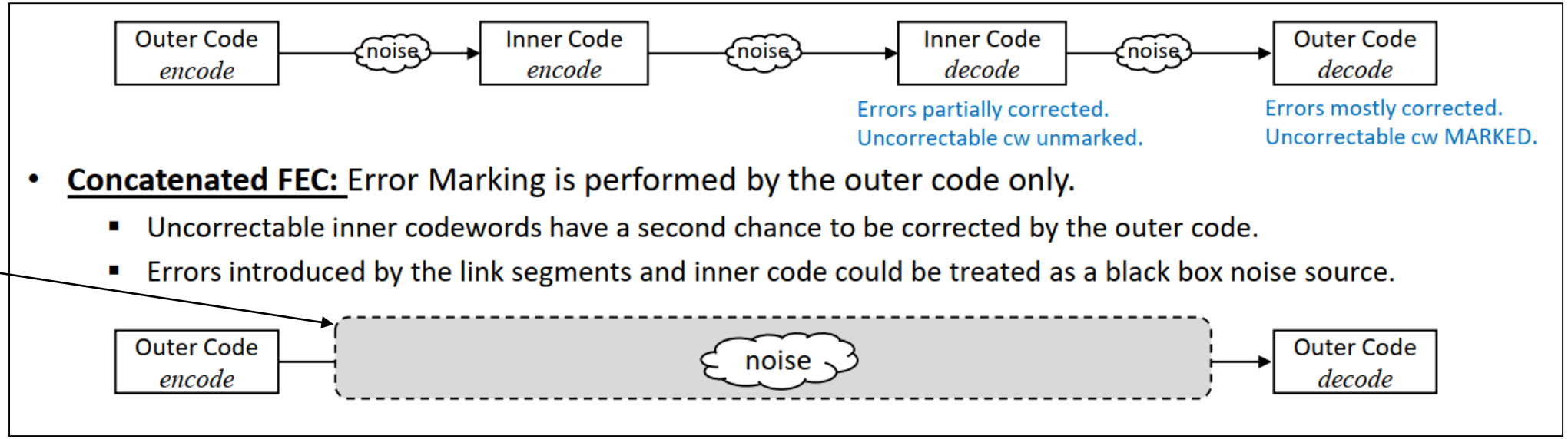
- UCR and UMR portion of each sub-code of concatenated code:
  - For the inner code output, uncorrectable codewords, including UnMarked uncorrectable codewords have a second opportunity to be corrected by outer code.
  - For the outer code output, both BER objective and MTTFPA can be met as inner code lower the pre-FEC BER of the outer code by 10-100X, e.g. from ~2.4E-4 to ~3.5E-5.



	Correctable Codeword Portion	UnCorrectable Codeword Portion (UCR)	UnMarked uncorrectable Codeword Portion(UMR) in UCR	UCR * UMR for MTTFPA
HD BCH(144, 136) @ 6.6E-4 pre-FEC BER	99.578600000000000%	0.421400000000000%	56.640000000000000000%	0.23868096000000000000000000000%
SD BCH(144, 136) @ 2.4E-3 pre-FEC BER	99.850900000000000%	0.149100000000000%	100.000000000000000000%	0.14910000000000000000000000000%
HD eBCH(76,68) @ 1.4E-3 pre-FEC BER	99.478600000000000%	0.521400000000000%	1.870000000000000000%	0.00975018000000000000000000000%
SD eBCH(76,68) @ 5.0E-3 pre-FEC BER	99.890600000000000%	0.109400000000000%	100.000000000000000000%	0.10940000000000000000000000000%
RS(544,514) @ 2.4E-4 pre-FEC BER	99.999999999918500%	0.000000000081515%	0.000000000000003070%	0.00000000000000000000000000250%
* Use the most pessimistic assumption of UMR@100%. Actual UMR may be lower depending on implementation				

FEC5: Error Marking for Inner Code

- If the detected uncorrectable codewords does not have further stage of error correction, it should be marked to discard as in Slides #13.
  - RS(544,514) used in 802.3bs or as an outer code should be error marked because it is the last stage of error correction.
  - Error marking on inner code will corrupt the message, and the corresponding codewords that could be corrected by the outer code can no longer be corrected.



Refer to: [he_b400g_01_210426]

Summary:

- From PCS, FEC and PMA sublayer in 800G/1.6TbE MAC/PHY perspective:
  - The concatenated codes proposed in this contribution can help to build a holistic logical architecture.

Thank you