# **Concatenated FEC Proposal for 200G/Lane PMD**

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May 18, 2022 IEEE 802.3df May 2022 session

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## **Goal of the presentation**

In this presentation we review a concatenated FEC scheme that works in conjunction with the standard KP FEC in the host. The proposed concatenated FEC is a simple soft decision FEC scheme that sits in the DSP SerDes inside the optical module.

This scheme will provide a coding boost to the overall concatenated FEC scheme and will relax the overall link budget as a result.

## FEC Architecture : End-to-End, Concatenated, Segmented



Source: https://www.ieee802.org/3/df/public/22\_02/shrikhande\_3df\_01a\_220203.pdf

## What is inside the Data center Optical modules today?

 "Re-timers" and "gearboxes" represent the bulk of DSP deployed inside the IM-DD optics today



## **Concatenated FEC extends this concept for NextGen – 200G/lambda**

- n:1 "gearbox" generalized to a simple convolutional inter-leaver
- Inner FEC code concatenated with the interleaved bit stream



## Various FEC Proposals : Baseline Assumptions

- KP4 FEC RS(544,514) : Pre-dominantly used in 100G/lane  $\rightarrow$  extended to 800G ETC mode
- RS(576,514) Slight better flavor of KP4 FEC but with more complexity proposed for 200G electrical channels
- KP4 + Hamming (128,120) Concatenated FEC candidate works in conjunction with Host KP4 FEC

FEC Type	Baud Rate	Pre-FEC BER threshold	Net Coding gain	Comments
RS(544,514)	PAM4: 106.25G	2.2E-4	7dB	* Leverages existing KP4 FEC, exists in switches, PHY today
RS(576,514)	PAM4:112.5G	1.1E-3	8dB	* Hard decision FEC
RS(544,514)+ Hamming (128,120)	PAM4:113.3G	4.85E-3	9.5dB	* Enhanced KP4 FEC with Soft decision Concatenated FEC proposal for 200G/lane

#### Performance of KP4 FEC Vs RS(576,514) Vs KP4 + Hamming (128,120)



#### **Generic Concatenated FEC Architecture**



• Lane Permutation block - it may be present for certain PMD types only

### **Purpose of Convolutional Interleaver for Concatenated FEC**



- The *Convolutional Interleaver* ensures each hamming code word encodes 12 10bit RS symbols from *different* Reed-Solomon codewords.
- 8 parity bits are computed over **12** (10b) RS Symbols.
- Burst error tolerance is a function of bit-symbol mapping block.

## Parametrized view of Per-lane Convolutional Interleaver

- Convolutional interleaver is defined per PCS lane
- Parameters for the per-lane convolutional interleaver
  - W: Number of KP4 RS codewords in each "word"
  - P: Number of sublanes of interleaver
  - D: Number of "word" delays
  - k : Time index
  - in[k]: Input "word" at time index k
  - out[k]: Output "word" at time index k



#### **Convolutional Interleaver + Hamming (128,120) Latency for 200G per Lane PMD**

Client Type	Parameters for Interleaver	FEC	Decoder Input BER	Latency
400GBASE-R (Clause 119)	W=2 P=6 D=6		4.85E-3	~140ns
800G-PCS assuming ETC Type	W =4 P =6 D =6	KP4 + Hamming (128,120)		~55ns
800G –PCS assuming speed up version of CL-119	W =2 P= 6 D= 6			~70ns

#### Concatenated FEC scheme : Keeping it Backward compatible & Forward looking



## Summary

- Simple concatenated soft FEC like hamming (128,120) can provide more than enough coding boost to enable 200G PMD over multiple mediums
- Leveraging the existing KP4 FEC for 200G AUI will benefit the industry and will ease the backward compatibility issues.
- Overhead for KP4 + SFEC is similar to stronger Hard coded FEC like RS(576,514) : 113.3Gbaud Vs 112.5 Gbaud while the concatenated scheme provide a better overall coding gain.

# Thanks !