

Logic Architecture Straw Poll

IEEE P802.3df Task Force
IEEE 802.3 May 2022

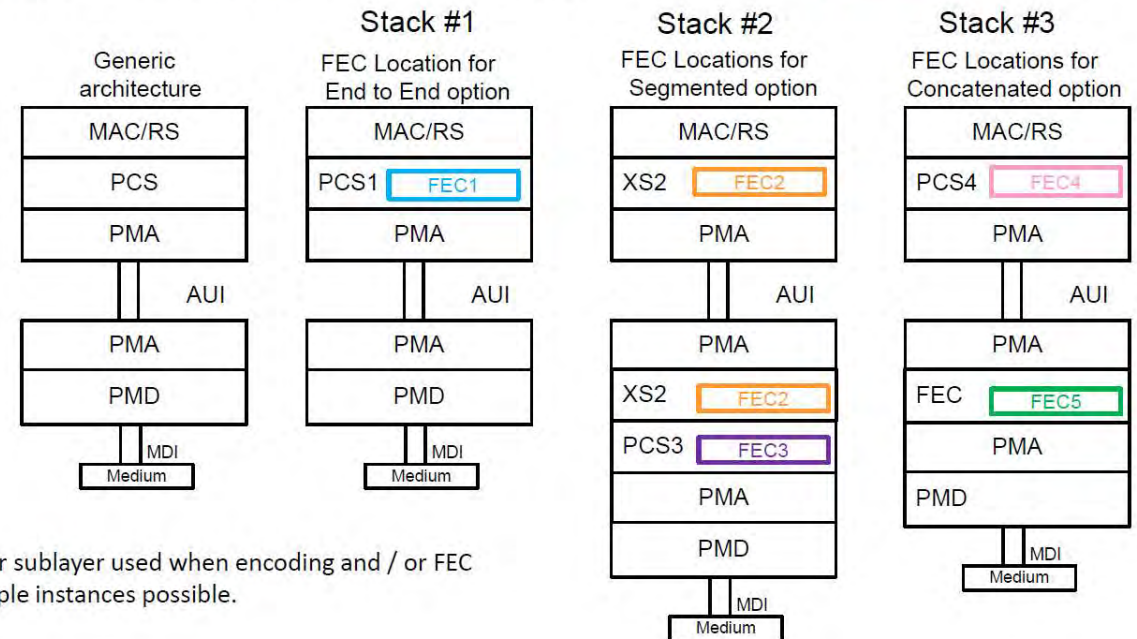
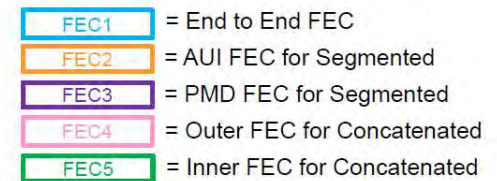
Mark Gustlin – Cisco

802.3df Architecture Proposal

- An architecture is proposed in [gustlin_3df_01a_220517.pdf](#) for all Ethernet rates in this project
- Supports all anticipated/proposed FEC schemes
- Consistent across Ethernet rates

Proposed 802.3df Overall Architecture

- For all Ethernet rates within this project (200G/400G/800G/1.6T)
- FECs might or might not be reused across schemes
- TBD which FEC scheme(s) are needed for this project



Note – Extender sublayer used when encoding and / or FEC changes. Multiple instances possible.

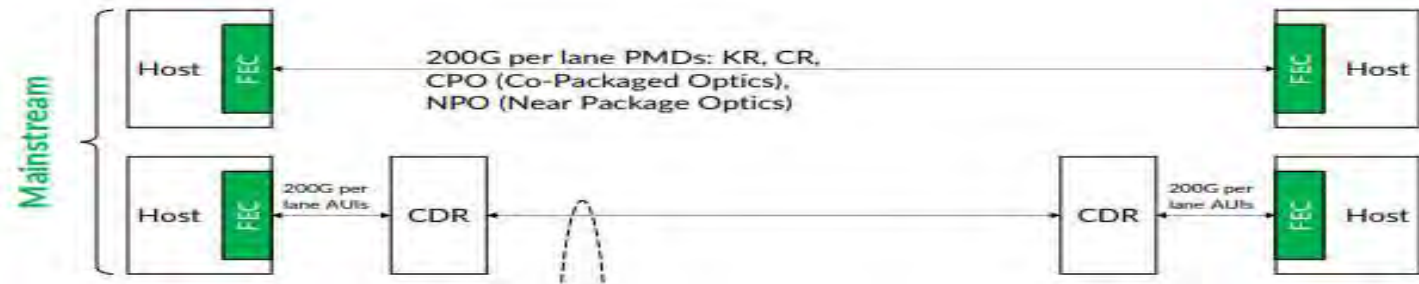
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From: [gustlin_3df_01a_220517.pdf](#)

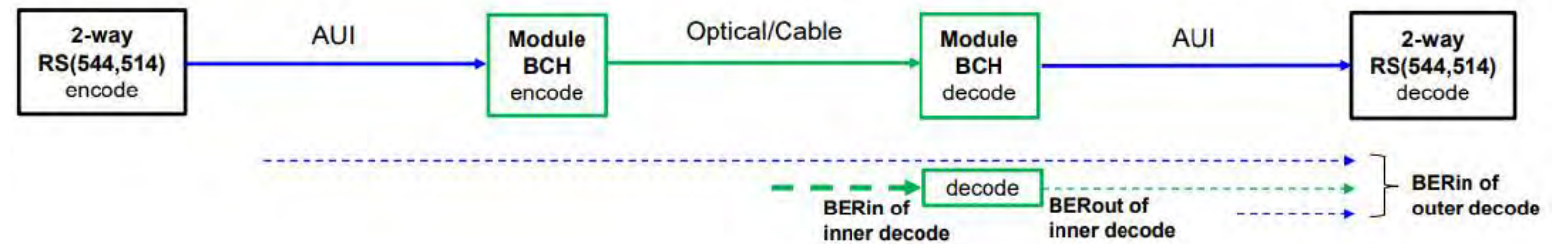
802.3df Architecture Proposal – FEC Schemes

- To reiterate, this architecture supports all anticipated/proposed FEC schemes:

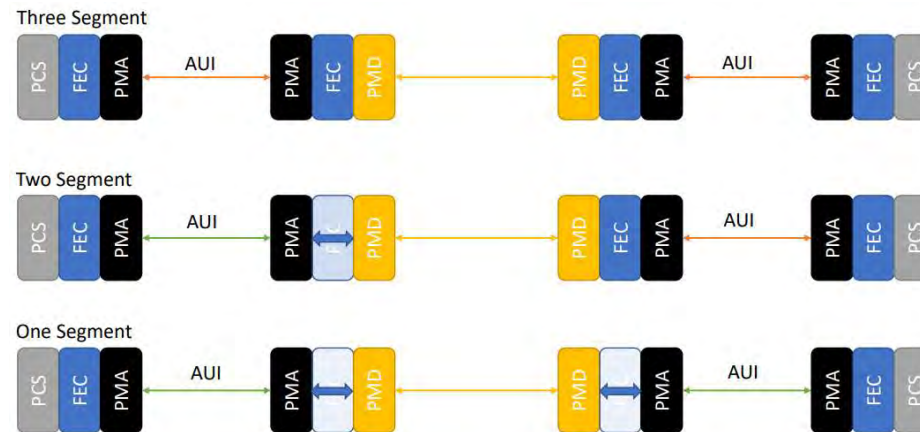
End to end FEC as shown, for example, in lu_3df_logic_220425.pdf



Concatenated FEC as shown, for example, in wang_3df_01_220517.pdf



End to Segmented FEC as shown, for example, in welch_3df_logic_220425.pdf



Proposed Straw Poll

- I would support adopting the architecture described in [gustlin_3df_01a_220517](#) as the basis for the logic architecture for IEEE P802.3df
 - Y
 - N
 - Need more information

Proposed Motion

- Move to adopt the architecture described in `gustlin_3df_01a_220517` as the basis for the logic architecture for IEEE P802.3df
 - Y
 - N
 - Abstain

Thanks!