IEEE P802.3df Architecture and Logic
June Ad Hoc Meetings Report

Mark Gustlin, Cisco
Architecture and Logic Ad Hoc Chair

Report

- Charter: The Architecture and Logic Ad Hoc is chartered to address the following:
  - 1) Develop terminology and definitions for terms related to architecture, including but not limited to FEC Architecture, FEC Scheme, End-to-end FEC, Segmented FEC, Concatenated FEC. Draft definitions to be presented to Task Force at May 2022 session.
  - 2) Act as forum to discuss architectural requirements and consider proposals related to PCS, FEC, and PMA logic sublayers.
- 2 ad hoc calls since May 2022 meeting
  - 23 June 2022, 30 June 2022
  - 80+ attendees
  - 7 contributions presented
- Meeting minutes and presentation materials: https://www.ieee802.org/3/df/public/adhoc/logic/index.html
- Next meeting: TBD

Presentations

- 23 April 2022
  - 800GbE PCS and PMA Baseline Proposal for 100Gbs/s per lane PHYs (draft), Xinyuan Wang
  - 800GbE baseline proposal for RS, MII, Time Sync (Clause 90), Extender/ XS and PMA, Gary Nicholl, Arthur Marris
  - Describing the FEC frame and rate adaption for 800G and 1.6T PCS, Tom Huber
  - Baseline proposal for 800GbE and 1.6TbE PCS, FEC and PMA using 100G PMD lanes, Yuchun Lu
- 30 April 2022
  - Comparison of Two 800GbE PCS and PMA Baseline Proposals for 100 Gb/s per lane PHYs; Xinyuan Wang, Matt Brown
  - BER and FLR Analysis for Random and Burst Errors for 8x100 PCS; Eugene Opsasnick, Cathy Liu
  - On clock issue for two parallel 400G PCS flows; Ryan Wong

Straw Polls

- No official straw polls for these sessions, but we did have discussions around some questions posed by Gary Nicholl from “800GbE baseline proposal for RS, MII, Time Sync (Clause 90), Extender/ XS and PMA”, summaries are posted in the meeting minutes

THANKS!