212.5 Gbps Chip-to-Module (C2M) Link Simulation and Analysis

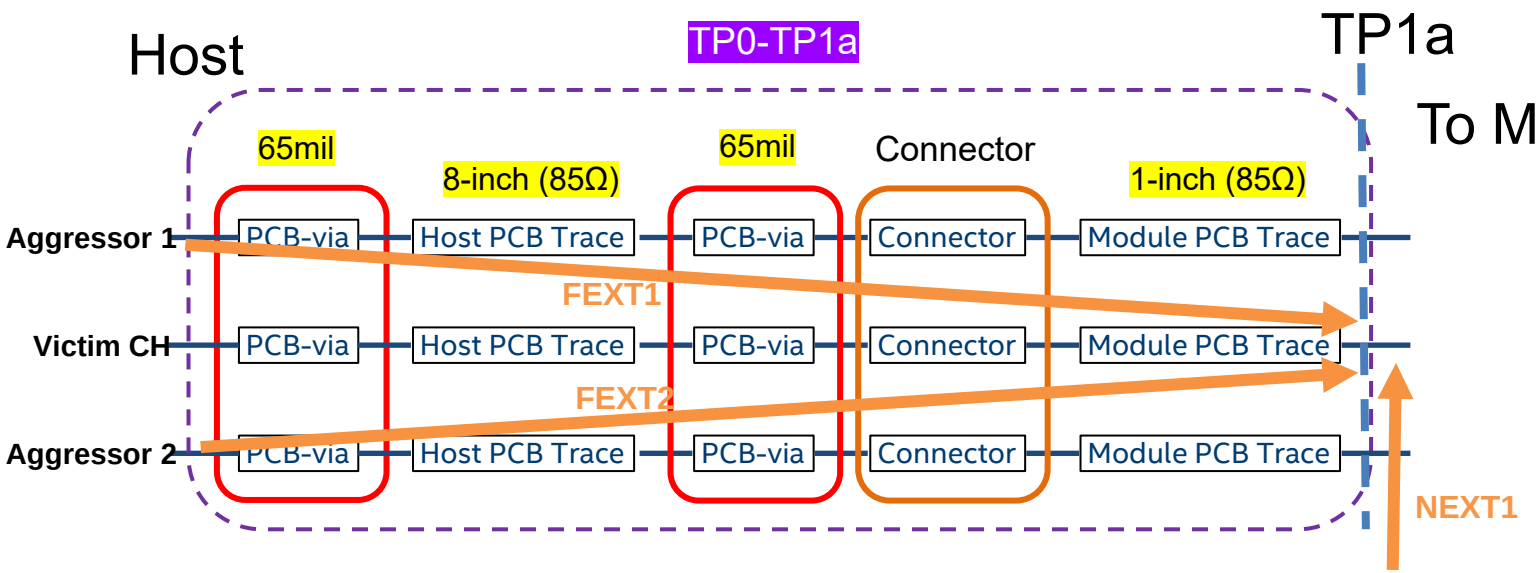
Mike Li, Hsinho Wu, Jenny Xiaohong Jiang, Masashi Shimanouchi,
Itamar Levin, Ariel Cohen, Ram Muthukaruppan (Intel)
Michael Rowlands, Sam Kocsis, Ali Hammoodi (Amphenol)

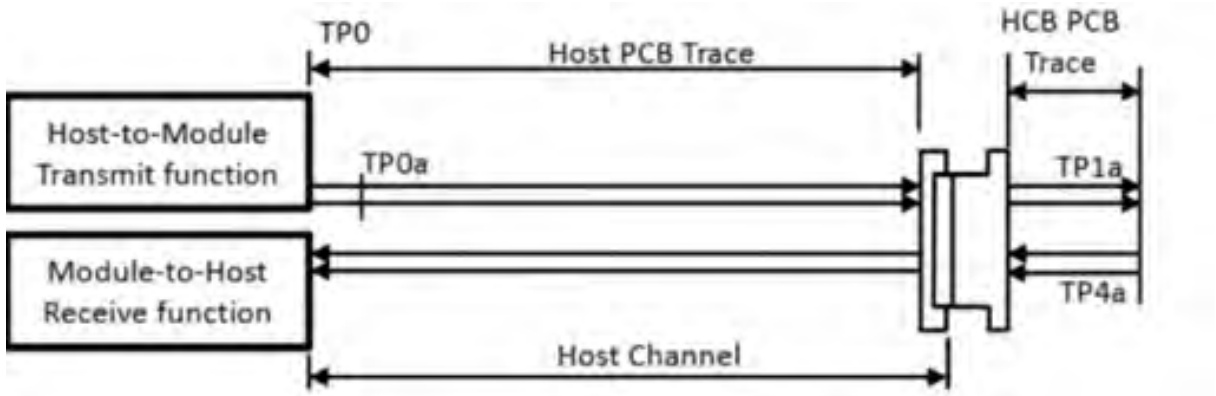
July 13, 2022

Background and Introduction

- Update to Q1'22 presentation "224 Gbps Chip-to-Module Link Simulation and Analysis Update" (oif2022.174.01), with
  - Proposed chip-to-model COM configuration and analysis results
  - New link simulation results appropriate to 802.3df
- Update to Q3'21 presentation "*212/224 Gbps Chip-to-Module Link Simulation and Analysis*" (oif2021.446.00), with
  - Latest C2M channel model(s)
  - Proposed CEI-224G-LR-PAM4 reference TX (oif2022.067.00)
  - Proposed CEI-224G-LR-PAM4 reference die/package model (oif2022.065.02)
  - TP1a reference scope RX based on the proposed CEI-224G-LR-PAM4 reference RX AFE (oif2022.067.00)

C2M Channel Topology

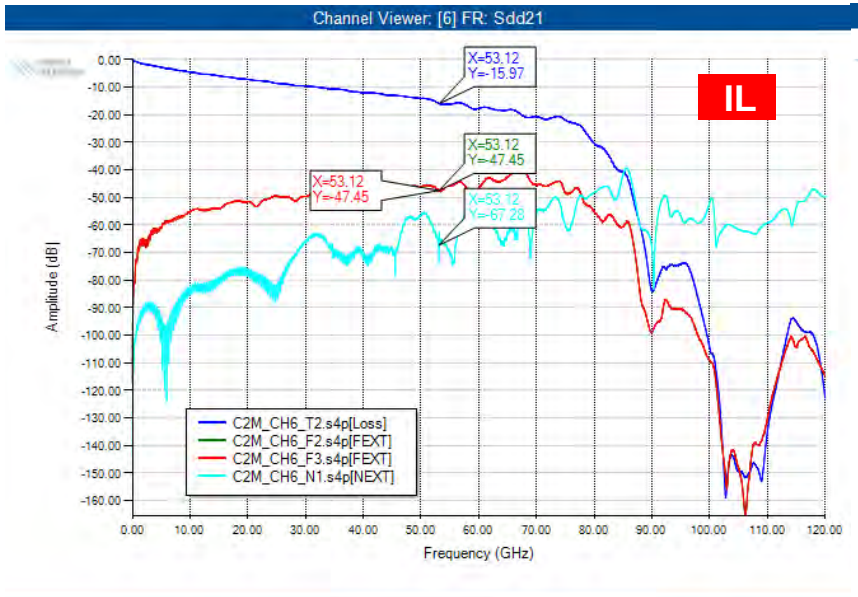


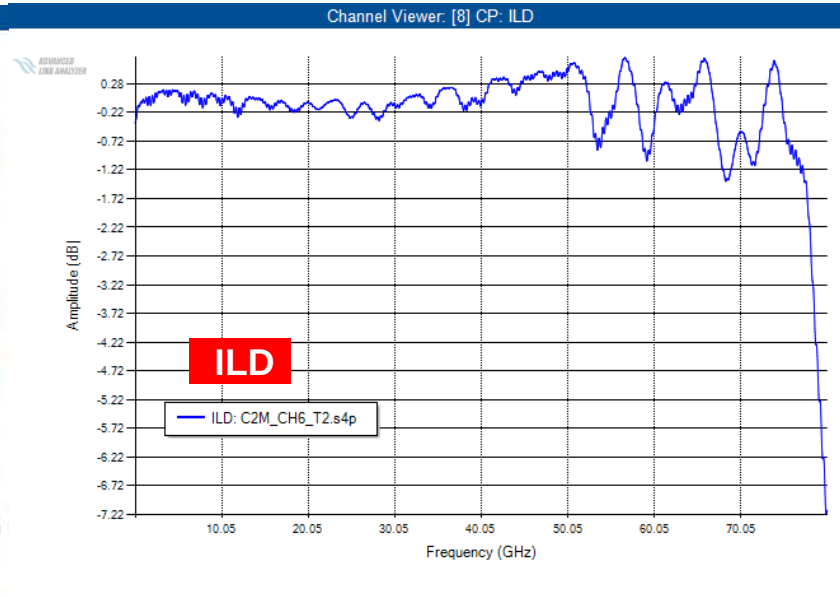


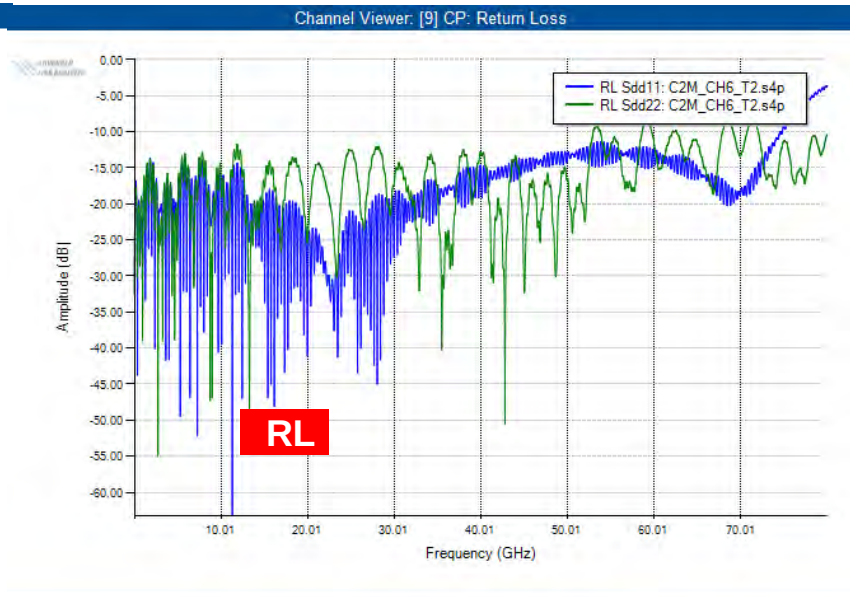
Channel Configuration Summary

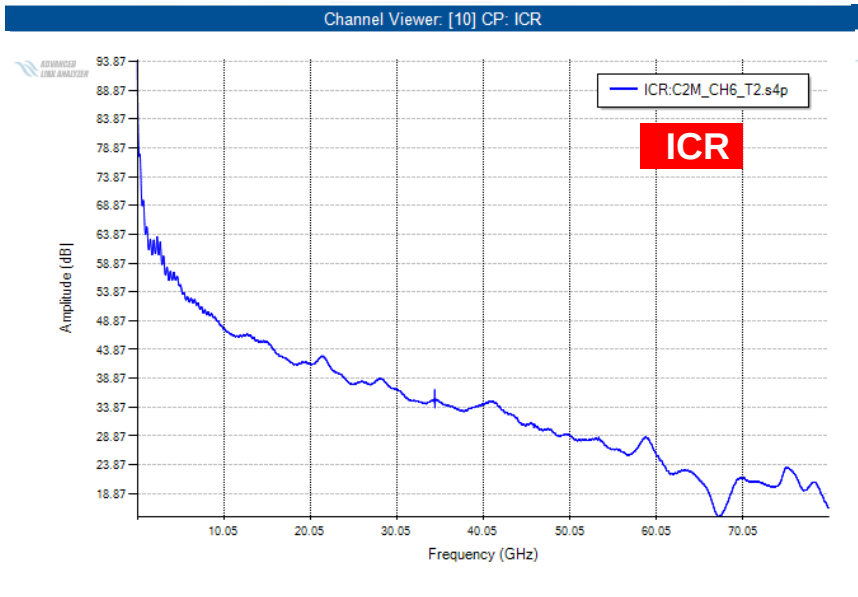
- 2 Channels were analyzed
  - CH6: Shown on the left
  - CH7: Same as CH6, but with improved connector
- Crosstalk
  - 2 FEXT
  - 1 NEXT

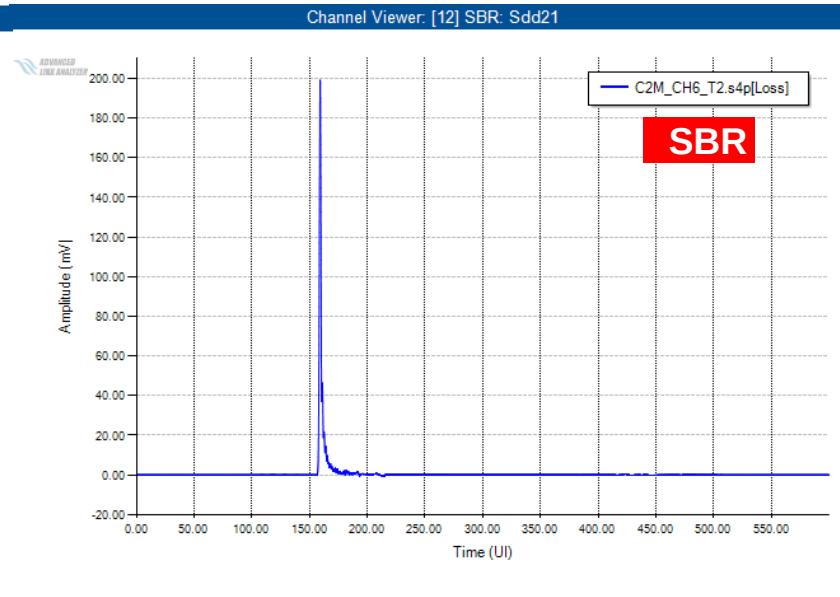
C2M Channel Characteristics (CH6)





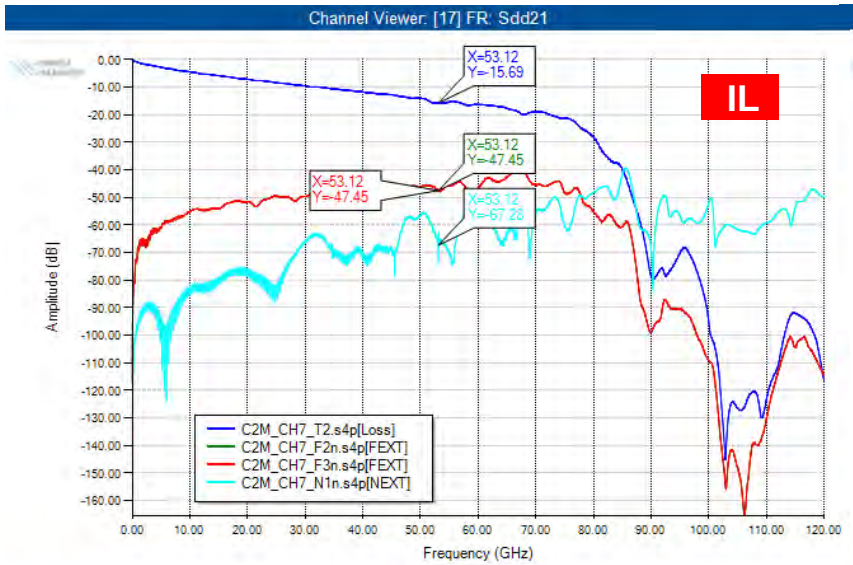


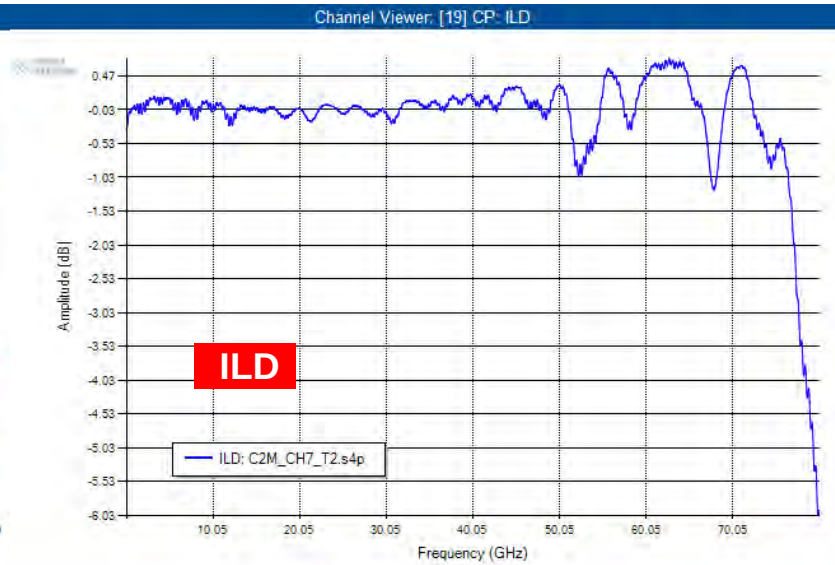


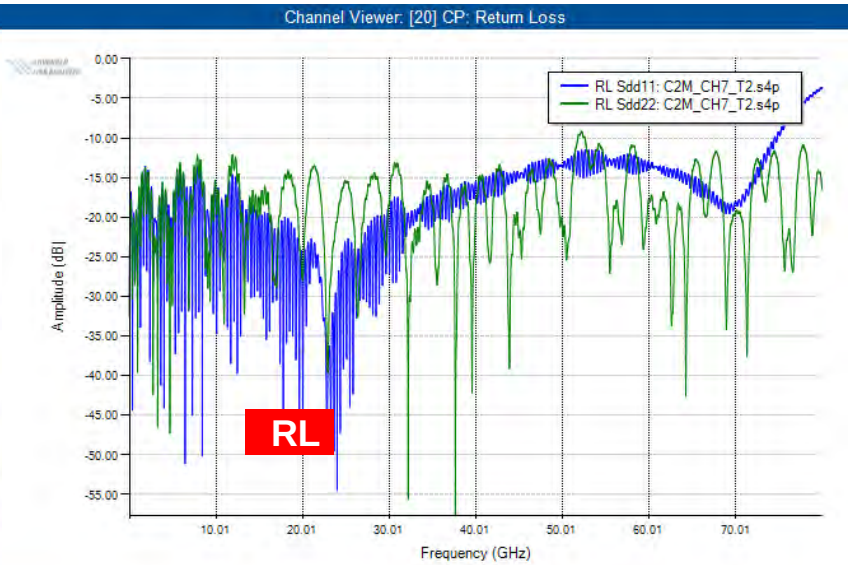


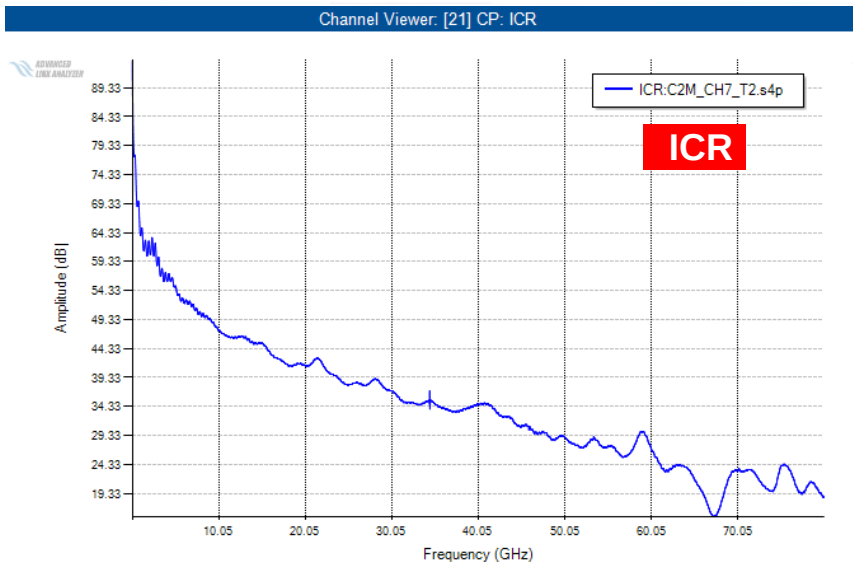
- IL: 15.97dB @ 53.125GHz
- ILD ~= 1dB
- RL ~= 10dB
- FEXT ~= 44dB NEXT ~= 53dB, ICR ~= 28dB

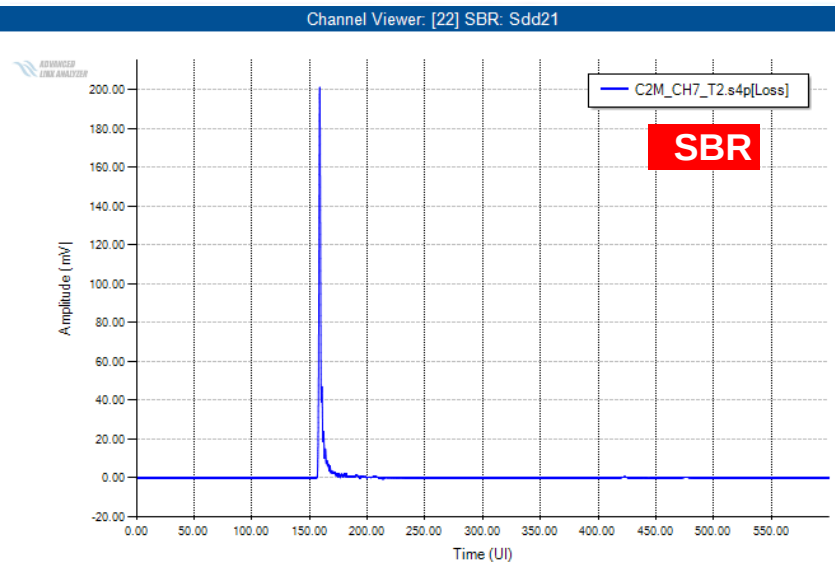
C2M Channel Characteristics (CH7)











- IL: 15.69dB @ 53.125GHz
- ILD ~= 1dB
- RL ~= 10dB
- FEXT ~= 44dB NEXT ~= 53dB, ICR ~= 28dB

Preliminary 212.5Gbps PAM4 COM Analysis

for C2M/VSR Channel TP1a Test

- Based on 802.3ck chip-to-Module COM with the following changes
  - TP1a COM Test Configuration:
    - Proposed CEI-224G-LR-PAM4 reference TX, die, and package models
      - RLM = 0.95, SNRTX=33dB, BUJ = 0.02UI_{pk}, RJ = 0.01UI_{RMS}
      - TX Package: 31mm
    - TP1a Reference Receiver (Scope)
      - Based on scaled 802.3ck C2M reference RX with 8-tap DFE, and Input Referred Noise = 2.05x10^{-8} V^2/GHz
    - DER: 10^{-5}
- Preliminary COM analysis results

212.5Gbps PAM4 (DER =10^{-5})

Channel	VEO	VEC	COM
CH6	9.19 mV	11.405 dB	2.722 dB
CH7	10.16mV	10.648 dB	3.018 dB

Preliminary COM Configuration

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0e-4; 0.9e-4, 0e-4; 1.1e-4, 0e-4]	nF	[TX RX]
L_s	[0.13, 0; 0.15, 0; 0.14, 0]	nH	[TX RX]
C_b	[0.3e-4, 0e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]
C_p	[0.4e-4 0e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
L	4		
M	32	Samp/UI	
samples_for_C2M	100	Samp/UI	
T_O	50	mUI	
AC_CM_RMS	0	V	[test cases]
filter and Eq			
f_r	0.5	*fb	
c(0)	0.5		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.16]		[min:step:max]
c(-3)	[-0.1:0.02: 0]		[min:step:max]
c(-4)	[0:0.02:0.1]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	8	UI	
b_max(1)	0.6		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,6)]		As/dfe2..N_b
b_min(1)	0.3		As/dffe1
b_min(2..N_b)	[-0.3 -0.2*ones(1,6)]		As/dfe2..N_b
g_DC	[-13:1:-0]	dB	[min:step:max]
f_z	25.16	GHz	
f_p1	40	GHz	
f_p2	56	GHz	
g_DC_HP	[-3:0.5:-0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
G_Qual	[]	dB	ranges
G2_Qual	[]	dB	ranges
GDC_Min	0	dB	0 disables check.

maybe different for each interface.

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	12	db
EH_min	8	mV
ERL Pass threshold	7.3	dB
Min_VEO_Test	5	mV
DER_0	0.00001	
T_r	0.003	ns
FORCE_TR	1	5
PMD_type	C2M	
BREAD_CRUMBS	0	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	0	logical
TDR and ERL options		
TDR	1	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	800	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0.2e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	0	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	2.05E-08	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.00089 0.000155]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
ICN & FOM_ILD parameters		
f_v	0.742	*Fb
f_f	0.742	GHz f_r specified in first column
f_n	0.742	GHz
f_2	40	GHz
A_ft	0.600	V
A_nt	0.600	V

Histogram_Window_Weight	Gaussian	gaussian. triangle, rectangle
sigma_r	0.02	sigma in UI fo or gaus.. Wind

Table 92–12 parameters	
Parameter	**Setting**
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]
board_tl_tau	0.00579
board_Z_c	100
z_bp (TX)	407
z_bp (NEXT)	407
z_bp (FEXT)	407
z_bp (RX)	407
C_0	0
C_1	0
Include PCB	0

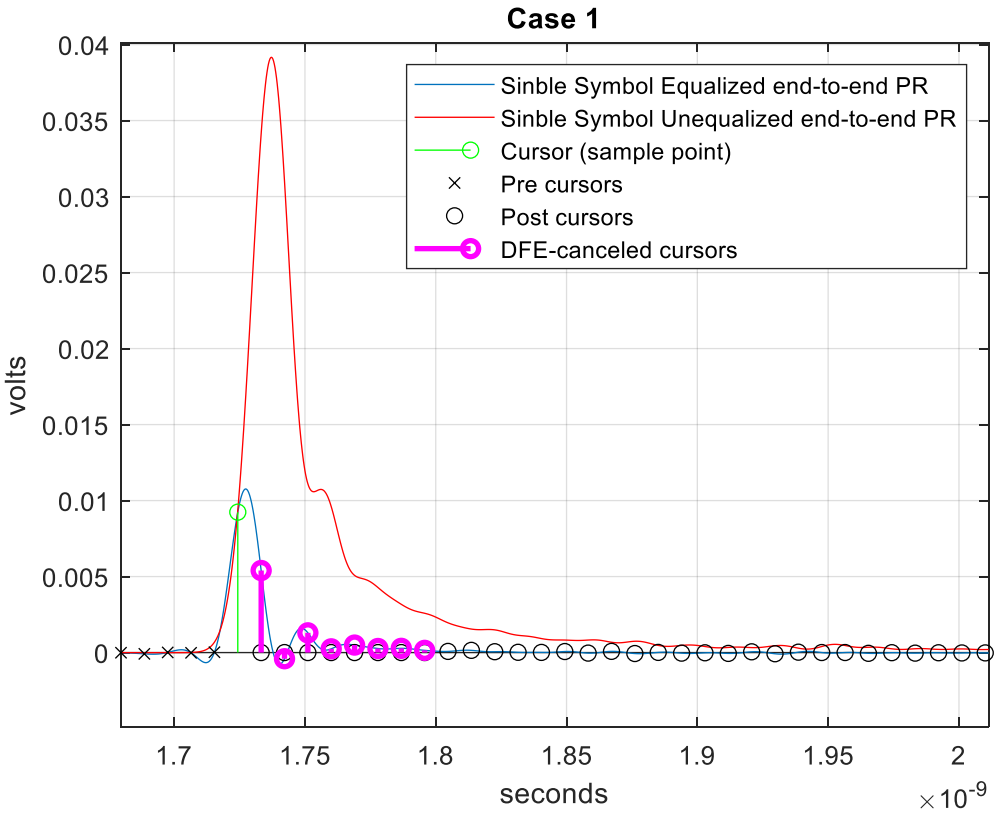
different for each test fixture

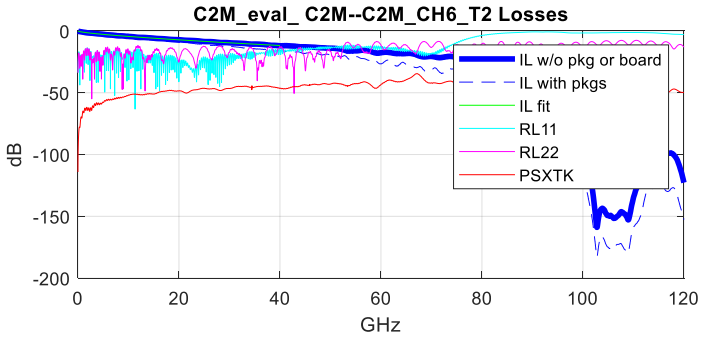
updated for 802.3ck C2M

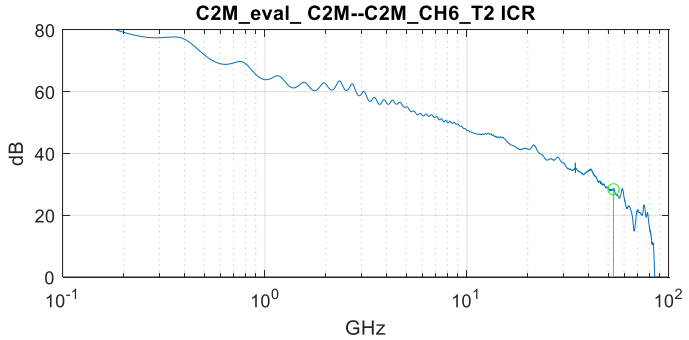
Floating Tap Control	
N_bg	0
N_bf	3
N_f	40
bmaxg	0.2

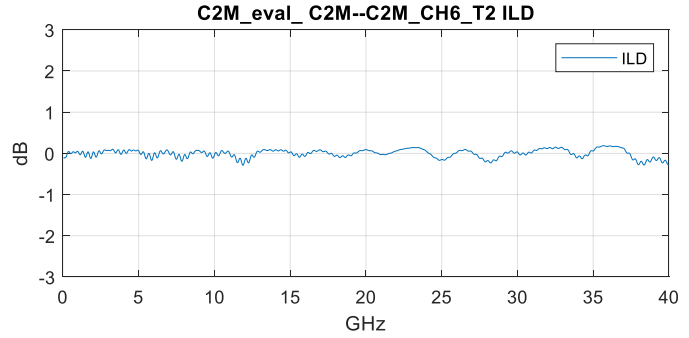
Preliminary 212.5Gbps PAM4 COM Analysis (CH6)

TP1a

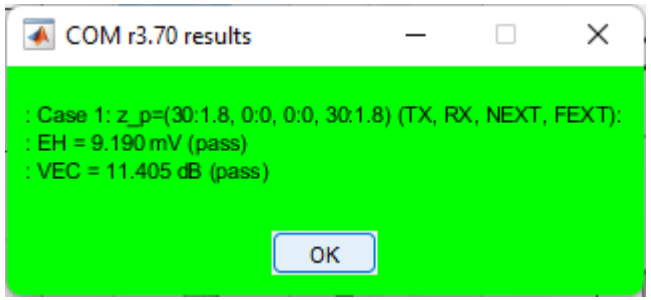






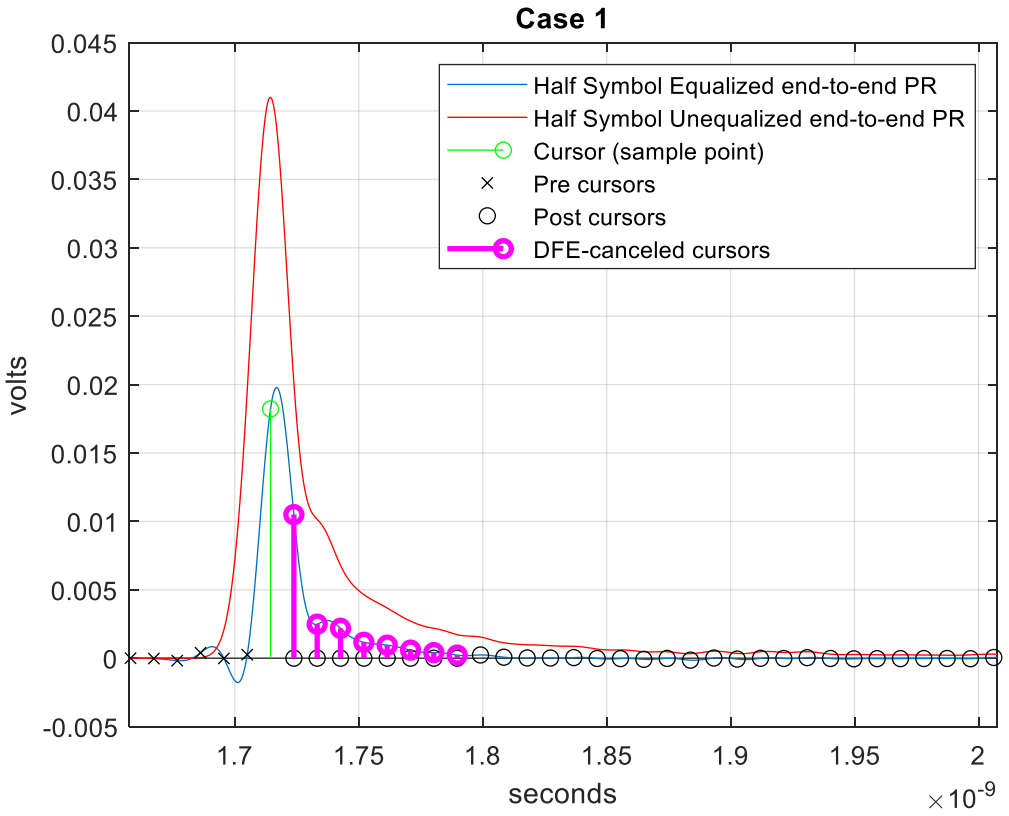


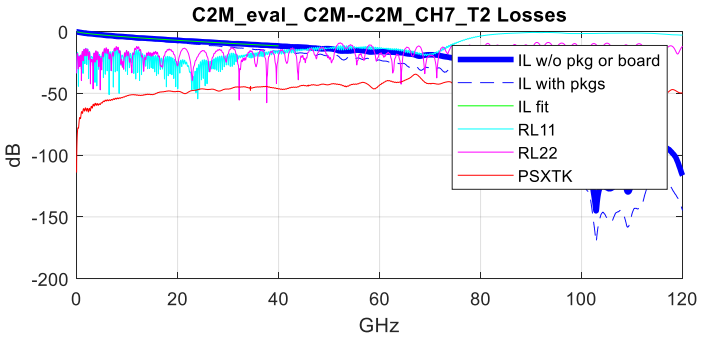
- EH = 9.19 mV
- VEC = 11.405dB
- DER = 1e-5
- DER Threshold = 1.1106e-12
- COM = 2.7218dB
- TXLE_taps: [0 -0.0200 0.1000 -0.2800 0.6000 0]
- CTLE_DC_gain_dB: -1
- g_DC_HP: -2

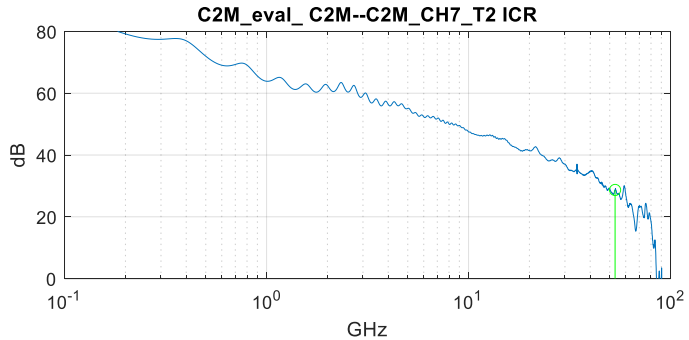


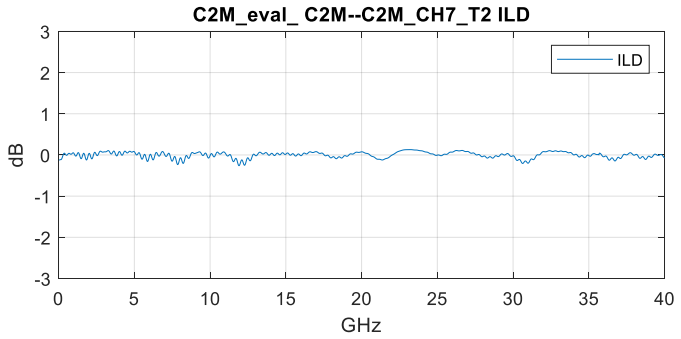
Preliminary 212.5Gbps PAM4 COM Analysis (CH7)

TP1a

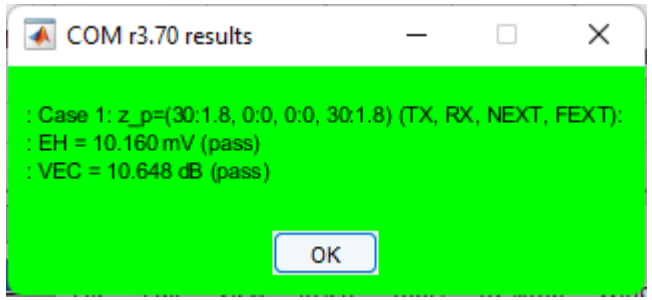




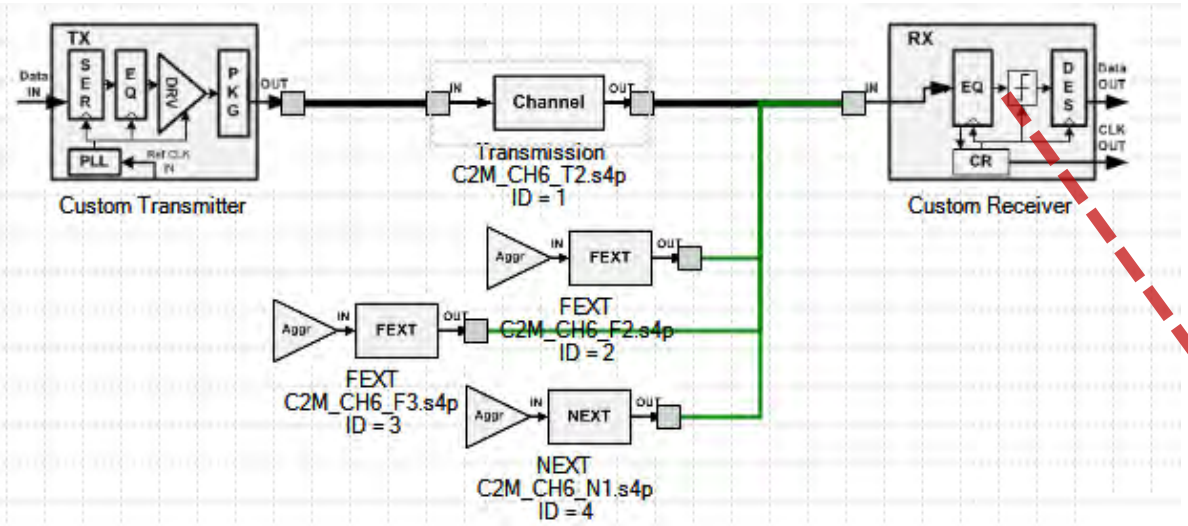




- EH = 10.16 mV
- VEC = 10.648dB
- DER = 1e-5
- DER Threshold = 1.1331e-14
- COM = 3.0178dB
- TXLE_taps: [0 -0.0200 0.1000 -0.2800 0.6000 0]
- CTLE_DC_gain_dB: -1
- g_DC_HP: -2

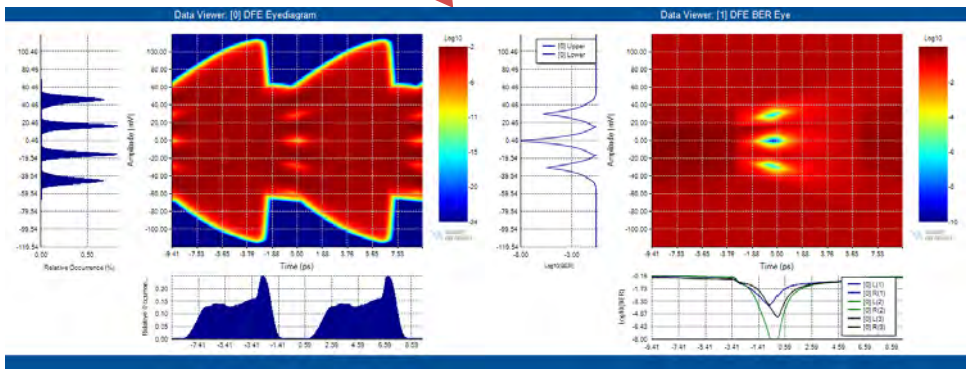


212.5Gbps PAM4 C2M TP1a Simulation (CH6)



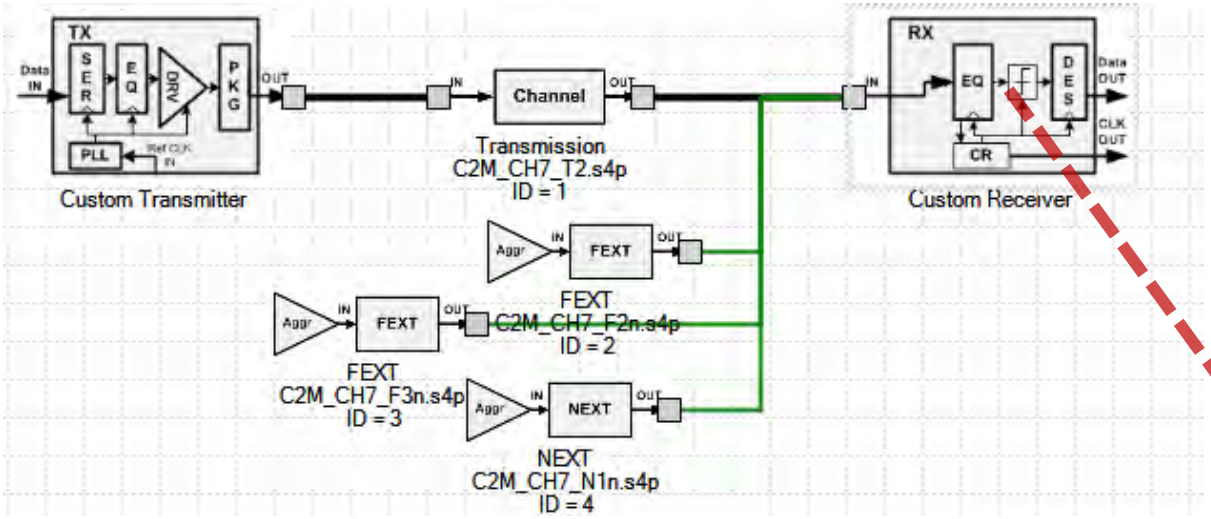
Simulation Configuration

- Test Pattern: PRBS-13Q
- Transmitter: Proposed CEI-224G-LR-PAM4 reference TX, die, and package
  - RLM = 0.95, SNR_{TX}=33dB, BUJ = 0.02UI_{pk}, RJ = 0.01UI_{RMS}
  - TX Package Length: 31mm
- TP1a Reference Receiver (Scope)
  - Based on scaled 802.3ck C2M reference RX with 8-tap DFE, and Input Referred Noise = 2.05×10^{-8} V^2/GHz
- Channel: C2M channel with 2 FEXTs and 1 NEXT
- DER = 10^{-5}



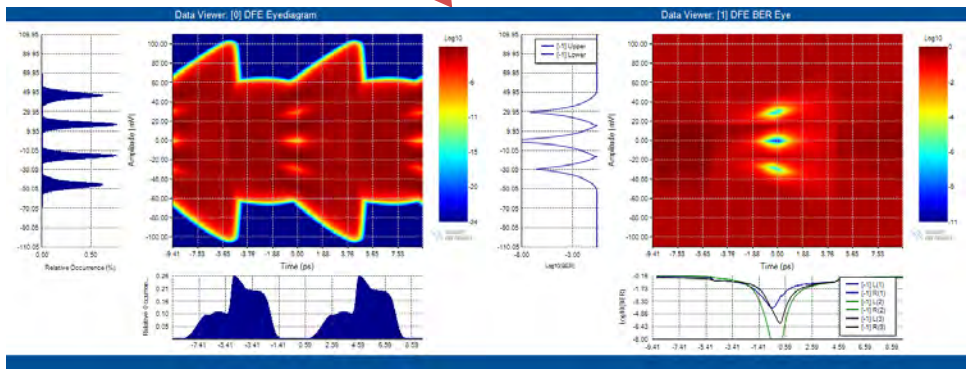
TP1a RX output
EH = 3.80mV, EW = 0.06UI VEC = 14.32dB @ DER=1e-5

212.5Gbps PAM4 C2M TP1a Simulation (CH7)



Simulation Configuration

- Test Pattern: PRBS-13Q
- Transmitter: Proposed CEI-224G-LR-PAM4 reference TX, die, and package
  - RLM = 0.95, SNR_{TX}=33dB, BUJ = 0.02UI_{pk}, RJ = 0.01UI_{RMS}
  - TX Package Length: 31mm
- TP1a Reference Receiver (Scope)
  - Based on scaled 802.3ck C2M reference RX with 8-tap DFE, and Input Referred Noise = 2.05x10^{-8} V^2/GHz
- Channel: C2M channel with 2 FEXTs and 1 NEXT
- DER = 10^{-5}



TP1a RX output
EH = 4.49mV, EW = 0.07UI VEC = 13.15dB
@ DER=1e-5

Summary & Conclusions

COM and Link Simulation Result Summ
212.5Gbps PAM4 (DER =10^{-5})

Channel	COM EH	COM VEC	Simulation Eye Opening Height	Simulation VEC
CH6	9.19 mV	11.405 dB	3.80 mV	14.32 dB
CH7	10.16mV	10.648 dB	4.49 mV	13.15 dB

- Preliminary COM and time-domain simulations with Intel/Amphenol latest C2M channels suggest good 212.5Gbps C2M TP1a performance/solution space with PAM4 modulation scheme.

212.5Gbps C2M TX EQ Pre-tap Length Revisited

- Background: In OIF CEI Q1'22 presentation "224 Gbps Chip-to-Module Link Simulation and Analysis Update" (oif2022.174.01), we proposed 6 pre-taps for TX EQ

- Two observations:
  - We have simulated and analyzed more channels and did not see the need for pre-tap 5 and pre-tap 6. The usage of pre-tap 4 is few.
  - Historically, we have observed the evolution of TX EQ pre-tap lengths, for both CEI/OIF and Enet:

Data Rate	TX EQ Pre-tap Length
25Gbps	1
53Gbps	2
106Gbps	3

212.5Gbps C2M TX EQ Pre-tap Length Proposal

- Based on the studies and observations from previous generations, we propose to have 4 TX pre-taps as a baseline start for the upcoming 212.5Gbps per-lane C2M electrical spec.