Starting Point: Chip to Chip (C2C) Mezzanine Test Board Channels for 200 Gb/s PAM 4

Abstract: Research grade C2C test board measurements of channels presented. In addition, an emulated channel example TP0-TP5 is provided.

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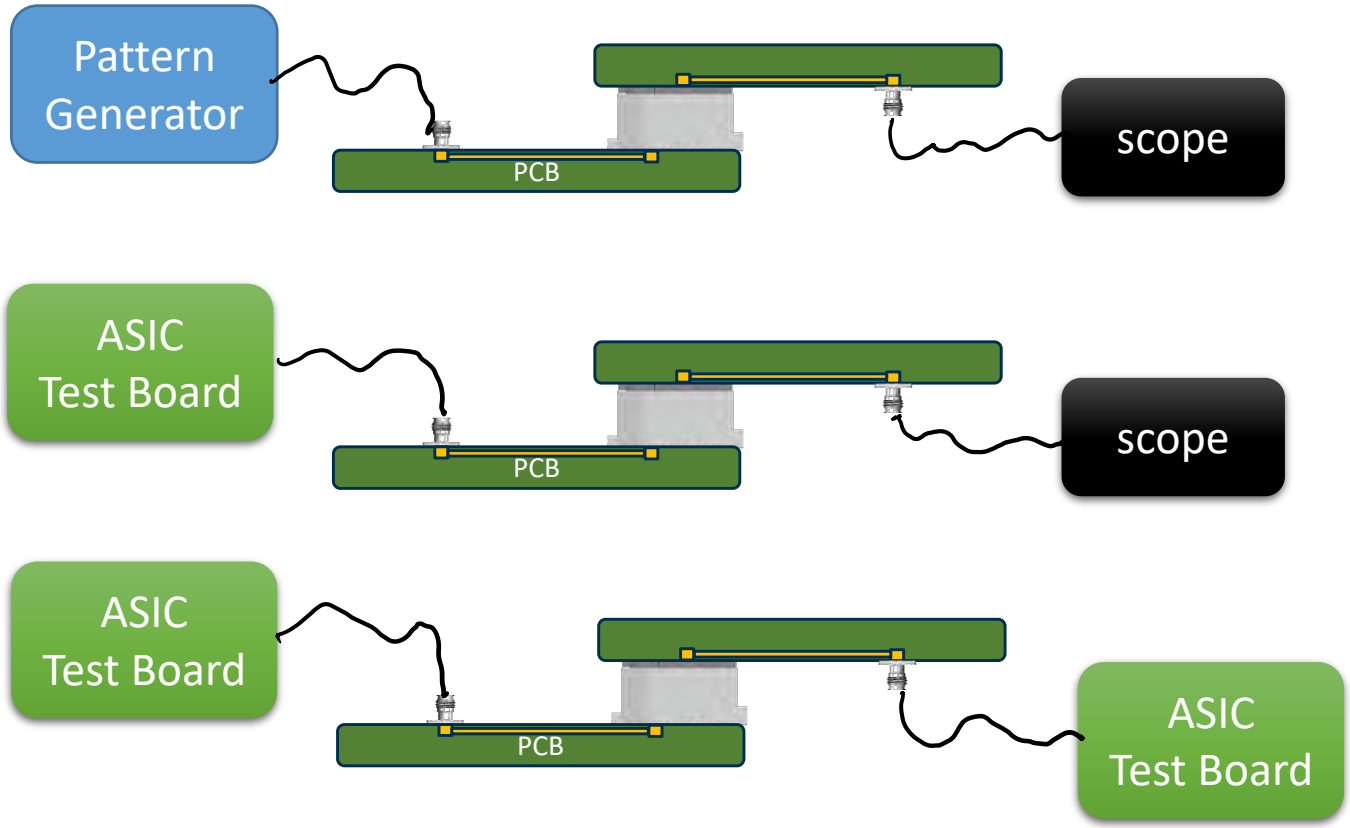
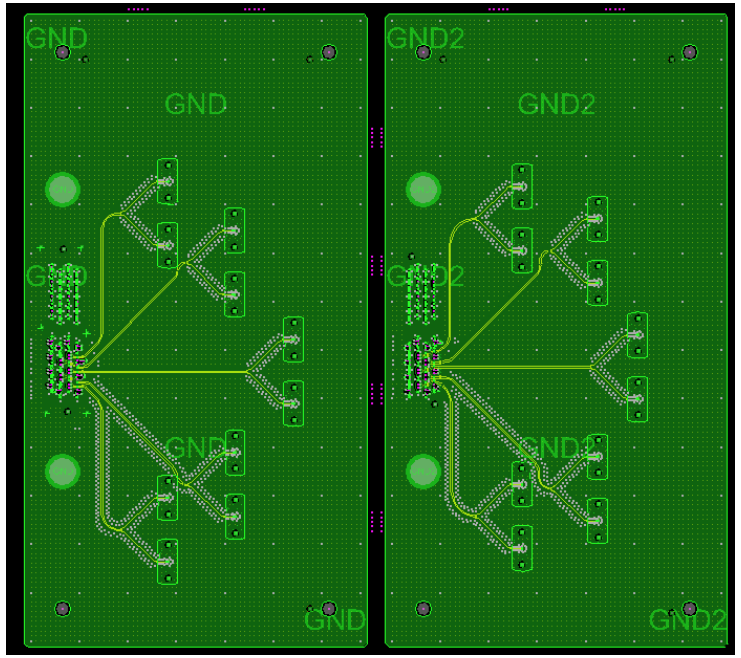
Background: Research grade C2C test board

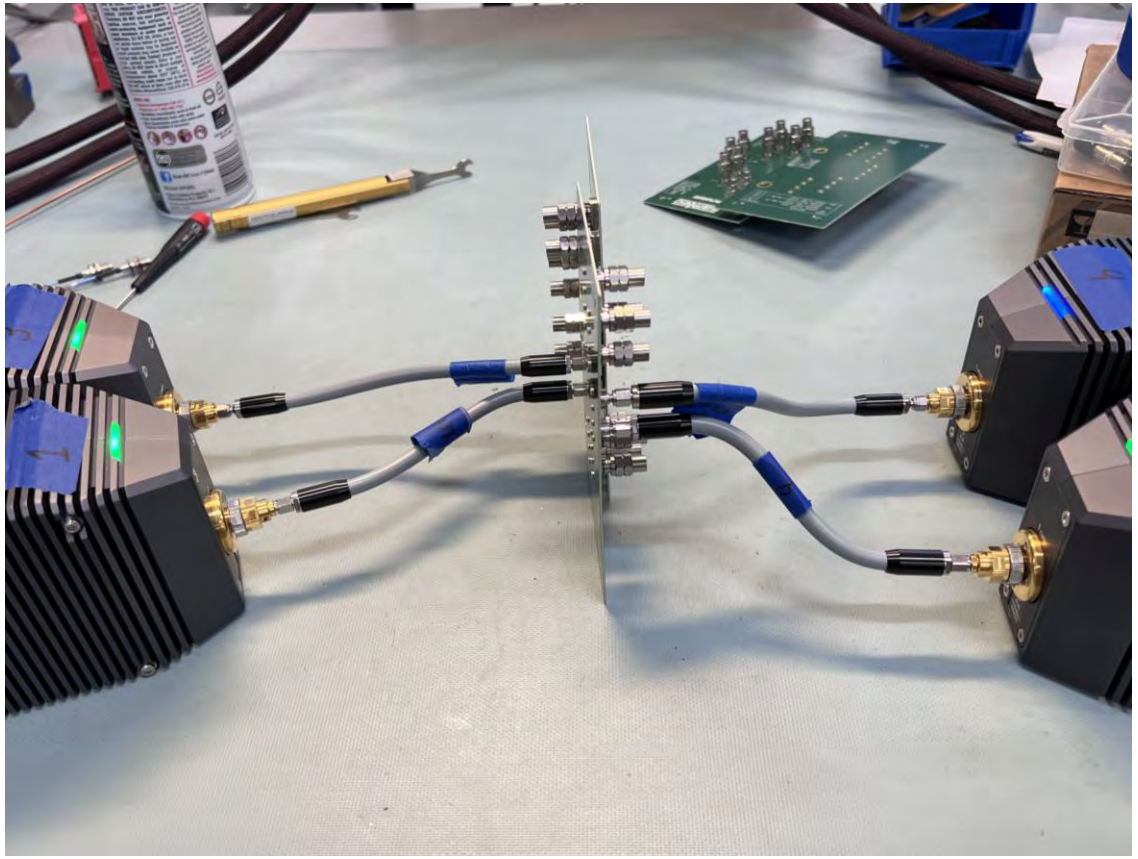
POTENTIAL USES

- Board used for C2C development
  - Fungible test board
- Provide S4P Channel models
  - IL and FEXT
- These boards utilize 1 mm “SMA” connectors
- Cable models may be added to support several scenarios



Chip to Chip (C2C) Mezzanine Test Board

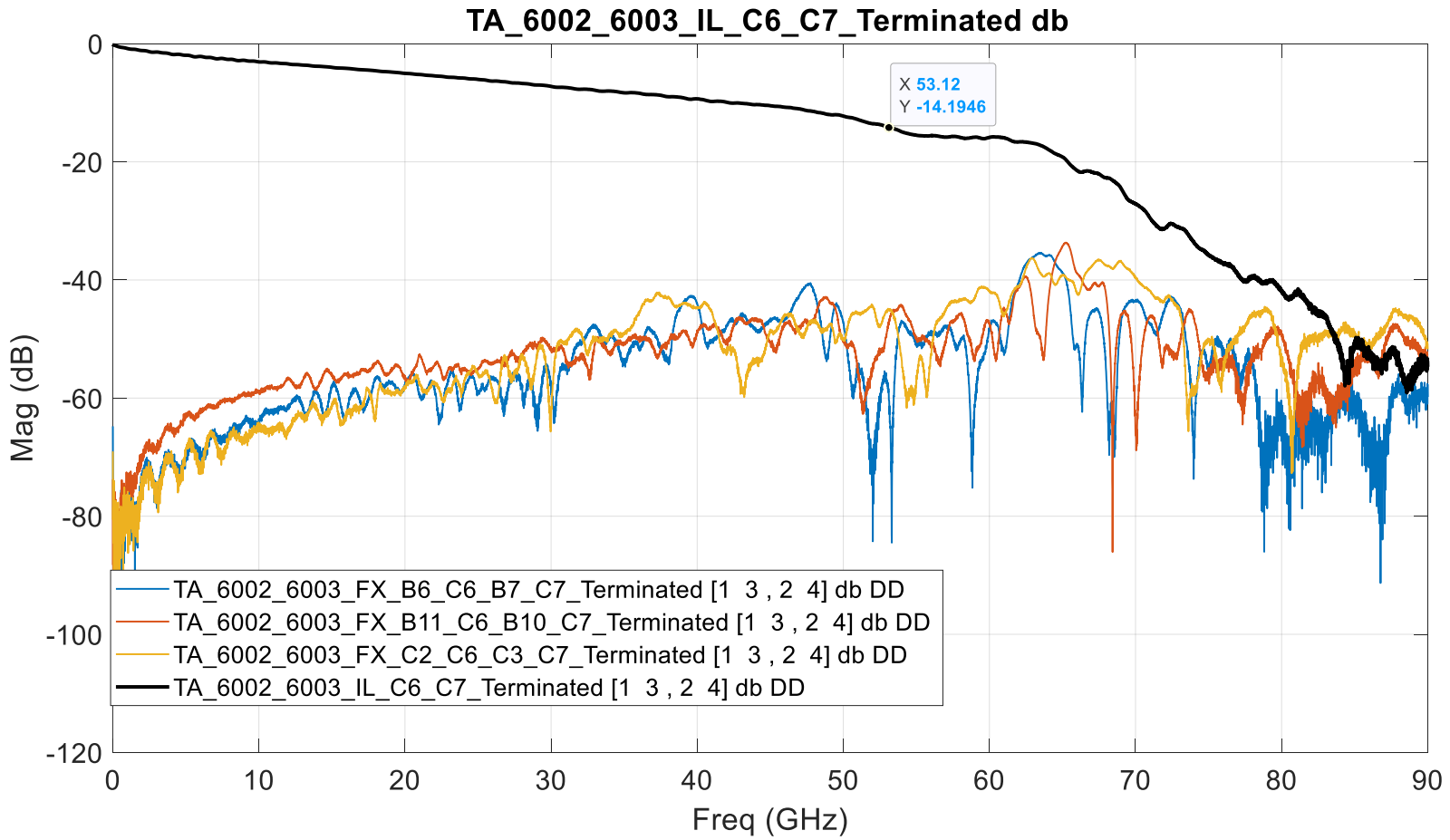




- 6 layer board using layer 2 with micro via routing
- 2” Tachyon 100G ~ 2.5 dB/in at 53.125 GHz
- Lower loss material board were made but results not included here

IL and Crosstalk

14 dB @ 53.125 GHz



2 Sets of Channel Files

1ST SET IS THE TEST BOARD,
2ND SET IS TEST BOARD WIRED TO A HYPOTHETICAL TEST CHIP

- Ports [1 3 2 4] ([tx+ tx-1 rx+ rx-])
  - TA_6002_6003_IL_C6_C7_Terminated.s4p
  - TA_6002_6003_FX_B11_C6_B10_C7_Terminated.s4p
  - TA_6002_6003_FX_B6_C6_B7_C7_Terminated.s4p
  - TA_6002_6003_FX_C2_C6_C3_C7_Terminated.s4p
- Ports [1 2 3 4] ([tx+ tx-1 rx+ rx-])
  - TA_6002_6003_IL_C6_C7_Terminated._tp0_tp5.s4p
  - TA_6002_6003_FX_B11_C6_B10_C7_Terminated_tp0_tp5.s4p
  - TA_6002_6003_FX_B6_C6_B7_C7_Terminated_tp0_tp5.s4p
  - TA_6002_6003_FX_C2_C6_C3_C7_Terminated_tp0_tp5.s4p

Chip to Chip Testing and Evaluation Setup

NO CROSS TALK IN BGA VIA REGION ON TP0/5 BOARDS

1” 1.9 dB/in @ 53 GHz

15 cm cable

PCB

1” 1.9 dB/in @ 53 GHz

Layer 3 with 4 mil stub from back drill

15 cm cable

Layer 3 with 4 mil stub from back drill

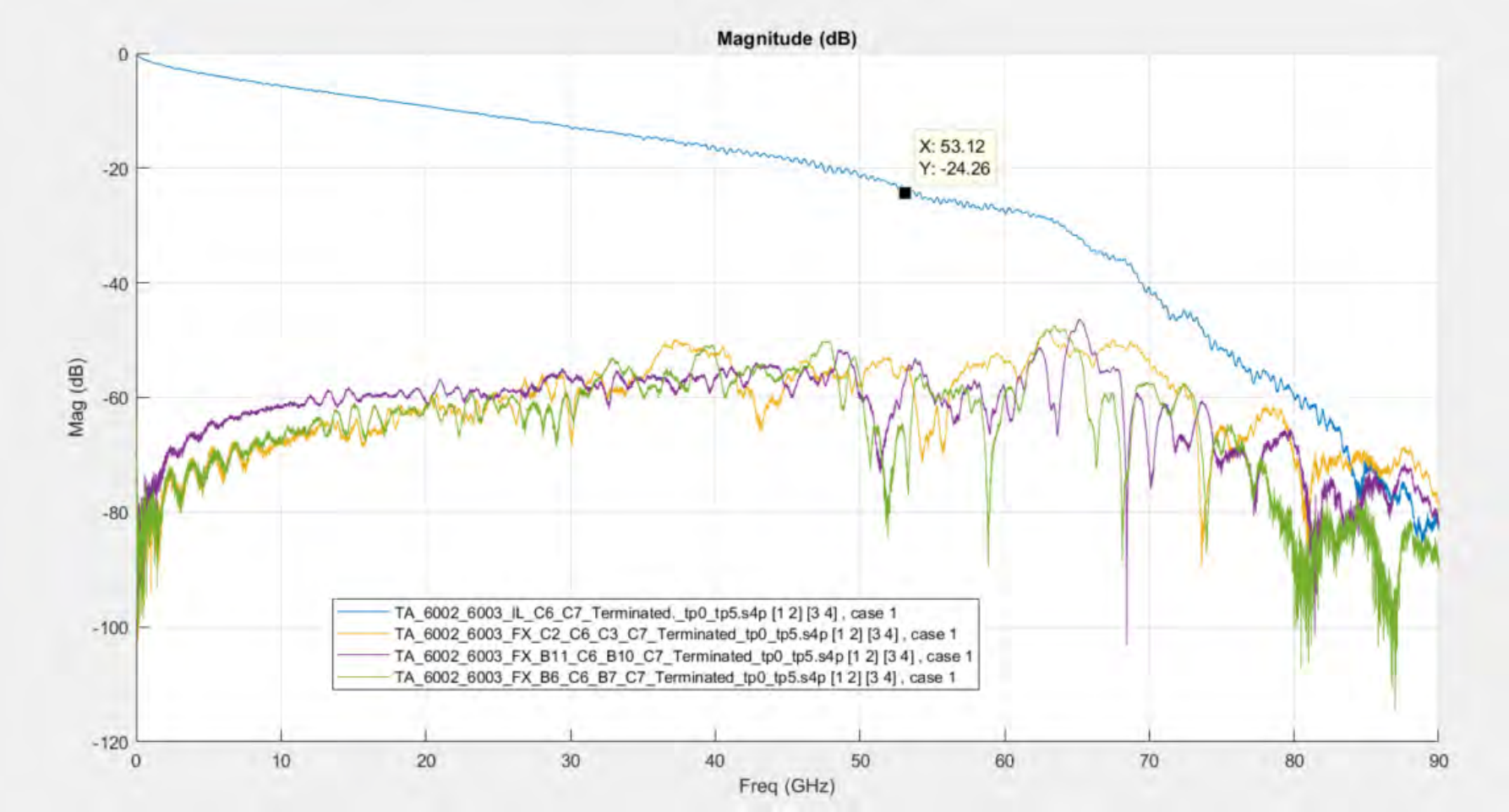
TP0

TP5

Chip to Chip board host hardware was not available at publication time
The above test board hardware is being used in laboratory 200 Gb/s studies

IL and Crosstalk (TP0/TP5 channel)

24.3 dB @ 53.125 GHz



COM 3.8beta example (w/ crosstalk)

FOR TEST BOARD WIRED TO TEST CHIP ATTACH

Table 93A-1 parameters			2
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ; 0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[.13 .15 .14; .13 .15 .14]	nH	[TX RX]
C_b	[.3e-4 .3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.408	V	
A_fe	0.408	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.2]		[min:step:max]
c(-3)	[-0.1:0.02: 0]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.3		
b_min(1)	-0.85		
b_min(2..N_b)	-0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-8:1:0]		[min:step:max]
f_HP_PZ	1.0625	GHz	
param.RC_Start	42500000000	HZ	
param.RC_end	79687500000	HZ	
Butterworth	0		logical
Raised_Cosine	1		logical

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\200G_C2C_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 2 3 4]	logical
RUNTAG	R200_eval	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	3.29E-03	ns
FORCE_TR	1	logical
Local Search	2	
SAVE_CONFIG2MAT	0	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	0	UI
Z_t	[45 50]	ohm
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-09	V^2/GHz
SNR_TX	34	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 8.4e-4 1.1e-4]	2.75 dB /in at 56G
package_tl_tau	6.14E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 6.44084e-4 3.6036e-05]	1.5 dbpi at 56G
board_tl_tau	0.00579	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	40	mm
z_bp (NEXT)	40	mm
z_bp (FEXT)	40	mm
z_bp (RX)	40	mm
C_0	[0.2e-4]	nF
C_1	[0.1e-4]	nF
Include PCB	0	**logical**
Floating Tap Control		
N_bg	4	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.2	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.676	*Fb
f_f	0.676	*Fb
f_n	0.676	*Fb
f_2	79.688	GHz
A_ft	0.600	V
A_nt	**0.600**	V

COM results

TP0 TO TP5 EXAMPLE

- Channel ERL
  - ERL for Z_t 45 Ω : 13.1 dB
  - ERL for Z_t 50 Ω : 12.2 dB
- Package 1 (12 mm)
  - COM : 4.34 dB
- Package 2 (31 mm)
  - COM : 3.57 dB

Summary

- 14 dB (@ 53 GHz) C2C test board channel measurements provided
- 24.3 dB (@ 53 GHz) C2C tp0-tp5 emulated channel provided
- Consider COM results and configuration just a WIP
- Hardware exists for these channels and will like improve over time
- Several usage models are possible with these channels

Thank You!