Baseline proposals for 800 GbE RS/MII, Extender/XS, Time Sync and PMA, using 100G/lane signaling

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Introduction

The IEEE 802.3df TF has already adopted the following AUI and PMD baselines for 800GbE using 100G/lane signaling:

- 800GAUI-8 C2C and C2M (lusted_3df_01a_220315)
- 800GBASE-CR8/KR8 PMDs (lusted_3df_01a_220315)
- 800GBASE-VR8/SR8 PMDs (murty_3df_01a_220315)
- 800GBASE-DR8/DR8-2 PMDs (welch_3df_01a_220222)

Introduction

This presentation will propose the following logic baselines in support of the adopted AUI and PMD baselines for 800GbE using 100G/lane signaling:

- RS/MII
- MII Extender/XS
- Time Sync
- PMA

An earlier version of this presentation was reviewed at the 802.3df logic ad-hoc call on 23 June 2022, and there was strong consensus for all four proposed baselines:

- https://www.ieee802.org/3/df/public/adhoc/logic/22_0623/minutes.pdf

Adopted logic architecture

A logic architecture baseline was adopted during the 802.3df Task Force meeting in May 2022, based on the following presentation:

- gustlin_3df_01a_220517

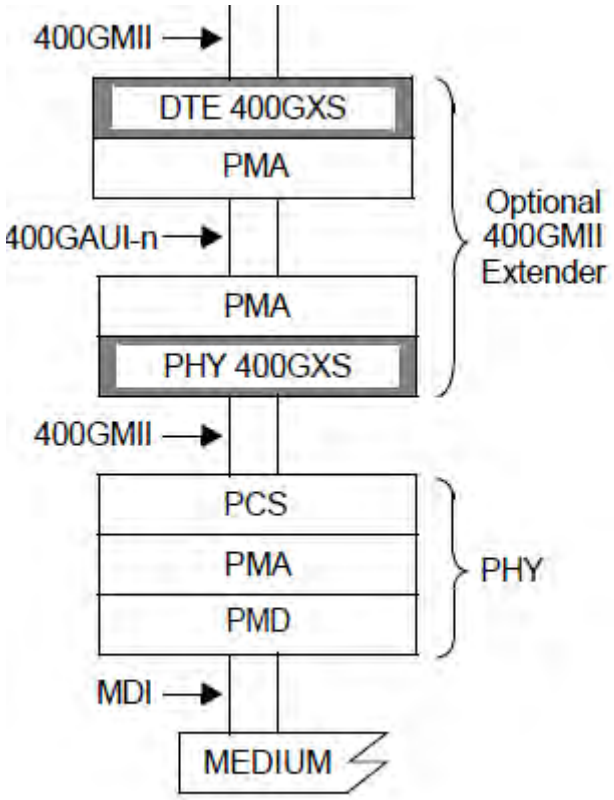
The baselines in this presentation are all compatible with the adopted logic architecture, for 800GbE interfaces using 100G/lane signaling.

RS/MII

- The RS/MII was changed to be a “logical” interface (i.e. no electrical specifications were defined) as part of the 802.3ba (40G/s, 100Gb/s) project.
- This approach was carried forward for 200GbE and 400GbE in the 802.3bs project.
- Propose that the same approach is used for 800GbE , and that the RS/MII is based on “*IEEE 802.3-2022, Clause 117 - Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII)”*, with the following changes:
  - ❑ The 800GMII supports a speed of 800 Gb/s
  - ❑ The 800GMII does not support EEE or Low Power Idle (LPI) signaling

MII Extender / Extender Sublayer (XS)

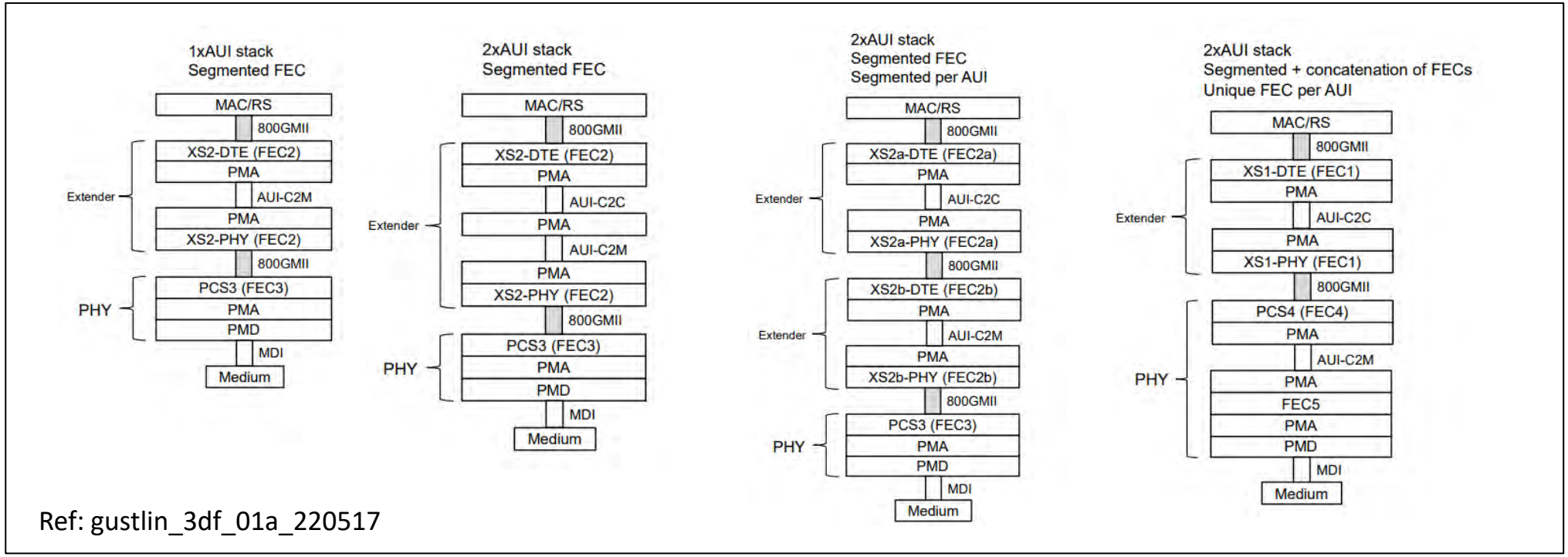
- The concept of an MII Extender (and associated extender sublayers) was first introduced in the 802.3bs (200GbE and 400GbE) project
- The purpose of the MII Extender is to extend the logical MII over an optional physically instantiated AUI, to allow different implementations and/or future PHYs that may require changing FEC (e.g. baseline_3bs_0715)
- The MII Extender comprises two sublayers, the “DTE XS” and the “PHY XS”. The “DTE XS” is functionally equivalent to the PCS, whereas the “PHY XS” is an inverted PCS.
- As an example, a MII Extender is used to support one or more optional AUIs with the 400GBASE-ZR PHY defined in 802.3cw.



Ref: 802.3-2022 Clause 118

MII Extender / Extender Sublayer (XS) for 800GbE

- The concept of an MII Extender was also adopted as part of the logic architecture baseline for 802.3df (gustlin_3df_01a_220517) .
- The primary reason for adopting an MII Extender was to allow the possibility of different FECs for the AUI and the PMD. Some Examples below:



Ref: gustlin_3df_01a_220517

MII Extender / Extender Sublayer (XS) for 800GbE

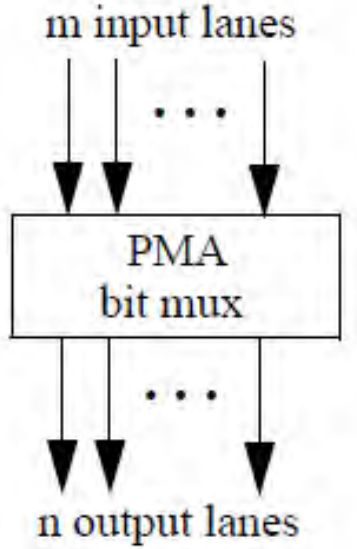
- Propose that the MII Extender for 800GbE using 100G/lane signaling, is based on *“IEE 802.3-2022 Clause 118 - 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)”*, with the following changes:
  - ❑ The 800GMII Extender and the 800GXS support a speed of 800Gb/s
  - ❑ The 800GMII Extender and the 800GXS reference the associated 800GbE PCS (baseline not yet adopted)

Time Synchronization Protocols

- Ethernet support for time synchronization protocols is defined in IEEE 802.3-2022 Clause 90 “Ethernet support for time synchronization protocols” and in P802.3cx informative Annex 90A “Timestamping accuracy considerations”
- Propose that 90.1 is amended as follows to support 800GMII (new text in blue font and underlined):
  - The TSSI is defined for the full-duplex mode of operation only. It supports MAC operation at various data rates. The MII (Clause 22), GMII (Clause 35), XGMII (Clause 46), 25GMII (Clause 106), XLGMII(Clause 81), CGMII (Clause 81), 50GMII (Clause 132), 200GMII (Clause 117), and 400GMII (Clause 117), and 800GMII (Clause TBD) specifications are all compatible with the generic Reconciliation Sublayer (gRS) defined in 90.5.
- Propose that “Table 90A-1 - Magnitude of potential timestamp accuracy impairments” in Annex 90A is amended to include the 800Gb/s Ethernet Rate.
- IEEE P802.3cx is expected to move to standards association balloting soon. Any relevant changes made to Clause 90 and Annex 90A prior to completion of the 802.3cx project will be accommodated in the 802.3df draft standard.

PMA

- The concept of a “bit muxing” PMA was first adopted in 802.3ba (40GbE and 100GbE) and carried over to 802.3bs (200GbE and 400GbE)
- The PMA accepts m input lanes, where each lane comprises of a bit mux of some number of PCS lanes.
- The PMA first bit demuxes each individual input lane into it’s constituent PCS lanes, and then bit muxes the PCS lanes from all of the input lanes (order not specified) onto the n output lanes.
- The PMA is also responsible for PAM4 encoding and decoding of input and output lanes if required.



Ref: 802.3-2022 Clause 120

PMA for 800GbE

- The 802.3df Task Force has yet to adopt a PCS baseline for 800GbE using 100G/lane signaling.
- There are (at least) two different PCS proposals under consideration, each with a different number of PCS lanes (but all currently assuming a bit muxing PMA).
- Propose that the PMA for 800GbE using 100G/lane signaling, is based on *"IEEE 802.3-2022 Clause 120 - Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R",* but with the number of PCS lanes left as "TBD" and with the following changes:
  - ❑ The PMA supports an aggregate speed of 800Gb/s

Thank You!