Updates on Concatenated FEC Proposal for 200G/Lane PMD

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Goal of the presentation

In this presentation we review the complexity of concatenated FEC scheme that works in conjunction with the standard KP FEC in the host. The proposed concatenated FEC is a simple soft decision FEC scheme that sits in the DSP SerDes inside the optical module.

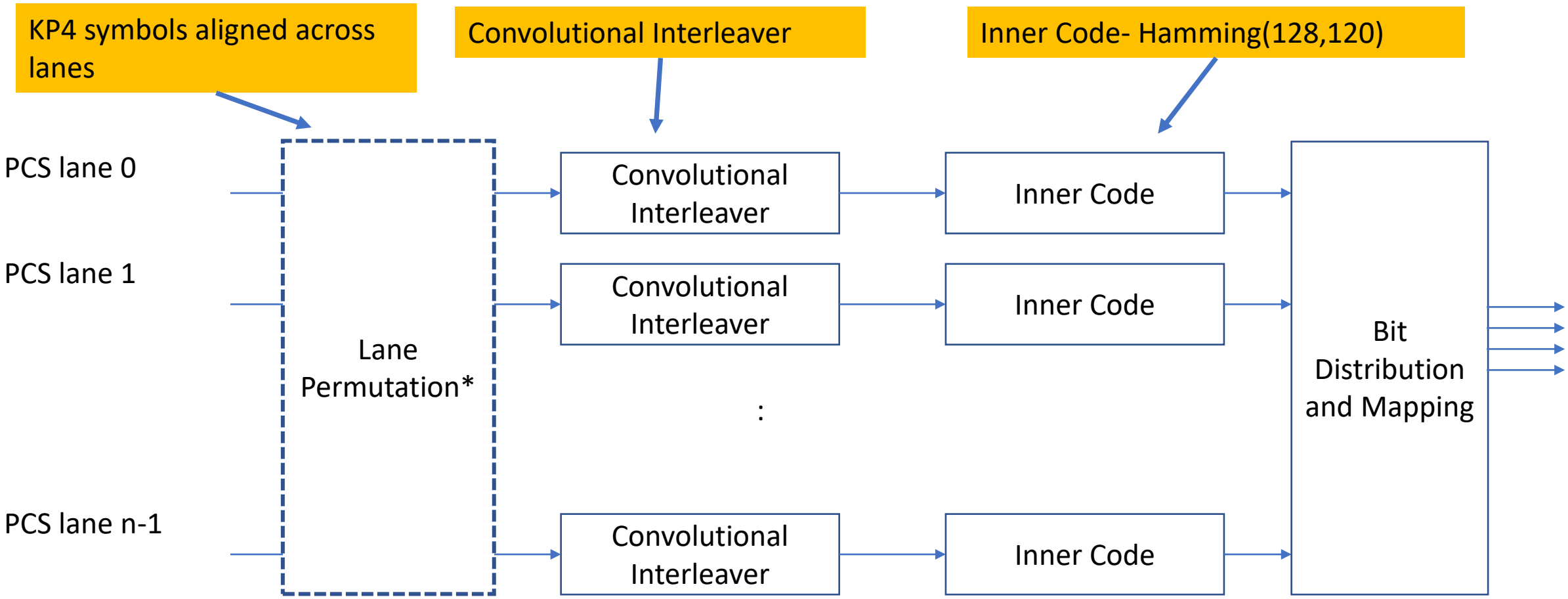
This scheme will provide a coding boost to the overall concatenated FEC scheme and will enable the deployment of 200G/Lane Optical PMD subsystem.

Various FEC Proposals : Baseline Assumptions

- KP4 FEC – RS(544,514) : Pre-dominantly used in 100G/lane → extended to 800G ETC mode
- RS(576,514) – Slight better flavor of KP4 FEC but with more complexity – proposed for 200G electrical channels
- KP4 + Hamming (128,120) – Concatenated FEC candidate – works in conjunction with Host KP4 FEC

FEC Type	Baud Rate	Pre-FEC BER threshold	Net Coding gain	Comments
RS(544,514)	PAM4: 106.25G	2.2E-4	7dB	* Leverages existing KP4 FEC, exists in switches, PHY today
RS(576,514)	PAM4:112.5G	1.1E-3	8dB	* Hard decision FEC
RS(544,514)+ Hamming (128,120)	PAM4:113.3G	4.85E-3	9.5dB	* Enhanced KP4 FEC with Soft decision Concatenated FEC proposal for 200G/lane

Generic Concatenated FEC Architecture

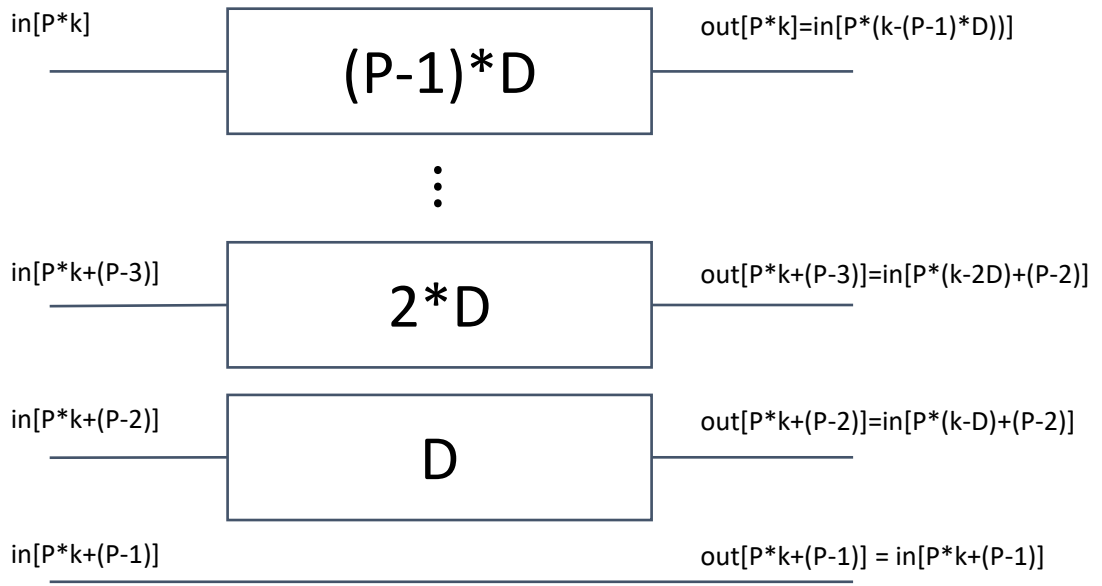


- Lane Permutation block - it may be present for certain PMD types only

Parametrized view of Per-lane Convolutional Interleaver

- Convolutional interleaver is defined per PCS lane
- Parameters for the per-lane convolutional interleaver
  - W: Number of KP4 RS codewords in each “word”
  - P: Number of sublanes of interleaver
  - D: Number of “word” delays
  - k : Time index
  - in[k]: Input “word” at time index k
  - out[k]: Output “word” at time index k

W-symbol words at interleaver input are round-robin distributed to P sub-lanes



W-symbol words from P sub-lanes are round-robin multiplexed to interleaver output

Convolutional Interleaver + Hamming (128,120) Latency for 200G per Lane PMD

Client Type	Parameters for Interleaver	FEC	Decoder Input BER	Latency
400GBASE-R (Clause 119)	W=2 P=6 D=6	KP4 + Hamming (128,120)	4.85E-3	~140ns
200GBASE-R*	W =2 P =6 D =6			~140ns
800G-PCS assuming ETC Type	W =4 P =6 D =6			~55ns
800G –PCS assuming speed up version of CL-119	W =2 P= 6 D= 6			~70ns

* For 200G breakout application – By reducing the inter-leaver depth, latency can be optimized to ~140ns without taking a substantial hit on NCG. The NCG penalty will be 0.25dB.

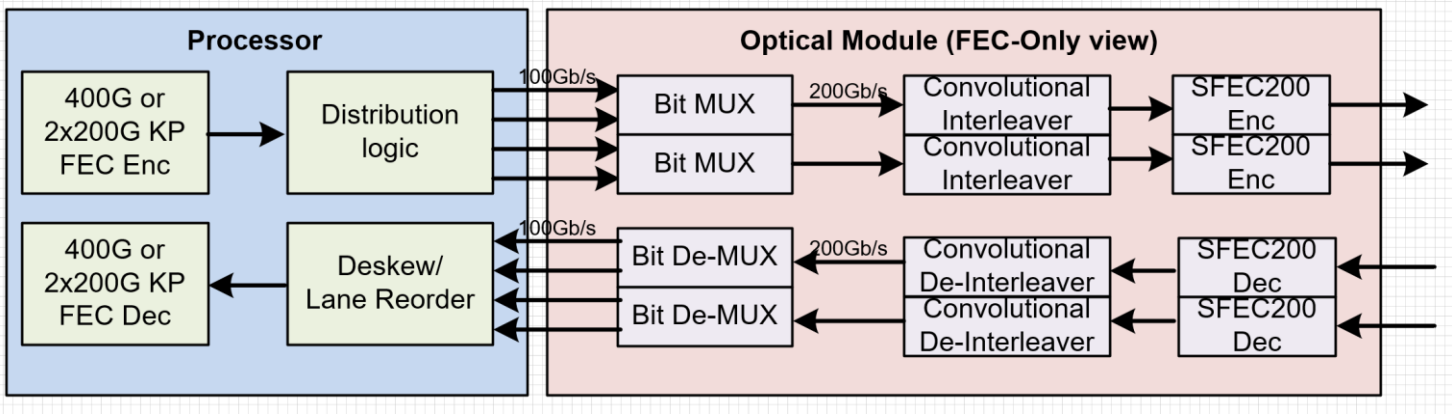
Soft Decision FEC implementation with FFE + DFE or FFE + MLSD type Equalizer

- 200G Optical PMD sub system needs stronger equalization than 100G/ Lane Optical PMD.
- Equalization may come in the form of FFE + MLSD type equalizer as it provides additional benefits like CD compensation.
- Soft decision decoding in conjunction with MLSD type of equalizer is NOT a new concept.
- Prior work in various read channel applications has already demonstrated the usage of Low complexity SOVA (soft in Viterbi out) decoder with MLSD type equalizer
- Here are some of the references to such implementation:
  - *A Concatenated Coding Technique for Partial Response Channels, Hideki Sawaguchi, Member, IEEE, Seiichi Mita.*
  - *List Viterbi Decoding with Continuous Error Detection for Magnetic Recording", Dragan Petrović, Borivoje Nikolić, Kannan Ramchandranm{dragan, kannanr,bora}@eecs.Berkeley.edu*

- For some more ideas on exploiting symmetries when implement Viterbi-stye decoders, please see:

https://www.ieee802.org/3/bj/public/sep12/farhoodfar_3bj_01_0912.pdf

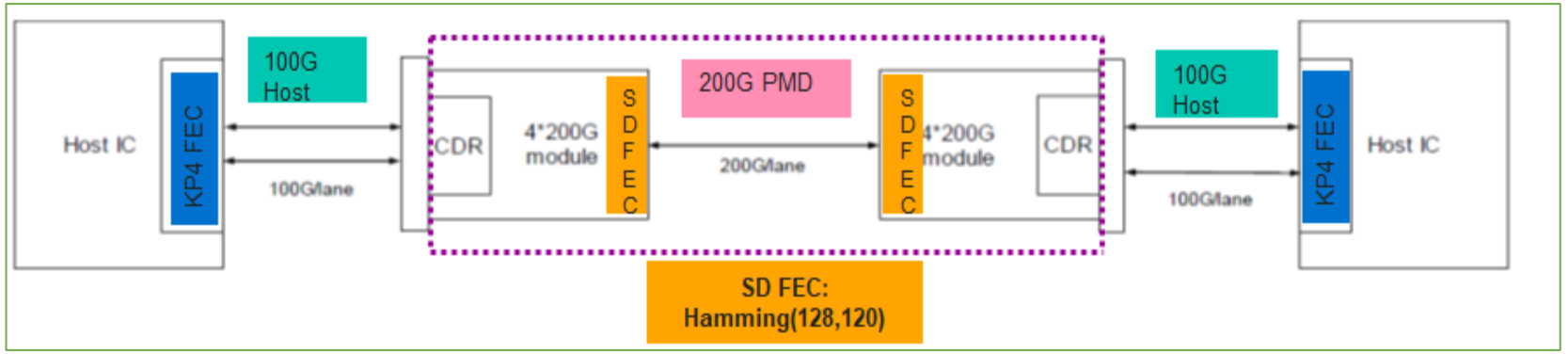
Soft Decision FEC implementation example with 200G Optical PMD



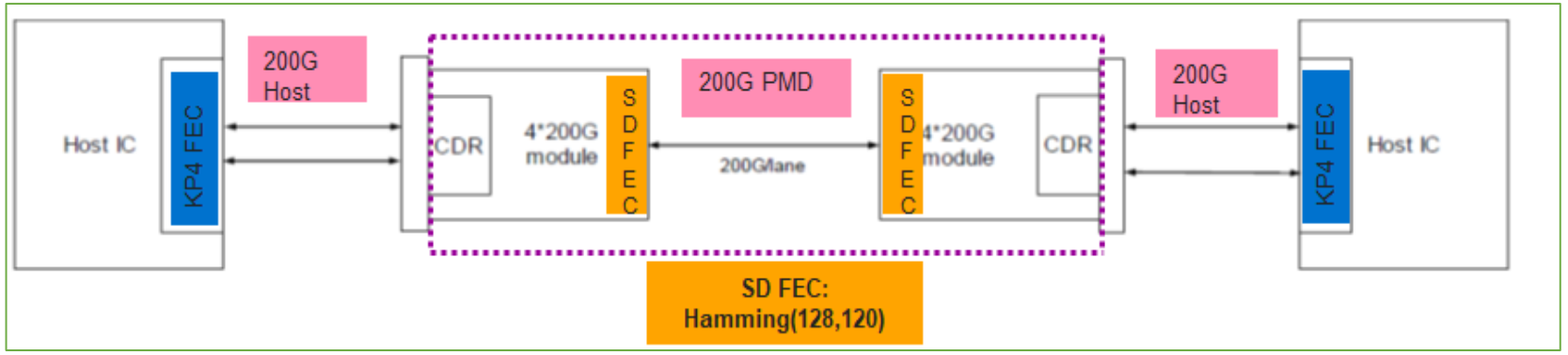
Attribute	Summary	Additional Notes
C2M Interface	For 100G – use existing C2M Spec	* For 200G – C2M spec in early development stage but same concept can be extended to 200G C2M to leverage KP FEC on host
Outer Code	802.3ck based KP FEC with bit multiplexing	Simply bit multiplex 2x100G/Lane into 1x200G/Lane. R_{outer}=514/544 For 200G – No need for Bit-muxing and demuxing
Inner Code	SDFEC : Hamming(128,120)	R_{inner}=120/128
BER threshold	4.85E-3	KP limit is 2.2E-4.
Net-Coding-Gain	9.5dB	KP NCG=7.0dB. Delta improvement over KP FEC=2.5dB
Implementation with DFE or MLSD	SOVA style implementation	Complexity is NOT hard. Prior work has been done in read channel domain.
SDFEC Power consumption	~100mW per 200G Lane	* Assumption of Process node – N5

Concatenated FEC scheme : Keeping it Backward compatible & Forward looking

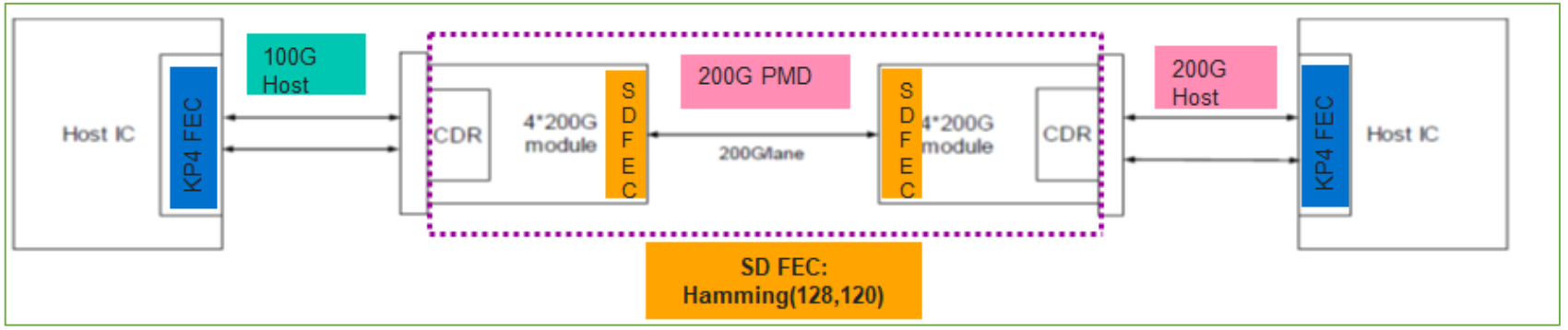
1st Gen deployment:
- 100G AUI Host + 200G/Lambda Optics



2nd Gen deployment: Leverage KP FEC on host
- 200G AUI Host + 200G/Lambda Optics



Solving the backward compatibility & keeping it forward compatibility
- 100 AUI Host + 200G/Lambda Optics + 200G AUI host



Summary

- Simple concatenated soft FEC like hamming (128,120) can provide more than enough coding boost to enable the deployment of 200G Optical PMD.

- Leveraging the existing KP4 FEC for 200G AUI will benefit the industry and will ease the backward compatibility issues.

- Overhead for KP4 + SFEC is similar to stronger Hard coded FEC like RS(576,514) : 113.3Gbaud Vs 112.5 Gbaud while the concatenated scheme provide a better overall coding gain.

Thanks !