

A Balanced Approach to PCB and Package Losses

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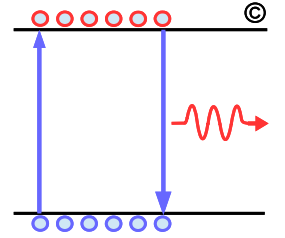
IEEE 802.3df Task Force Meeting

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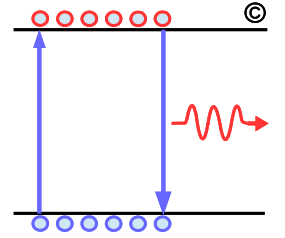
Contributors

- ❑ Habib Hichri – Ajinomoto
- ❑ Liav Ben Artsi – Marvell
- ❑ Richard Mellitz – Samtec
- ❑ Brian Nelson – Sanmina.

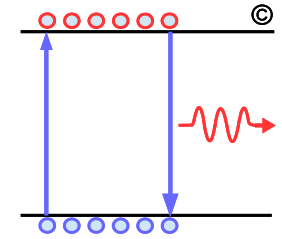


Overview

- ❑ Balancing PCB and package losses
- ❑ Advance package losses for several geometries
- ❑ Large radix switch breakout challenges
- ❑ Advance PCB loss per inch
- ❑ Summary.



Balancing 200G PCB and Package Losses



❑ Unless we can balance the PCB and package losses

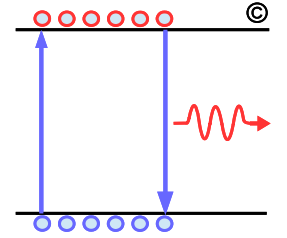
- We will define something that can't be manufactured
- Or the loss is so high that some applications are not viable and/or the power is too high

❑ Some of the early 200G package and PCB losses reported are too optimistic at least for large complex packages or on high-density PCB boards

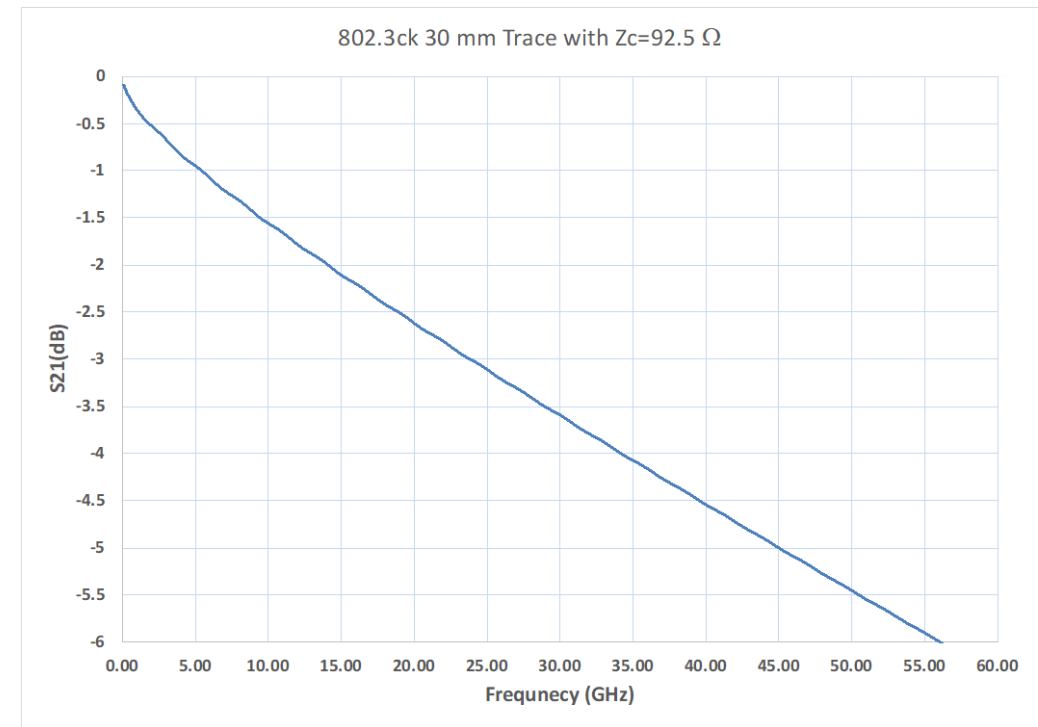
- [mli 3df 01a 220316](#) proposes to use skip ABF layers to allow using wider traces to lower loss/mm to ~ 0.14 dB/mm @53 GHz (loss include transition via/BGA)
- [benartsi 3df 01b 2207](#) uses best ABF conventional 27-45-27 μm construction and reports trace loss of 0.31 dB/mm @53 GHz (loss include transition via/BGA)
 - Benartsi loss expected to be lower ~ 0.22 dB/mm after accounting for improved surface roughness
- [diminico 3df 02a 220602](#) based on Amphenol TCS data show 1.3 dB/in loss @53 GHz for 6.3 mils wide stripline trace on Doosan DJN3+

❑ How low a package and PCB losses are practical, and how high a loss the application becomes impractical?

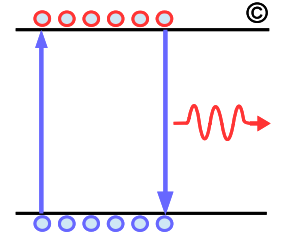
What was the Baseline CK Package Loss



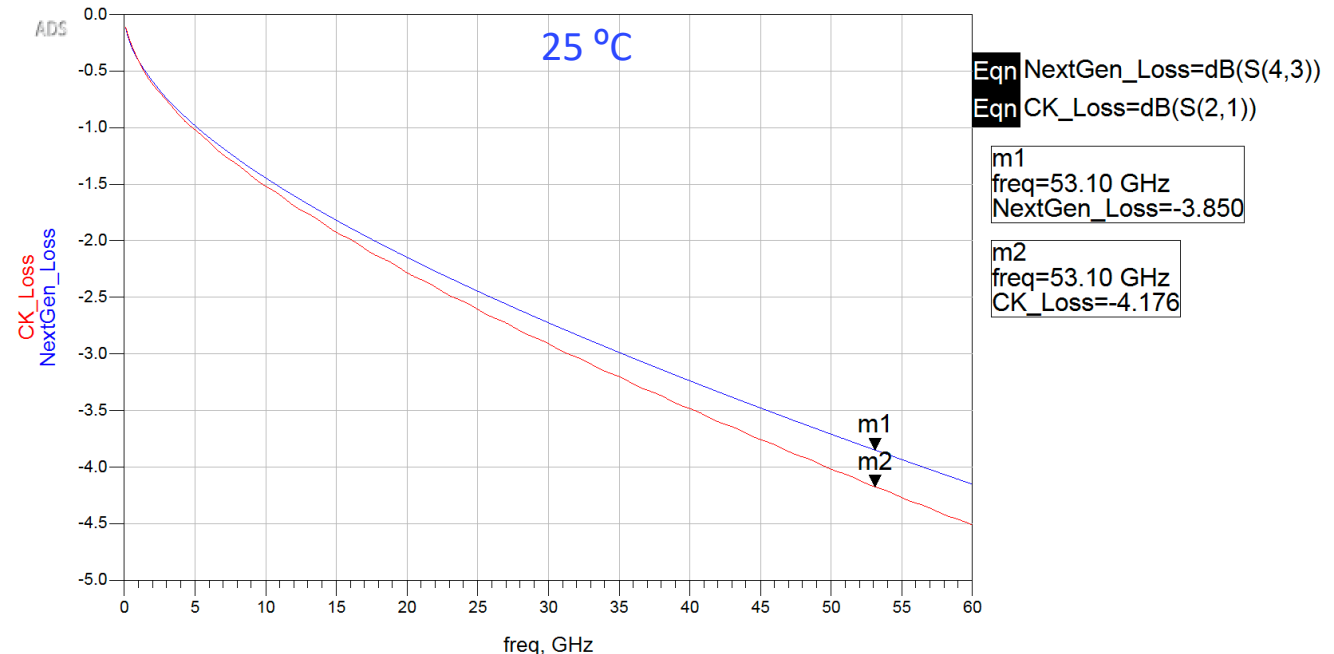
- ❑ **802.3ck package loss is ~ 4 dB @26.55 GHz for the two segments**
 - The main TL segment has a loss of 0.109 dB/mm
- ❑ **Did we assume too aggressive a package model in CK?**
 - For 2018/2019 4 dB package loss was very aggressive
 - To meet CK package loss on large ASICs requires using somewhat wider 38 μm striplines using 2018/2019 next Gen ABF films
 - Considering 256 and 512 we now have 100G/lanes switches in the marketplace that are compliant to CR, the package loss of these products can't be much higher than 4 dB.



Li Skip Layer Package Loss

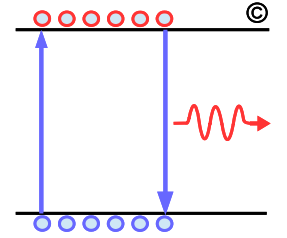


- Trace width was not provided in [mli 3df 01a 220316](#) but it is estimated to be 52 μm wide traces
 - Use the same Hurray surface roughness model that was previously matched best ABF film in 2018/2019 “CK_Loss”
 - Hurray surface roughness model was adjusted in ADS to match the measured loss for the above film and the loss is referred to CK loss model
 - Trace width was adjusted to meet 3.85 dB loss at 53.1 GHz for next Gen ABF film 0.128 dB/mm “NextGen_Loss”
 - To match MLI losses 52x15 μm striplines are used
 - Since MLI proposal to use Skip layer due to lack of thicker ABF films, now the largest supplier of ABF films Ajinomoto can supply films to construct packages with similar structures without Skip layers
 - The bigger issue with the ~52 μm wide traces or ~150 μm differential pairs are the breakout from a dense SerDes bumps map on a 512 lanes switch even with 9-2-9 package!

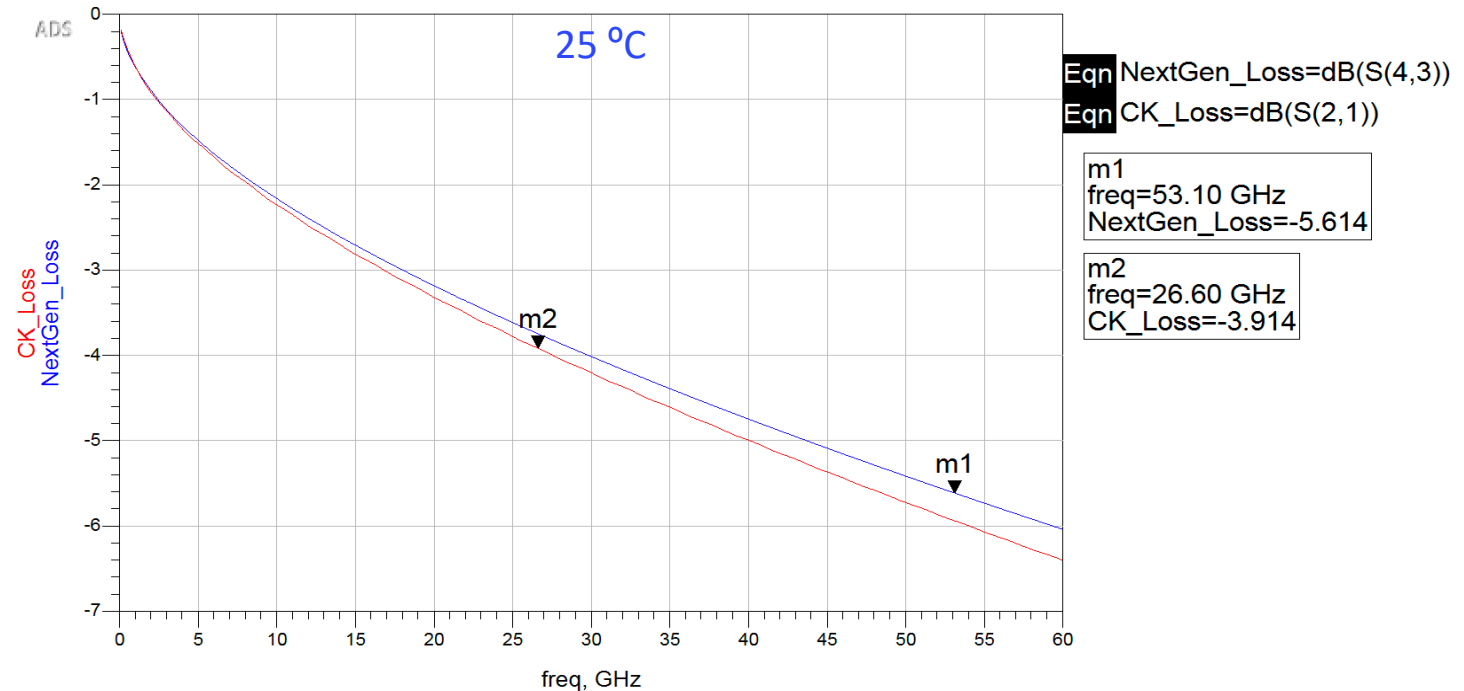


Loss Reported is only for the trace and does not include transition Via/BGA

CK and Next Gen Package Losses for Reduced Trace Width

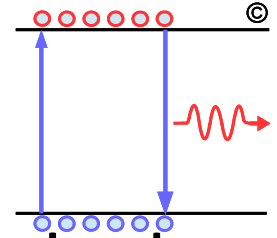


- Adjust trace width to 27 μm as suggested by [benartsi 3df 01b 2207](#)
 - Use the same Hurray surface roughness model that was previously matched best ABF film in 2018/2019
 - Reduced trace width may be required for some high radix switches implementations
 - Losses for 27 μm wide 92.5 Ω stripline traces
 - For best ABF film from 2018/2019 the CK 30 mm package trace loss is 3.94 dB or 0.13 dB/mm instead of assumed 0.109 dB/mm assumed loss @26.56 GHz
 - Next Gen 2022 ABF film the 30 mm package trace loss would be 5.6 dB or 0.19 dB/mm @53.1 GHz (6.75 dB or ~0.225 dB/mm 90°C).



Loss Reported is only for the trace and does not include transition Via/BGA

CK Package Loss vs Proposed 200G Package Losses



benartsi 3df 01b 2207 proposed 200G package trace loss is 0.31 dB/mm and on other hand mli 3df 01a 220316 package loss overly aggressive with 0.129 dB/mm

- Benartsi extracted package model parameters possibly has an error as the loss is greater than HFSS extracted loss
 - Updated Benartsi results expect to have lower loss after additional surface roughness's considered
- Even if CK package loss was too low for 2018/2019 circa, in DF need to be forward looking to what is feasible in 2025/2026!

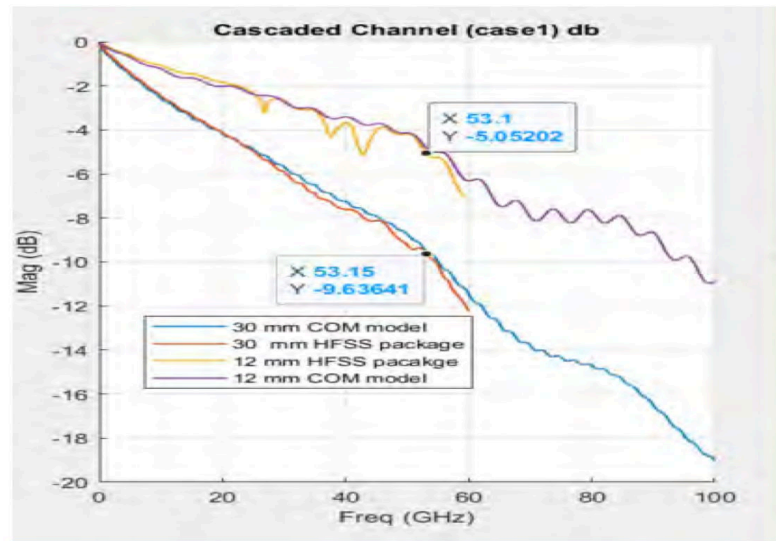
200G Package Parameters in Benartsi

Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0017423 0.000517778]	
package_tl_tau	6.42E-03	ns/mm
package_Z_c	[94 94 ; 76 76; 200 200; 70 70]	Ohm

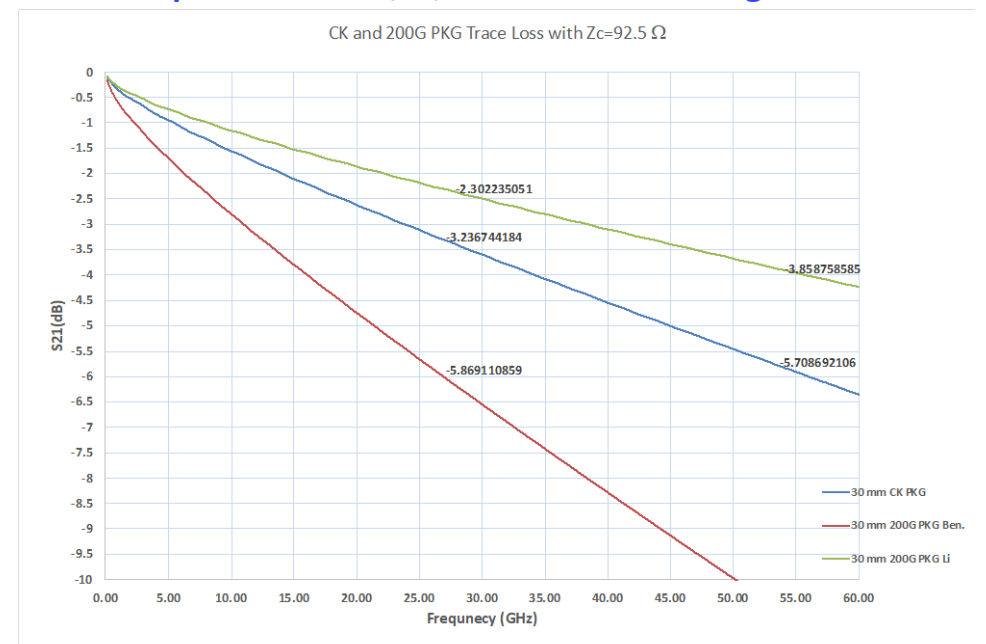
200G Package Parameters in Li

Parameter	112G Package T-Line Model Parameters	Proposed 224G Package T-Line Model Parameters
Z_p	30 mm	30 mm
γ_0	0 /mm	0 /mm
τ	6.141e-3 ns/mm	6.141e-3 ns/mm
a_1	9.909e-4 ns ^{1/2} /mm	8.9e-4 ns ^{1/2} /mm
a_2	2.772e-4 ns/mm	1.55e-4 ns/mm
Z_c	87.5 Ω	87.5 Ω
R_o	50 Ω	50 Ω
C_p	87 fF	40 fF

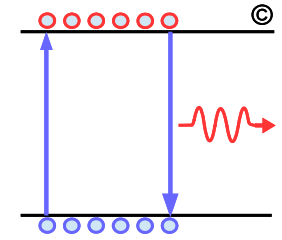
Benartsi HFSS Trace + PKG Extracted



Comparisons of CK, Li, and Benartsi Package Trace Losses

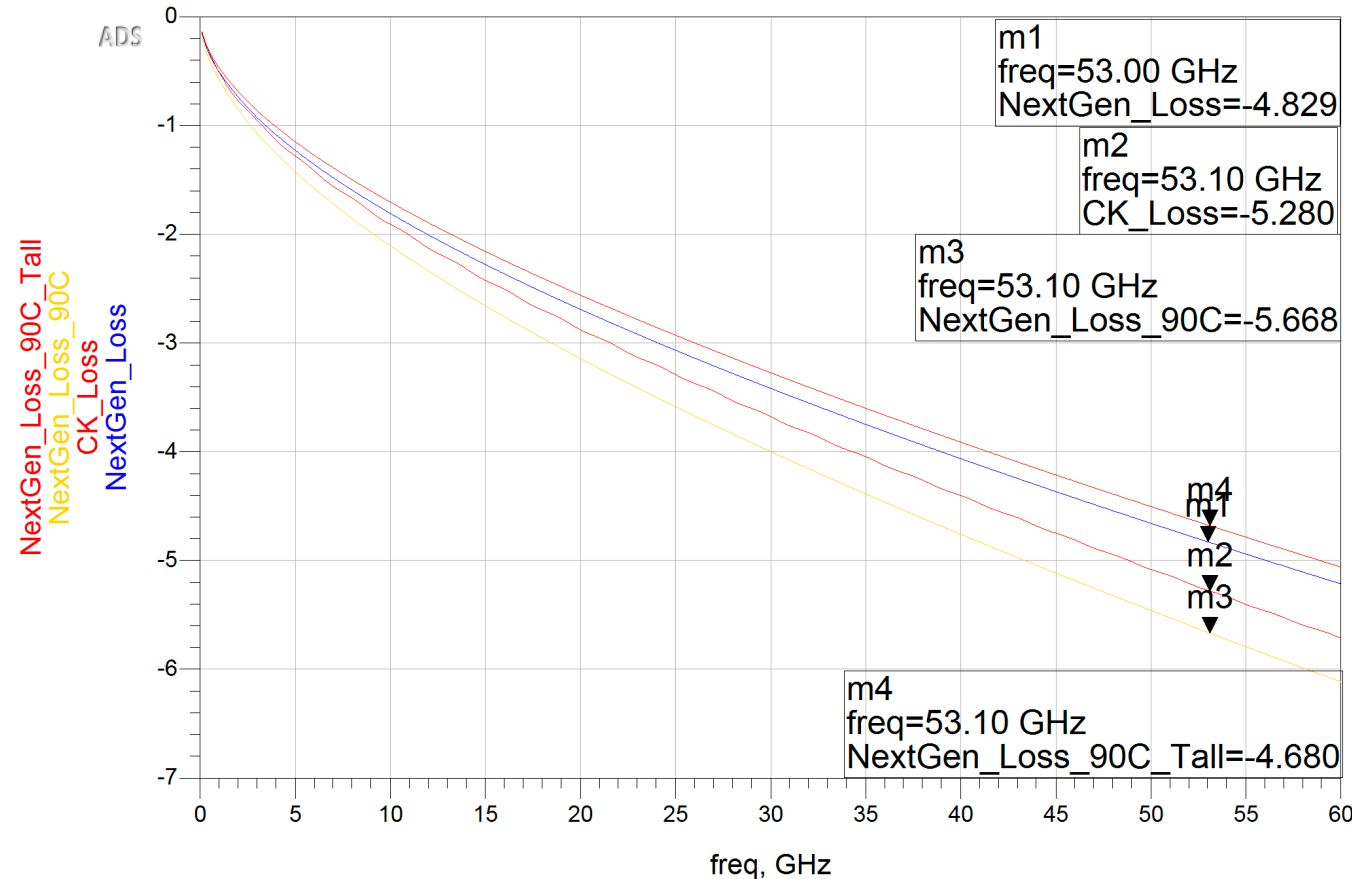


Is there a path to Lower Package Loss



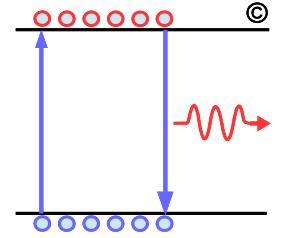
□ 30 mm CK package trace loss is ~3.25 dB@26.55 GHz as shown on previous page which was optimistic for the time

- To meet loss of 0.108 dB/mm @26.55 GHz it required to use the most advance ABF film in 2018/2019 having **38 μm** wide x 15 μm high 92.5 Ω stripline traces
- NextGen_Loss_90C_Tall uses 38x30 μm trace
 - Emerging package technology allow up to 50 μm thick traces
- The losses for next Gen 2018/2019 “CK_Loss” and 2022 ABF “NextGen_Loss” films are shown at 25 ° and 90 °C
 - 2018/2019 Next Gen ABF loss **0.171 dB/mm** (25 °C)
 - 2022 next Gen ABF loss **0.161 dB/mm** (25 °C)
 - 2022 next Gen ABF loss **0.189 dB/mm** (90 °C)
 - 2022 next Gen ABF loss **0.156 dB/mm** (90 °C) for tall 38x30 μm structure and the loss for this structure is similar to MLI skip layer 52 μm wide traces at 25°C).



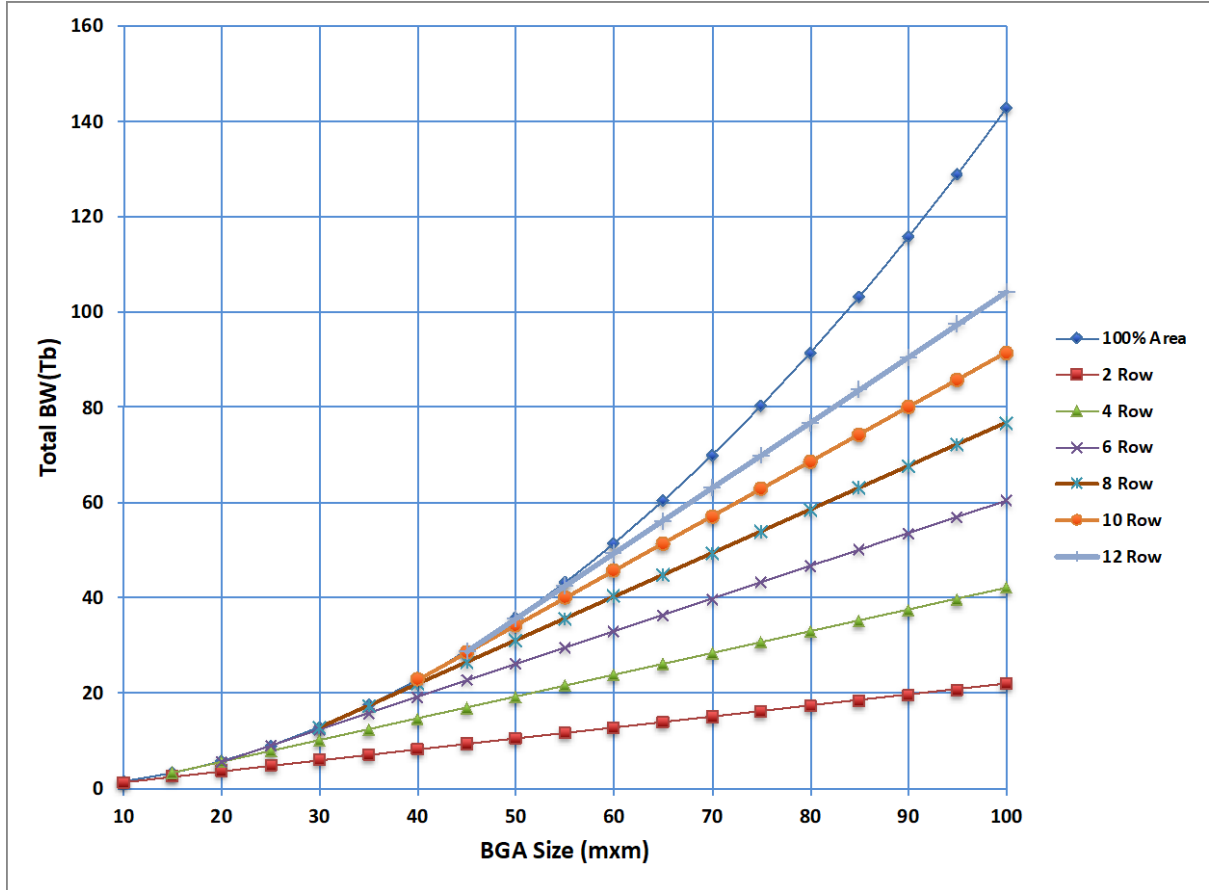
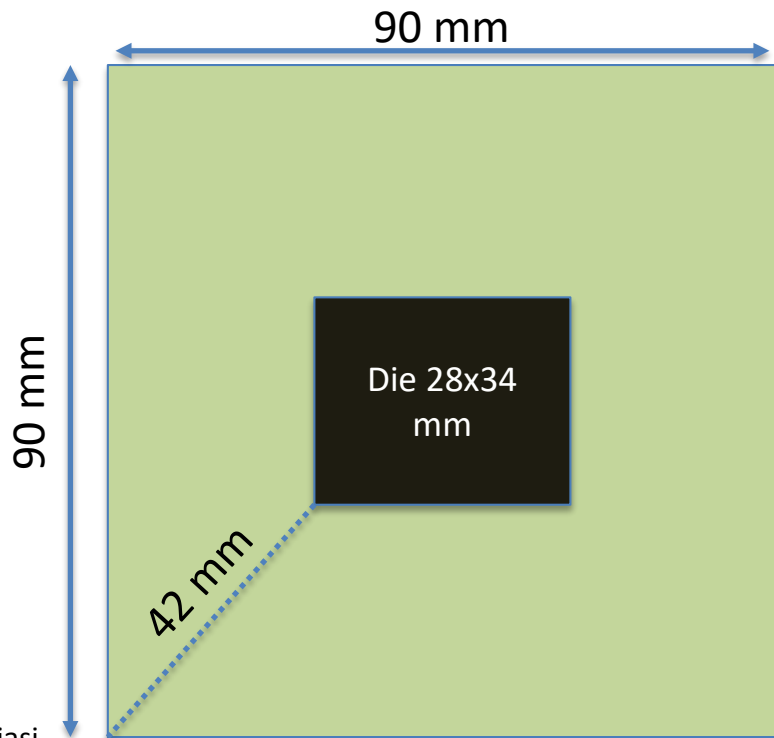
Loss Reported is only for the trace and does not include transition Via/BGA

Hypothetical 512x200G Switch



□ Likely will require 90x90 BGA

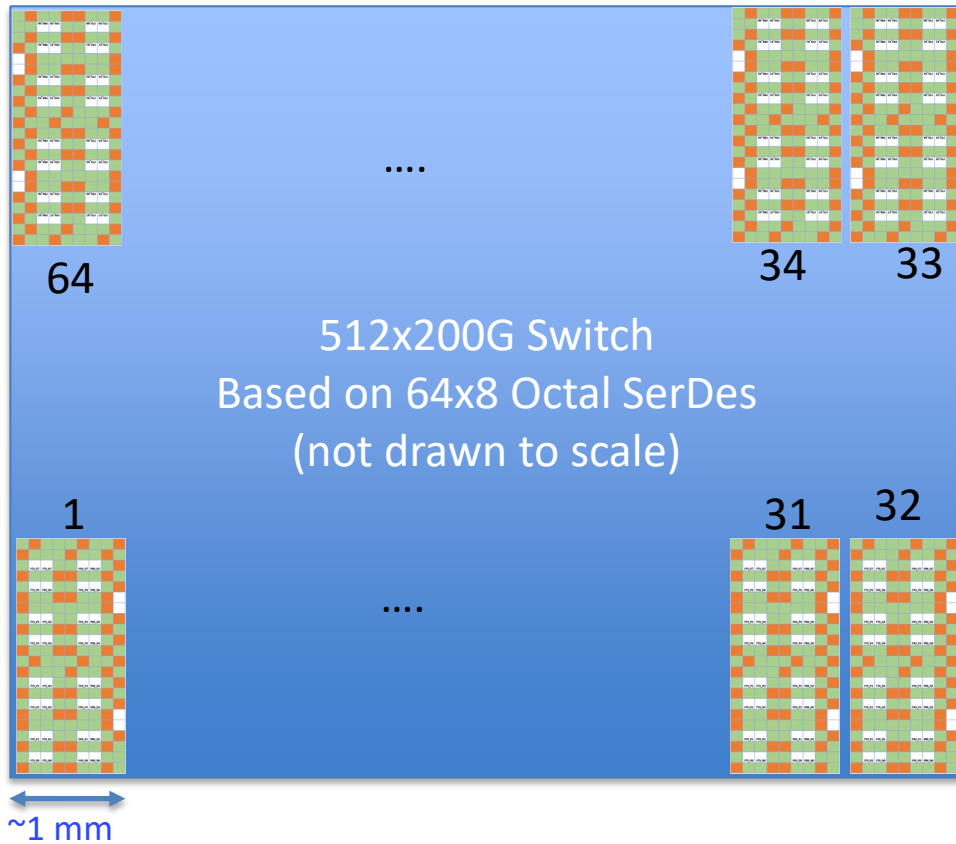
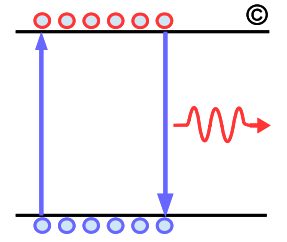
- Provides $\sqrt{2}$ for FEXT pairs
- Provides 2 balls separations for NEXT
- For the hypothetical switch with 28x34 mm die results in 42 mm long substrate trace!



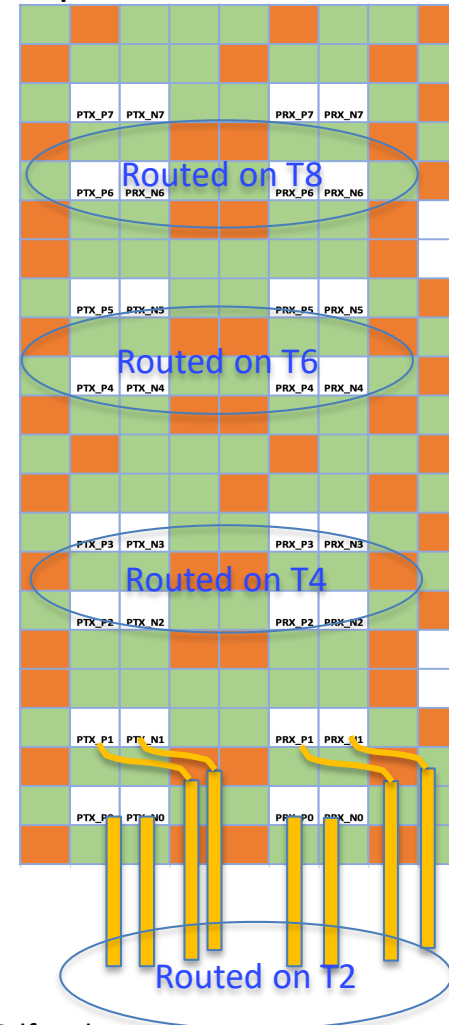
For the BGA ball grid assumed, see <https://opg.optica.org/oe/fulltext.cfm?uri=oe-23-3-2085&id=310831>

Hypothetical 512 Radix Switch Routing

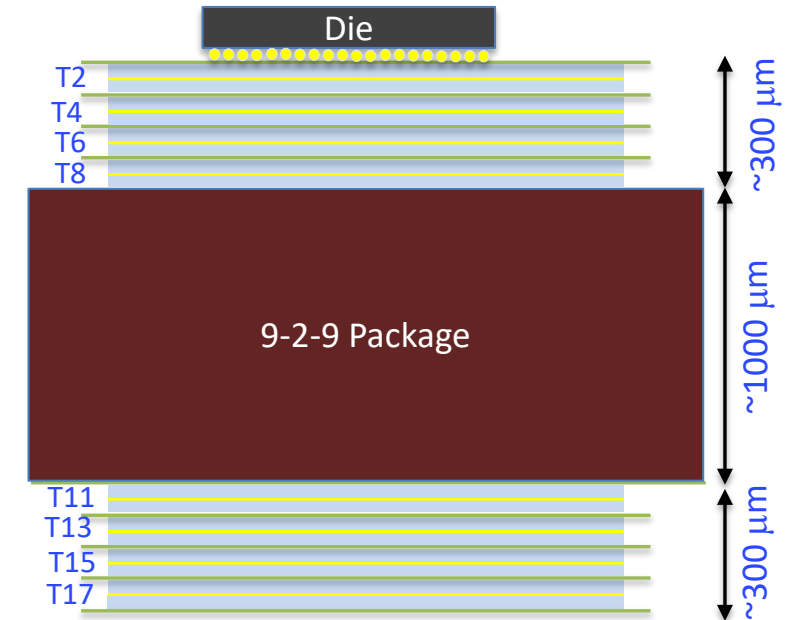
- 38 μm traces likely require 9-2-9 package and expected to be in volume by 2025/2026
 - 200G packages will also benefit from emerging thin cores (Cu-prepreg, resin coated Cu RCC, or glass interposer) then one may utilize layers T11-T17 for bump attachment!



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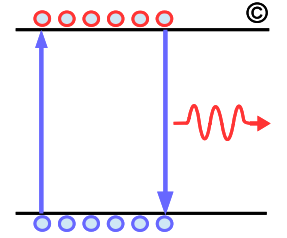


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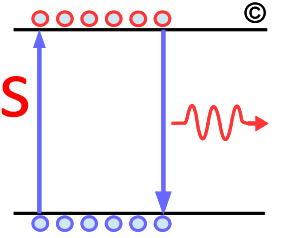
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What Should the Base Assumption be for 200G Package be?



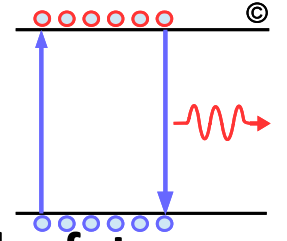
- ❑ Are we OK with [benartsi 3df 01b 2207](#) ~9.5 dB package loss assuming 27 μm wide trace with correct surface roughness the trace length will be ~40 mm instead of reported 30 mm
 - Leavening only 17 dB for ball-ball loss in case of 200G-KR/CR or consume half the budget in two packages
- ❑ Package to support 512 lanes of 200G with sufficiently low crosstalk likely will be ~90x90
 - A single monolithic die in 1 mm pitch BGA may have traces as long as 42 mm but can we even afford allocating ~12.5 dB to such a package
- ❑ Options to consider
 - Considering CK package trace width had to be at least 38 μm , should we consider similar trace width?
 - With advancement in the HDI features size and introduction of several coreless technology (Cu-prepreg, RCC, or glass interposer), should our 200G reference package have 1.2 mm core?
 - Getting ride of 1.2 mm PCB core also eliminate the need for ~280 μm large core vias
 - With the 1.2 mm core gone now all lower layer can also be utilized to connect to the bump
 - Should we consider chiplet to mitigate trace lengths, die yield, and allow increasing switch buffer?
 - Do we need some fundamental improvement in BGA manufacturing to allow supporting 0.65- or 0.8-mm pitch BGAs considering potential TM modes as shown by [mli 3df 01a 220316](#)?

Surface Roughness is a Major Contributing Factor in PCB Loss



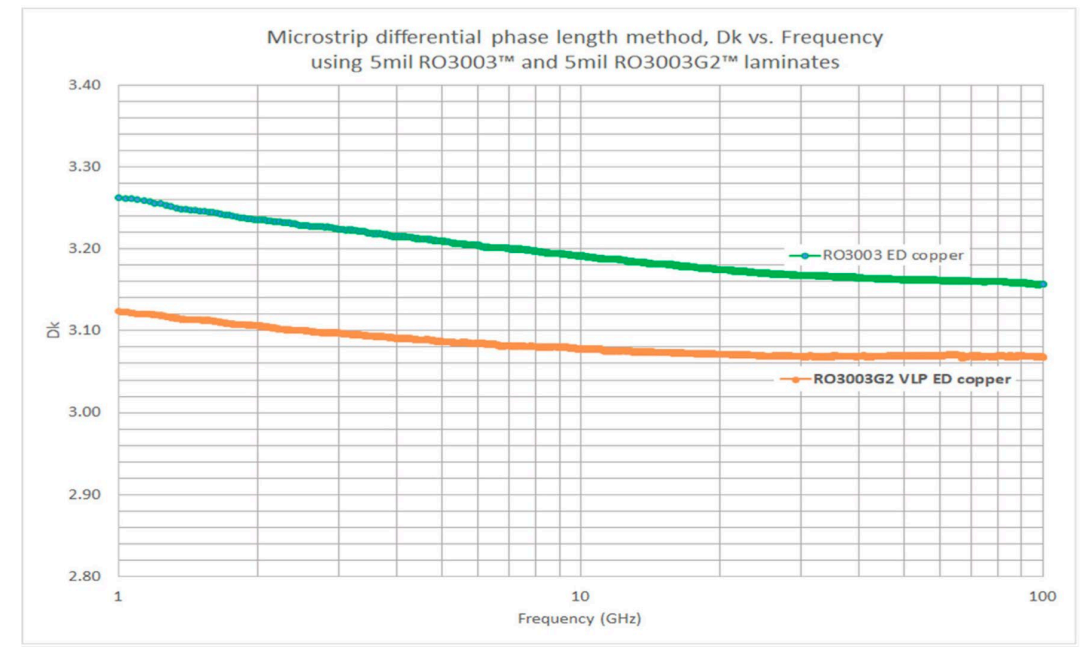
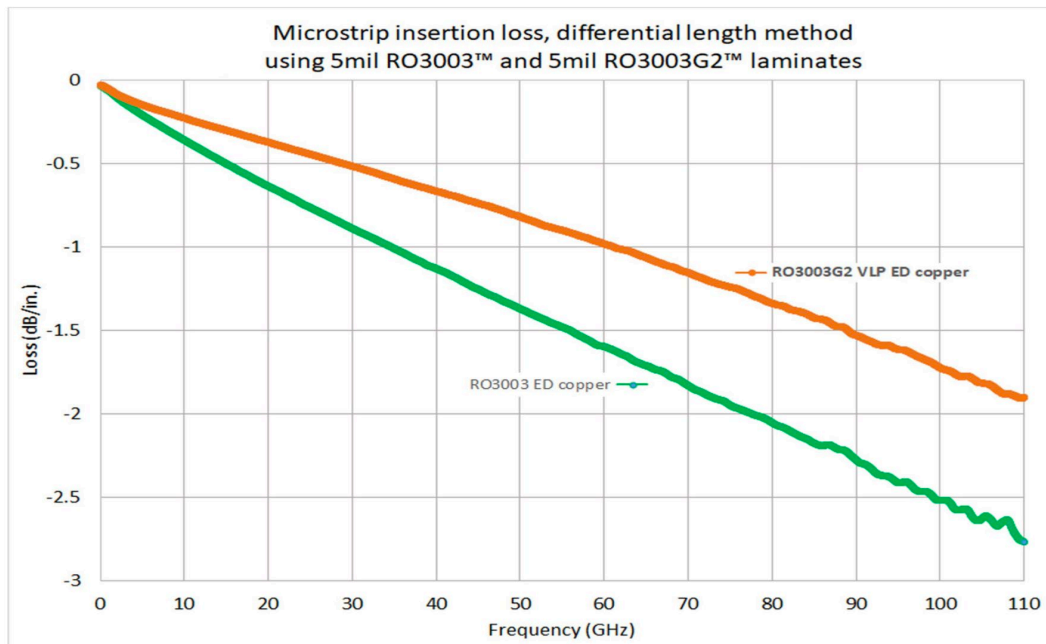
- ❑ **Rolled annealed (RA) copper offer the best surface roughness $R_a \sim 0.3 \mu\text{m}$ (RMS) and conductivity as you are using pure copper**
 - Rogers Corp is a major supplier of RA PTFE laminates generally not used for complex high-density PCB due to risk of delamination
 - High volume PCBs utilize electrodeposited Cu instead of RA Cu
- ❑ **Some of the PCB/Cu foils suppliers with advance electro-deposited (ED) foils are list below (the list is not exhaustive, and some PCB laminate maker have developed their own Cu foils):**
 - Rogers Corp offers high performance flat electrodeposited laminates on RO3003G2 with $R_a \sim 0.4 \mu\text{m}$ with R_z bonding side flat [Rogers Cu Foils](#)
 - Oak Mitsui Technology sampling SI-VSP advance foil $R_z(\text{bonding side}) \sim 0.5 \mu\text{m}$ [oak-mitsuitechnologies](#)
 - Furukawa offers HVLP2 foil FZ-WS with $R_z(\text{bonding side}) \sim 1.1 \mu\text{m}$ with HVLP3 under-development [furukawa.co.jp-foil](#)
 - Fukuda Meta Foil & Powder CF-T4X-SV foil has $R_z(\text{bonding side}) \sim 1.0 \mu\text{m}$ [fukuda-kyoto Foils](#)
 - Different manufacturers calls their advanced foils by different name and currently there is no IPC definition.

What is the Limit of Low Loss PCBs

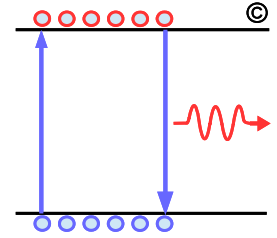


□ Rogers [RO3003G2](#) VLP ED copper can provide us the limit what might be possible in the future for some of the advanced non-PTFE based volume PCB materials

- The loss shown below is for ½ oz Cu ~13 mil wide microstrip
- Rogers internal PCB tool show a loss of 1.15 dB/in compared to measured loss of 0.85 dB/in @53 GHz
- 6 mills wide stripline would have a worst-case loss of 1.56 dB/in and including over-etch ~1.66 dB/in (assuming similar typical vs worst case one may measure the typical loss ~1.25 dB/in).



Estimated Worst Case Stripline Loss on Rogers 3003G2

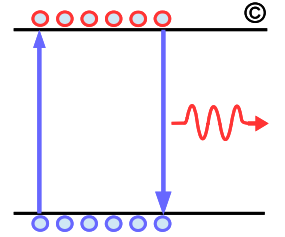


Using Rogers Hurray parameters and measured data from previous page stripline losses for 4.5, 6, and 7.5 mils on Rogers 3003G2 graphed below

- Any commercial high-volume PCB in foreseeable future expected to have higher losses
- The Oak Mitsui SI-VSP foil on an advance volume laminate may come close to RO3003G2
- Summary of the losses:
 - 2.05 dB/in for 4.5 mil wide stripline
 - 1.67 dB/in for 6 mils wide stripline
 - 1.43 dB/in for 7.5 mils wide stripline the loss is similar 6 mils wide RO3003G2 with rolled Cu
 - At 200G high density line cards may need to use 6 wide traces to lower the PCB losses
- [diminico 3df 02a 220602](#) based on Amphenol TCS data show 1.3 dB/in loss @53 GHz for 6.3 mils wide stripline trace on Doosan DJN3+ somewhat optimistic for 70°C operation.



Summary



- ❑ **Without significant advancement of PCB and package technology the conventional PCB channels may have limited practical use case and instead may need to consider CPC implementation [tracy 3df 01a 2207](#)**
 - The 200G IO and channels should be designed based on what will be feasible in 2025/2026 otherwise we may not meet some of our objectives and/or pay a very high premium on power
- ❑ **Package losses for two BGAs can consume half of KR/CR budget without package technology advancement**
 - [benartsi 3df 01b 2207](#) suggest using 27 μm traces in the package where the package loss will be 8+ dB
 - [mli 3df 01a 220316](#) uses skip layer where traces in package are $\sim 52 \mu\text{m}$ wide with 4 dB package loss but maybe too aggressive even for 2025/2026-time frame
 - To meet the CK package loss one had to use 38 μm wide traces and the recommendation is to use trace width at 200G
 - With availability of thicker ABF films one may even use wider or thicker traces without skip layer if bump breakout is feasible
 - Recommendation is to define the 200G package with thick core or coreless with trace loss of $\sim 0.16 \text{ dB/mm @}^\circ 90\text{C}$
 - Could give us the path to **6 dB package loss!**
- ❑ **200G 512 radix monolithic die switches that don't use chiplet likely will have 42 mm long traces**
 - Requiring every C2M/CR link to support 42 mm package trace is burdensome
 - The default package trace length should remain at 30 mm long
 - Otherwise need a mechanism to trade off the higher package loss with PCB/cable losses.
- ❑ **Need to be forward looking but pragmatic on the PCB trace loss**
 - Linecards constructed from advance emerging PCB laminates and copper foils the loss for 6 mils wide stripline at 70°C expected to be **1.65 dB/in.**