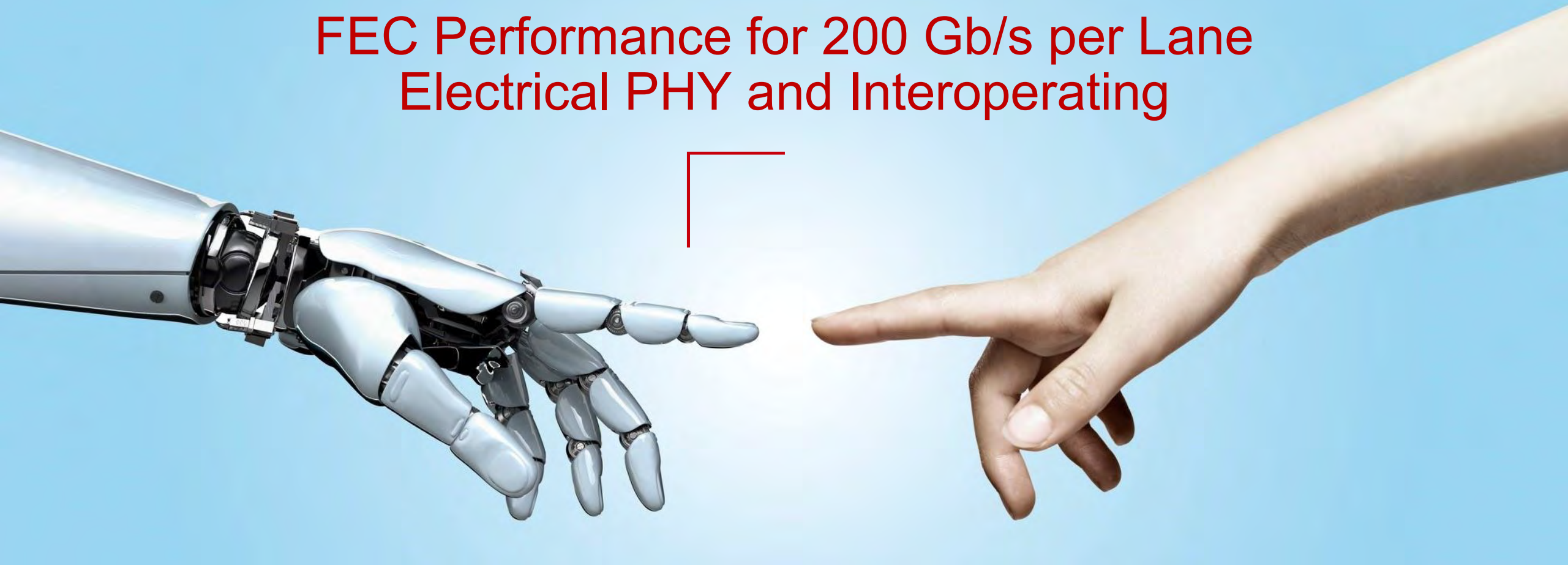
FEC Performance for 200 Gb/s per Lane Electrical PHY and Interoperating



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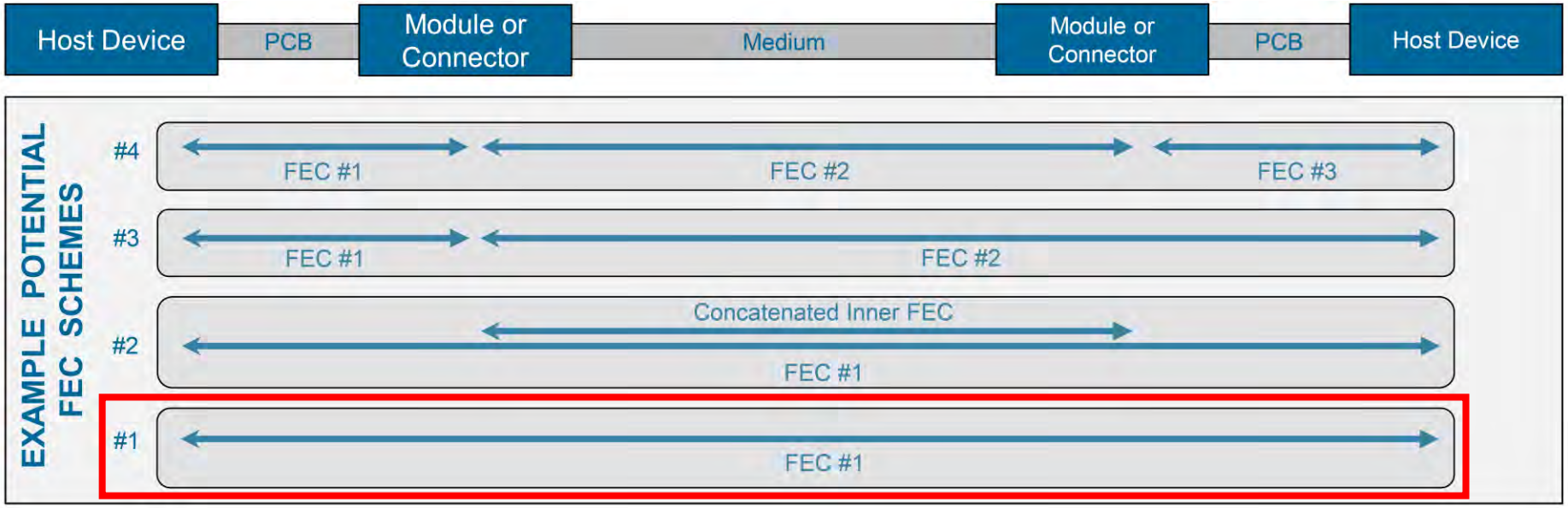
Introduction: 200 Gb/s per Lane PHY

- Various objectives based on 200 Gb/s per lane technology have been adopted in P802.3df/dj for 800G/1.6TbE, including C2C/C2M AUIs, CR/KR electrical PMDs, IM-DD(PAM4) optical PMDs, and potential coherent (16QAM) PMDs.
- The PCS, FEC, PMA architecture will have influences on technical specifications for all of these PHYs.
- FEC performance, such as required pre-FEC and post-FEC BER/FLR, should be analyzed for various PCS/FEC/PMA architectures.

Motivation

- To investigate FEC performance for 200 Gb/s per lane based single-part link model, such as CR/KR PMDs.
  - Single-part link: one analyzed instance between interoperating host devices at each end.
  - Moderate FEC performance to support PMD specification development.
  - Multi-part link model will be conducted later in another contribution.



https://www.ieee802.org/3/B400G/public/21_1028/B400G_overview_c_211028.pdf

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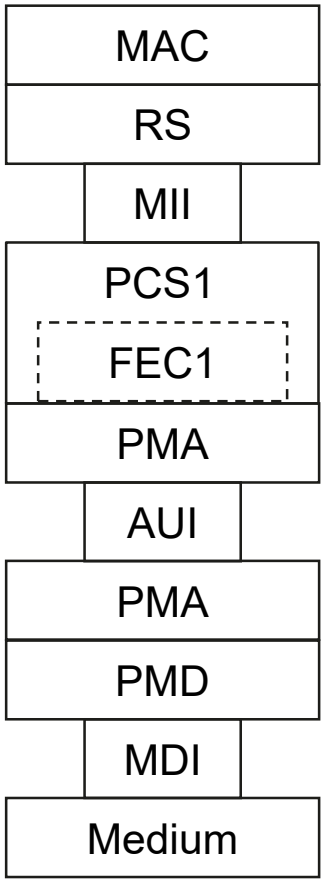
Things to Consider for Single-Part Link FEC Performance

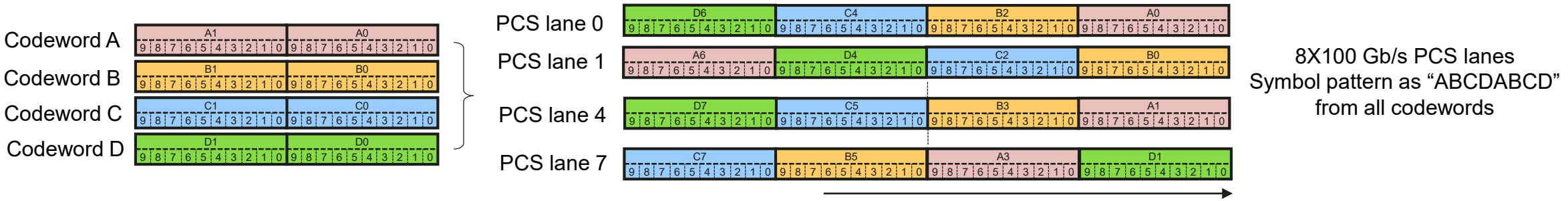


- FEC Scheme: End-2-End, Concatenated, Segmented.
- Number of interleaved FEC codewords.
- Number and rate of PCS lanes.
- Interleave scheme from codewords to form PCS lanes.
- Bit or symbol multiplexing in PMA to form 200 Gb/s per physical lane.
- Gray coding, precoding in PMA.

Assumption for FEC Performance Analysis

- RS(544,514), End-2-End FEC scheme.
- 2 codewords and 4 codewords interleave.
- 100 Gb/s per PCS lane, RS FEC symbol interleaved from 2 or 4 codewords.
- Bit or symbol multiplexing in PMA to form 200 Gb/s per physical lane from 2 PCS lanes.
- Gray coding.
- Burst error model: 1-tap DFE introduced error propagation.
  - DFE tap coefficient is between 0 and 1.
  - Precoding on for a ≥ 0.6.
- BER objective: 1E-13, equivalent to FLR 6.2E-11 for 64-byte frames.
  - Pre-FEC BER: ~2.4E-4?

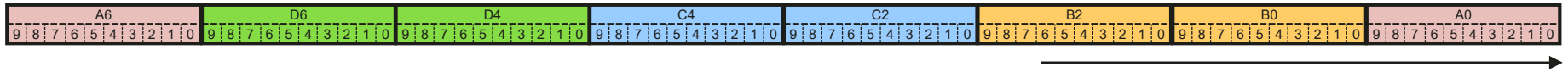
Symbol Multiplexing Cases in PMA



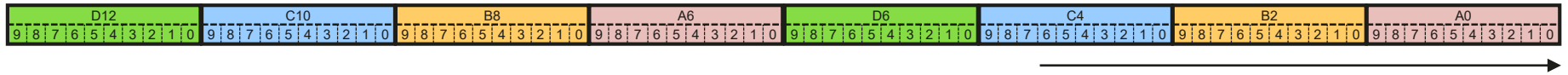
8X100 Gb/s PCS lanes
Symbol pattern as “ABCDABCD” from all codewords

2:1 multiplexing to form 4X200 Gb/s physical lanes, PCS lane 0/1 as example:

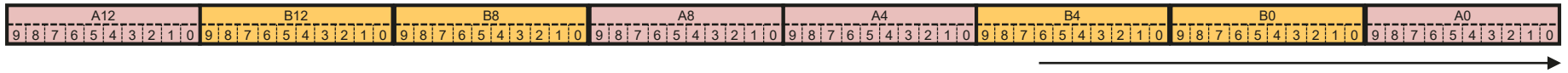
Case #1: 4 codewords, symbol multiplexing with “AABBCCDD” pattern. Worst FEC performance.



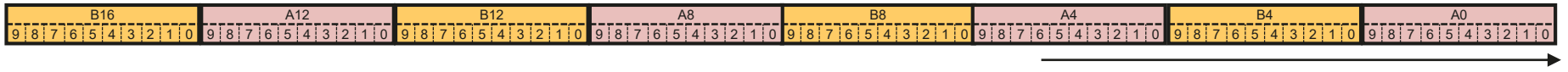
Case #2: 4 codewords, 4-symbol group multiplexing with “ABCDABCD” pattern. Best FEC performance.



Case #3: 2 codewords, symbol multiplexing with “AABB” pattern. Worst FEC performance.

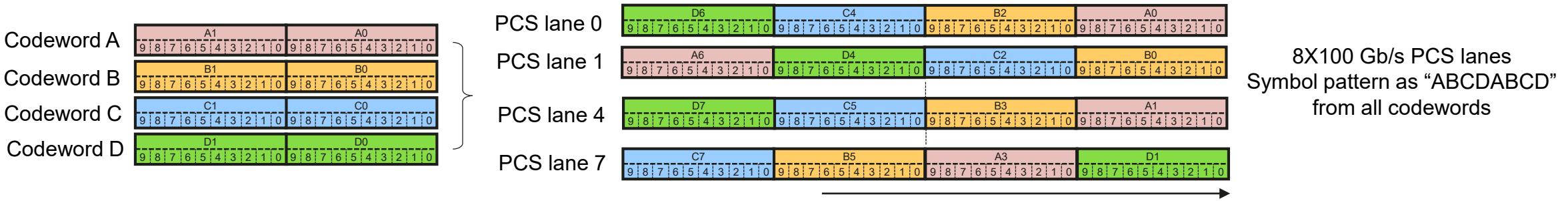


Case #4: 2 codewords, 2-symbol group multiplexing with “ABAB” pattern. Best FEC performance.



Symbol multiplexing in PMA **REQUIRES** PCS lane AM lock only and de-skew.

Bit Multiplexing Cases in PMA

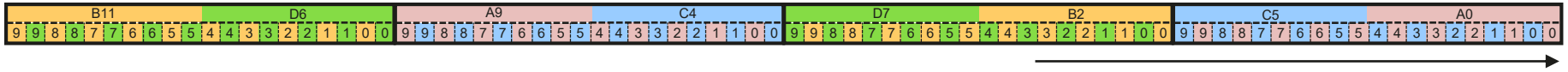


8X100 Gb/s PCS lanes
Symbol pattern as “ABCDABCD” from all codewords

2:1 multiplexing to form 4X200 Gb/s physical lanes, PCS lane 0/4 as example:

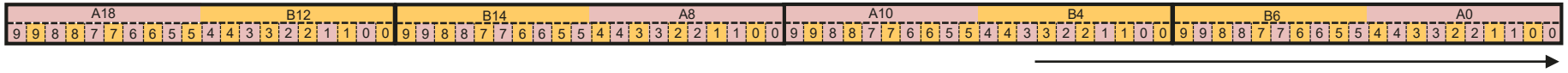
Case #5: 4 codewords, bit multiplexing with “AA/BB/CC/DD” pattern. Worst FEC performance.

Case #6: 4 codewords, bit multiplexing with “AC/BD/CA/DB” pattern. Best FEC performance.



Case #7: 2 codewords, bit multiplexing with “AA/BB” pattern. Worst FEC performance.

Case #8: 2 codewords, bit multiplexing with “AB/BA” pattern. Best FEC performance.



Bit multiplexing in PMA **DOES NOT REQUIRE** PCS lane AM lock and de-skew.

Mathematical Calculation for FEC Performance with Random Errors

$$\mathrm{SER_{in}} = 1 - (1 - \mathrm{BER_{in}})^{\mathrm{m}}$$

$$\mathrm{UCR} = \sum_{\mathrm{i}=t+1}^{\mathrm{n}} \binom{n}{\mathrm{i}} \mathrm{SER^{i}_{in}}(1 - \mathrm{SER_{in}})^{\mathrm{n-i}}$$

$$\mathrm{BER_{out}} = \sum_{i=t+1}^{n} \frac{i}{n} UCR_i \approx \frac{t+1}{n*m} * UCR$$

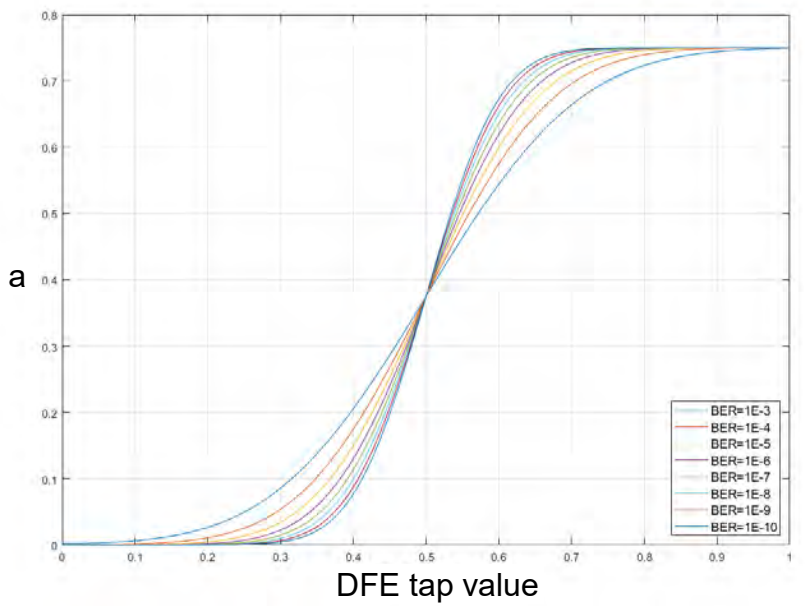
$$\mathrm{FLR} = \mathrm{UCR}*(1+\mathrm{X}*\mathrm{MFC})/\mathrm{MFC}$$

$\mathrm{BER_{in}}$:	Pre-FEC Bit Error Ratio.
$\mathrm{SER_{in}}$:	FEC Symbol Error Ratio.
UCR:	Uncorrectable Codeword Ratio.
$\mathrm{BER_{out}}$:	Post-FEC Bit Error Ratio.
FLR:	Frame Loss Ratio.
n:	FEC codeword size in symbols.
k:	Number of message bits in a FEC codeword.
t:	FEC error correction capability.
m:	Galois Field index.
MFC:	Number of MAC frames per FEC codeword.
X:	Number of interleaved FEC codewords (1, 2, or 4).

- For RS(544,514), n = 544, k = 514, t = 15, m = 10.

Verification of Theoretical FEC Performance Analysis

- Monte Carlo analysis is often used to analyze probability related problems.
  - From Wikipedia: The underlying concept is to use randomness to solve problems that might be deterministic in principle.
- We performed Monte Carlo based simulation over a large number of FEC codewords, with randomly inserted errors, to verify the results from the mathematical analysis.
  - Errors can be with or without bursts.
  - Burst errors are simplified with the 1-tap DFE concept that the probability of error propagation is “a”.
    - E.g. the probability of a burst of n errors is $a^{n-1}(1-a)$.
    - “a” is 0.1, 0.375, 0.5, 0.6, 0.75 in this simulation.



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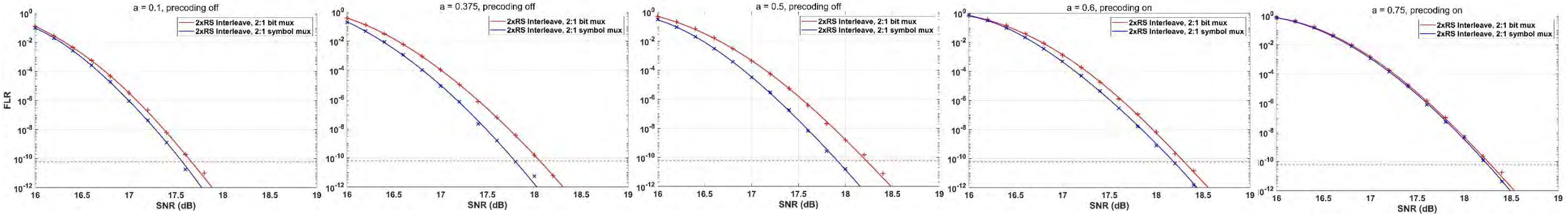
Two Codewords Interleave: Comparing Bit and Symbol Multiplexing

- Based on worst case for both bit and symbol multiplexing schemes, worst FEC performance bound is achieved for a=0.75 with precoding on.
  - No significant FEC performance difference between bit and symbol multiplexing for worst cases.
  - The required SNR for FEC input is ~18.28dB, equivalent to 9.2E-5 random error BER.
    - To account for burst errors, multiply this BER by 2 for a = 0.75 with precoding.



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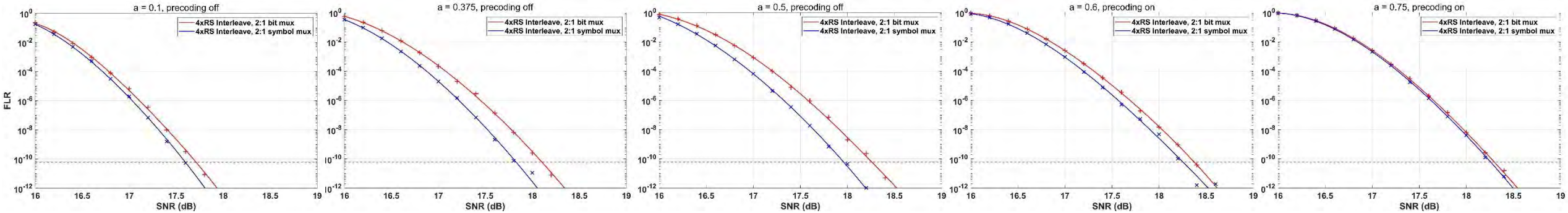
Four Codewords Interleave: Comparing Bit and Symbol Multiplexing

- Based on worst case for both bit and symbol multiplexing schemes, worst FEC performance bound is achieved for a=0.75 with precoding on.
  - No significant FEC performance difference between bit and symbol multiplexing for worst cases.
  - The required SNR for FEC input is ~18.30dB, equivalent to 8.9E-5 random error BER
    - To account for burst errors, multiply this BER by 2 for a = 0.75 with precoding.



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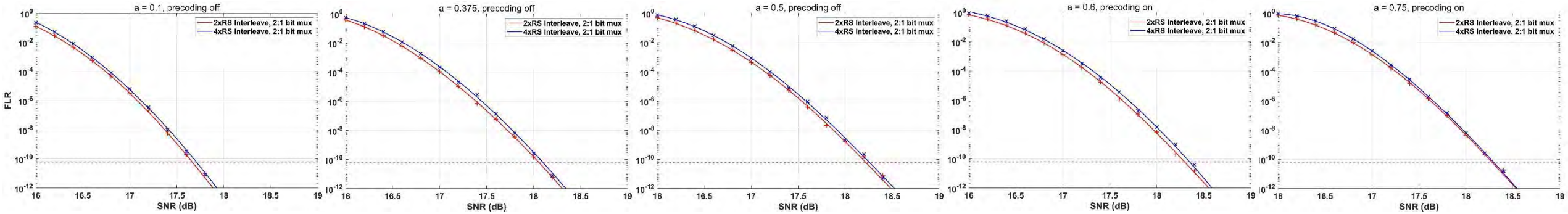
Comparing Two and Four Codewords Interleave with Bit Multiplexing

- Based on worst case for bit multiplexing for both 2X and 4X RS(544,514) codewords interleave, worst FEC performance bound is achieved for a=0.75 with precoding on.
  - No significant FEC performance difference between 2X and 4X.
  - The required SNR for FEC input is ~18.30dB, equivalent to 8.9E-5 random error BER.
    - To account for burst errors, multiply this BER by 2 for a = 0.75 with precoding.



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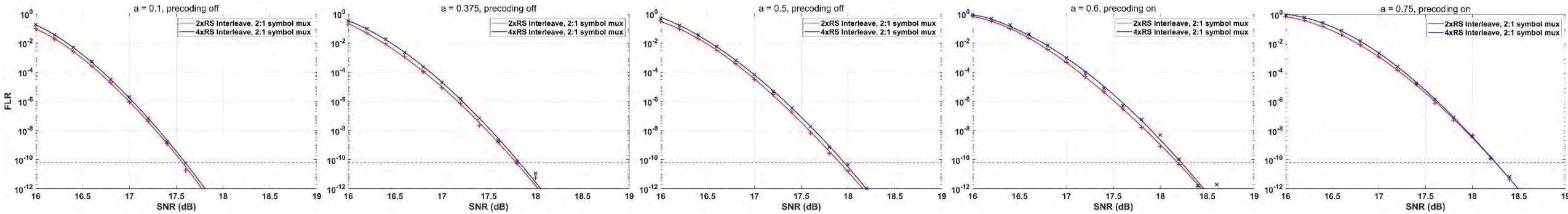
Comparing Two and Four Codewords Interleave with Symbol Multiplexing

- Based on worst case of symbol multiplexing for both 2X and 4X RS(544,514) codewords interleave, worst FEC performance bound is achieved for a=0.75 with precoding on.
  - No significant FEC performance difference between 2X and 4X.
  - The required SNR for FEC input is ~18.25dB, equivalent to 9.6E-5 random error BER.
    - To account for burst errors, multiply this BER by 2 for a = 0.75 with precoding.



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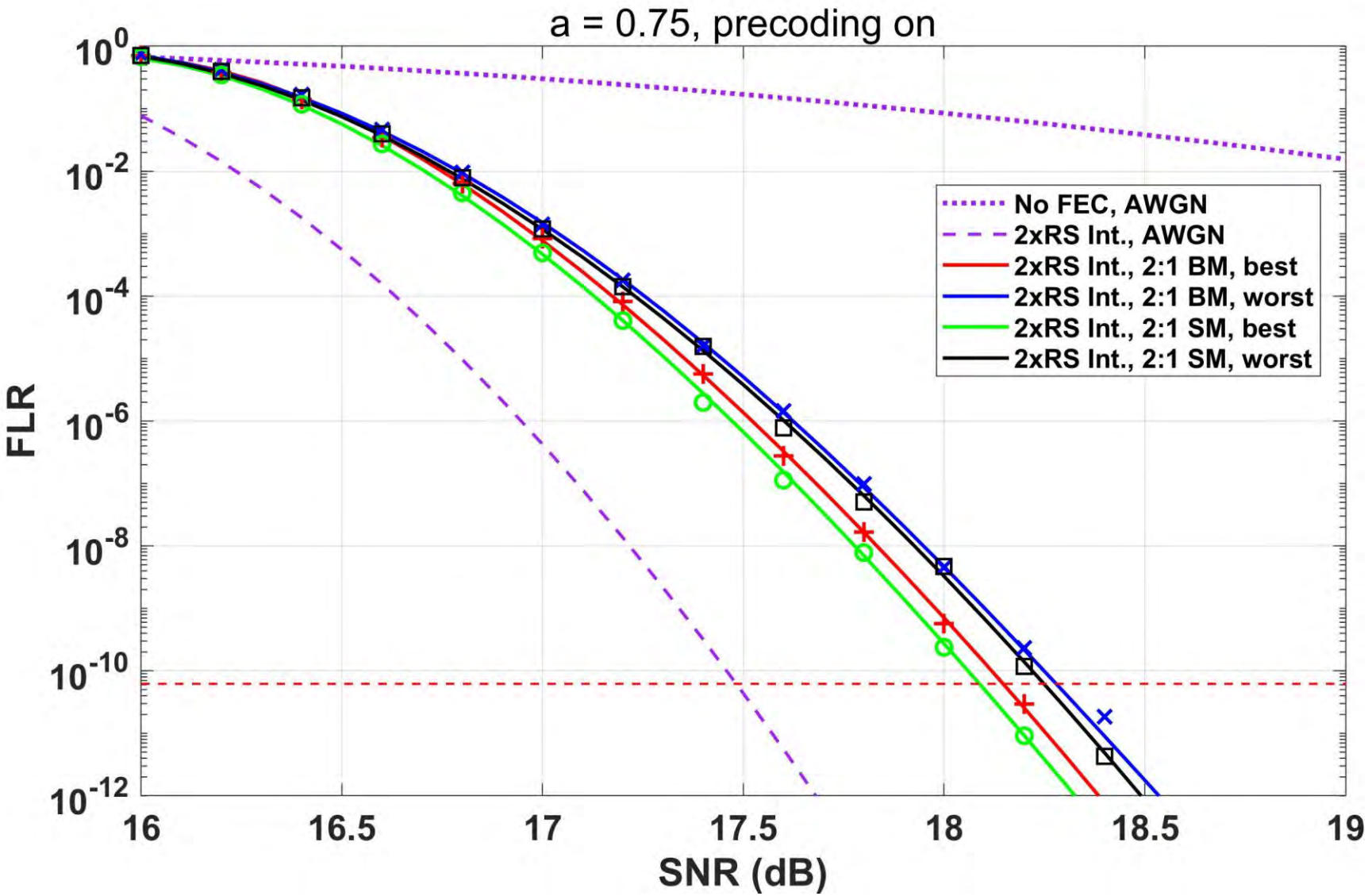
Two Codewords Interleave Comparing Worst/Best Multiplexing



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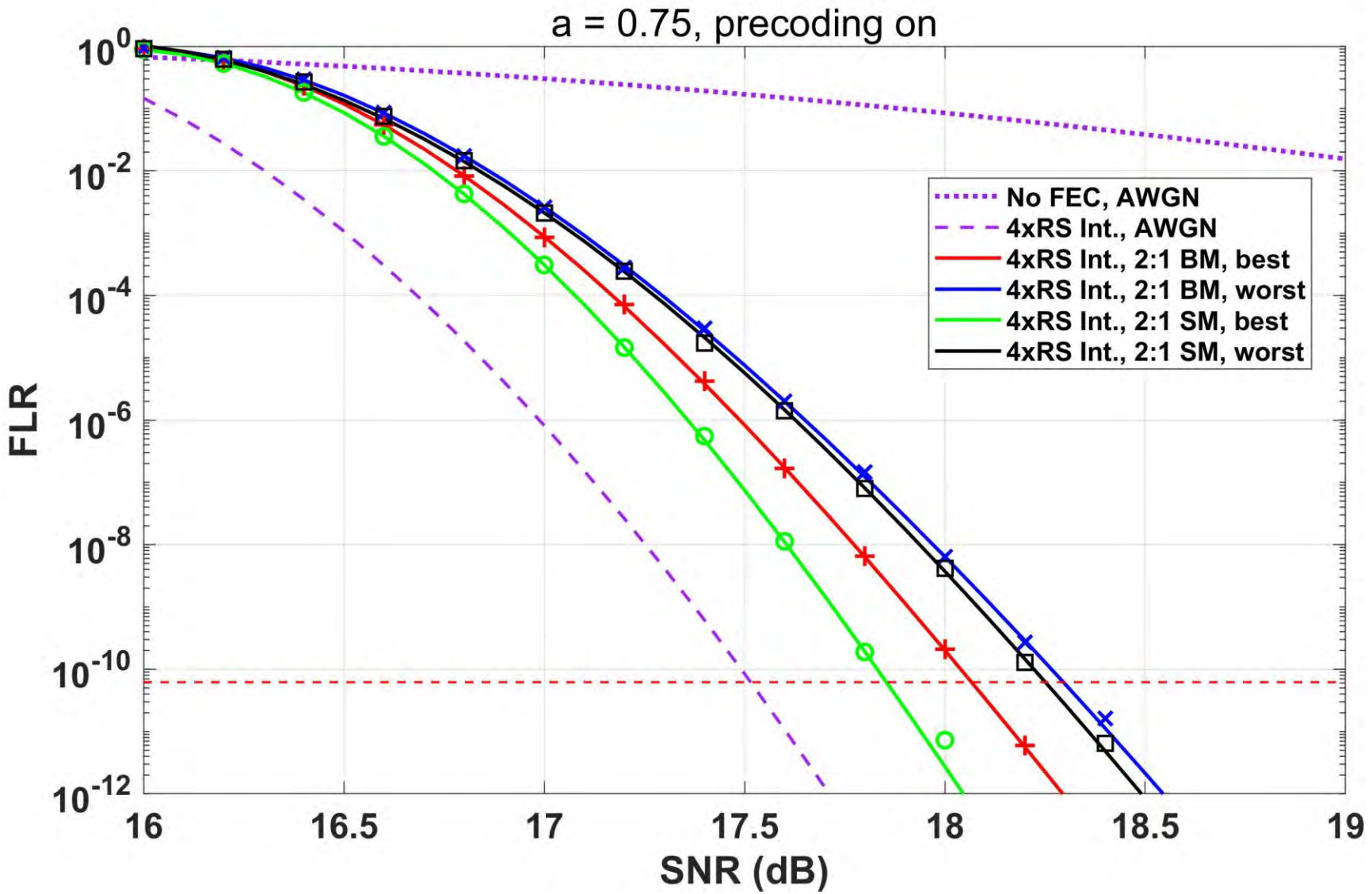
Four Codewords Interleave Comparing Worst/Best Multiplexing



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FEC Performance Results to Meet BER/FLR Objective

- The required SNR and DER at the slicer input, and the corresponding BER values at input of FEC decode to meet FLRs equivalent (6.2E-11) to that of a BER of 1E-13 are:

	Best case			Worst case			Best case			Worst case		
	SNR	DER	BER*	SNR	DER	BER*	SNR	DER	BER*	SNR	DER	BER*
a	2xRS, 8:4 bit mux						2xRS, 8:4 symbol mux					
0	17.48	6.15E-04	3.08E-04	17.48	6.15E-04	3.08E-04	17.48	6.15E-04	3.08E-04	17.48	6.15E-04	3.08E-04
0.1	17.55	5.58E-04	3.10E-04	17.66	4.77E-04	2.65E-04	17.495	6.02E-04	3.35E-04	17.565	5.46E-04	3.03E-04
0.375	17.75	4.18E-04	3.34E-04	18.06	2.61E-04	2.09E-04	17.555	5.54E-04	4.43E-04	17.79	3.94E-04	3.15E-04
0.5	17.93	3.19E-04	3.19E-04	18.22	2.02E-04	2.02E-04	17.625	5.01E-04	5.01E-04	17.91	3.29E-04	3.29E-04
0.6**	18.03	2.73E-04	2.73E-04	18.295	1.78E-04	1.78E-04	17.85	3.60E-04	3.60E-04	18.185	2.14E-04	2.14E-04
0.75**	18.15	2.26E-04	2.26E-04	18.28	1.83E-04	1.83E-04	18.09	2.49E-04	2.49E-04	18.25	1.92E-04	1.92E-04
a	4xRS, 8:4 bit mux						4xRS, 8:4 symbol mux					
0	17.515	5.86E-04	2.93E-04	17.515	5.86E-04	2.93E-04	17.515	5.86E-04	2.93E-04	17.515	5.86E-04	2.93E-04
0.1	17.56	5.50E-04	3.05E-04	17.71	4.43E-04	2.46E-04	17.52	5.82E-04	3.23E-04	17.595	5.23E-04	2.91E-04
0.375	17.74	4.24E-04	3.39E-04	18.1	2.45E-04	1.96E-04	17.58	5.34E-04	4.28E-04	17.825	3.74E-04	2.99E-04
0.5	17.87	3.50E-04	3.50E-04	18.26	1.89E-04	1.89E-04	17.655	4.80E-04	4.80E-04	17.96	3.05E-04	3.05E-04
0.6**	17.975	2.98E-04	2.98E-04	18.35	1.63E-04	1.63E-04	17.78	4.00E-04	4.00E-04	18.22	2.02E-04	2.02E-04
0.75**	18.065	2.59E-04	2.59E-04	18.295	1.78E-04	1.78E-04	17.855	3.58E-04	3.58E-04	18.25	1.92E-04	1.92E-04

* These values are the BER including the additional errors due to the bursts. The values have been multiplied by 1.11 when a = 0.1, by 1.6 when a = 0.375, and by 2 when a = 0.5/0.6/0.75.

** Precoding is turned on for a = 0.6 and 0.75.

Summary

- For FEC performance analysis of 800G/1.6TbE in single-part link with burst errors, the PMA multiplexing scheme will influence the FEC capability, such as pre-FEC BER and BER/FLR objective.
  - The worst case scheme rather than the best case should be used to evaluate FEC performance, as less restriction is needed.
  - 4X codeword interleave has slightly worse FEC performance than 2X in some scenarios, due to the additional FLR penalty.
  - No significant FEC performance difference between 2:1 bit and symbol multiplexing.

Thanks!