Consideration on the Concatenated FEC for 800G FR4 and LR4

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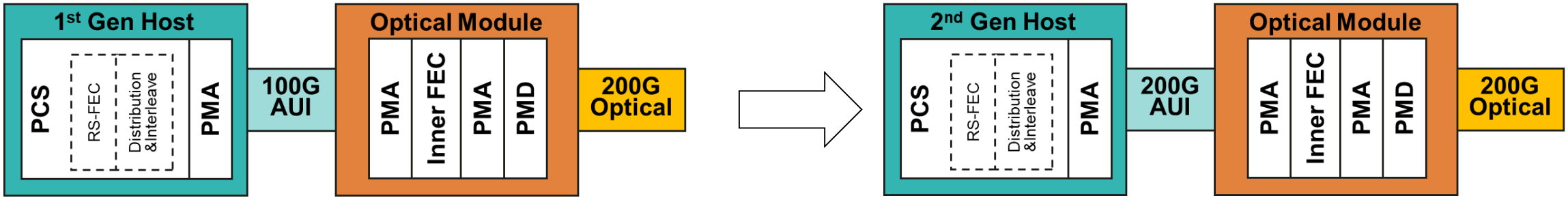
Background

- Technical feasibility on 800G FR4 and LR4 were discussed in the Task Force
  - E.g., kuschnerov_3df_01_220222, lin_3df_01_220609, liu_3df_01b_2207, rodes_3df_01c_2207
  - Receiver sensitivity can be improved about 1.5 dBm by considering pre-FEC BER target from ~2E-3 to ~5E-3
- End-to-end, segmented, and concatenated FEC architectures were discussed, where the Concatenated FEC architecture got lots of interest
  - Concatenated FEC has significant net coding gain (NCG) but with low latency, low power, and good backward compatibility.
  - See he_3df_01a_220308, bliss_3df_01a_220517, patra_3df_01a_2207 for more details
  - KP4 RS(544,514) code in the host acts as the outer code
  - Soft Hamming or BCH code in optical module acts as the inner code
- In this presentation, general consideration on concatenated FEC architecture for 800G FR4 and LR4 will be discussed

Consideration on Concatenated FEC Architecture (1/2)

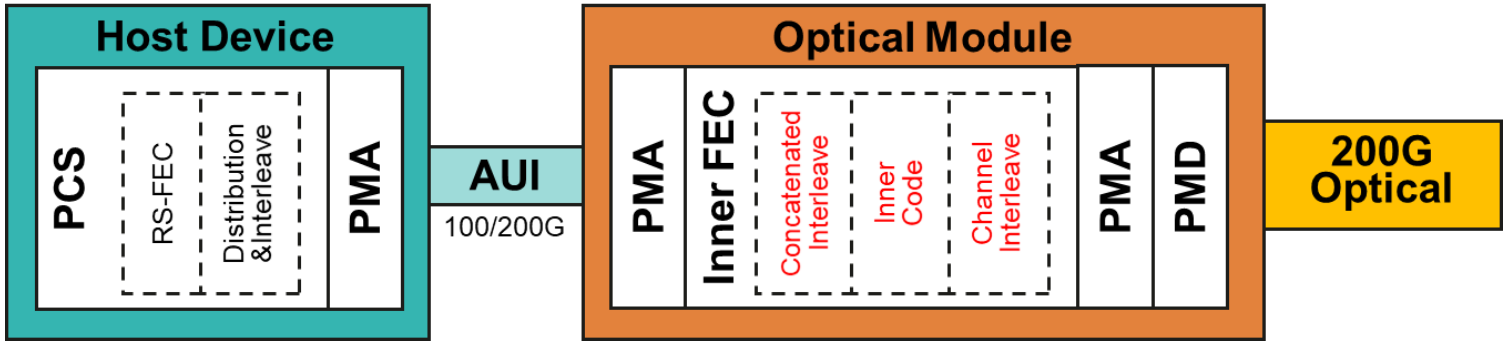


First Generation Development based on 100G/lane AUI

Second Generation Development based on 200G/lane AUI

- "800GbE PCS/FEC/PMA Baseline Proposal for PHYs using 8x100G PMD lanes" passed motion
  - Two 400G FEC flows, and 32 PCS lanes per 800GbE
  - "Does not constrain future PCS/FEC/PMA schemes using 200G/lane AUIs, PMDs and/or Coherent PMDs"
  - See shrikhande_3df_01a_221004 for more details
- More details on 800GbE PCS/FEC/PMA using 200G/lane AUI will be discussed in the Task Force
- Suggest to consider potential forward compatibility of concatenated FEC solution
  - Try to design the concatenated FEC solution to be easily extended to future 800GE host using 200G/lane AUI

Consideration on Concatenated FEC Architecture (2/2)



- Soft inner code with short code length can be used to achieve low latency
  - Hamming(128,120) with rate 15/16 was proposed in bliss_3df_01a_220517, patra_3df_01a_2207, resulting in baudrate 113.33GB
  - Hamming(144,136) with rate 17/18 was proposed in he_3df_01a_220308, resulting in baudrate 112.5GB (720x156.25 MHz)
- Channel Interleaver can be introduced to decorrelate the noise introduced in the optical medium
- Concatenated Interleaver can be introduced to achieve high NCG of the concatenated solution
  - Assuming AWGN channel, the distribution of errors in the inner decoder input is random, while the output error distribution of the soft decoder is very far from random
  - The NCG performance vs. latency was discussed in bliss_3df_01a_220517
  - Convolutional Interleaver instead of Block Interleaver can be used to achieve lower latency, but the synchronization process of the Convolutional De-Interleaver in the receiver side should be taken into consideration, see next page

Toy Example: Convolutional Interleaver and De-Interlevaer

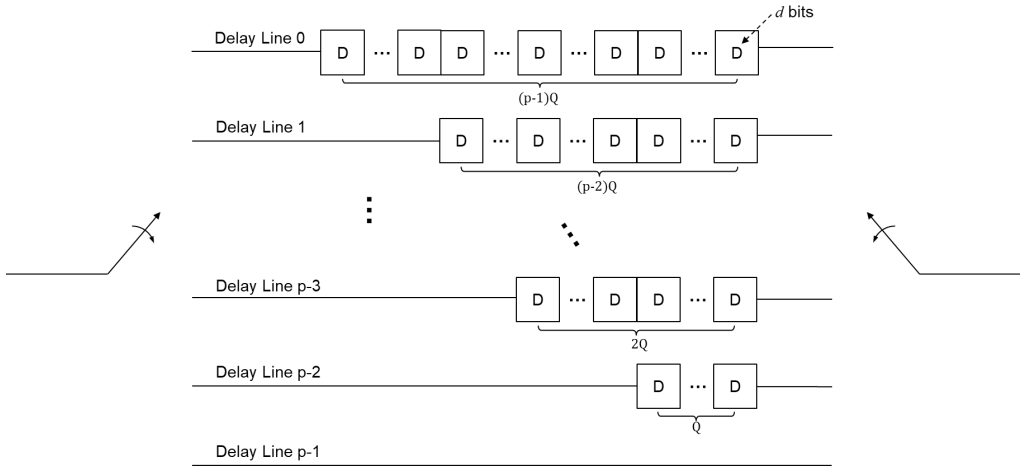


Diagram of Convolution Interleaver

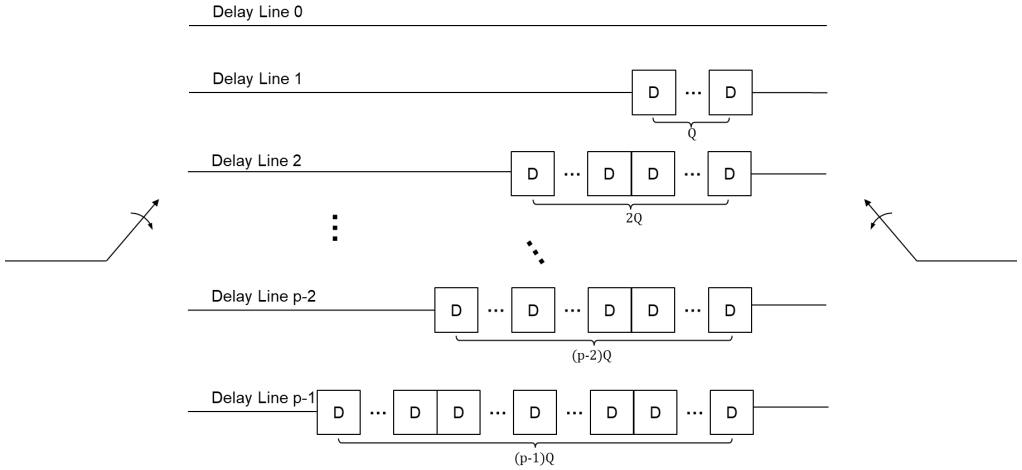
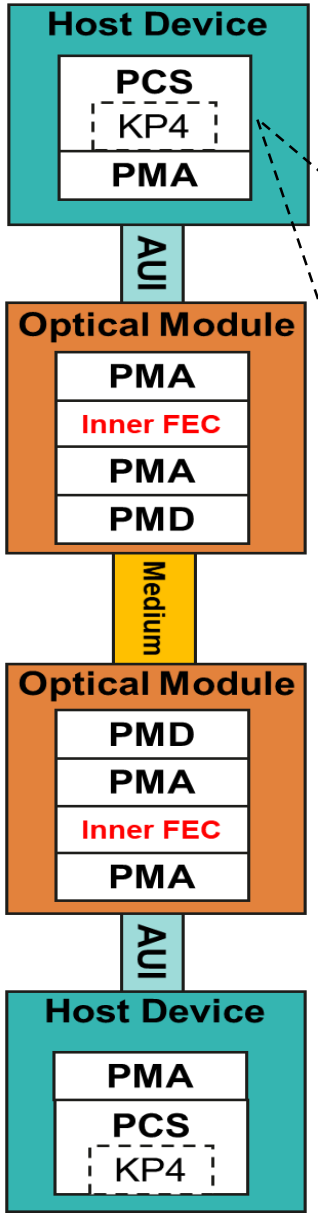
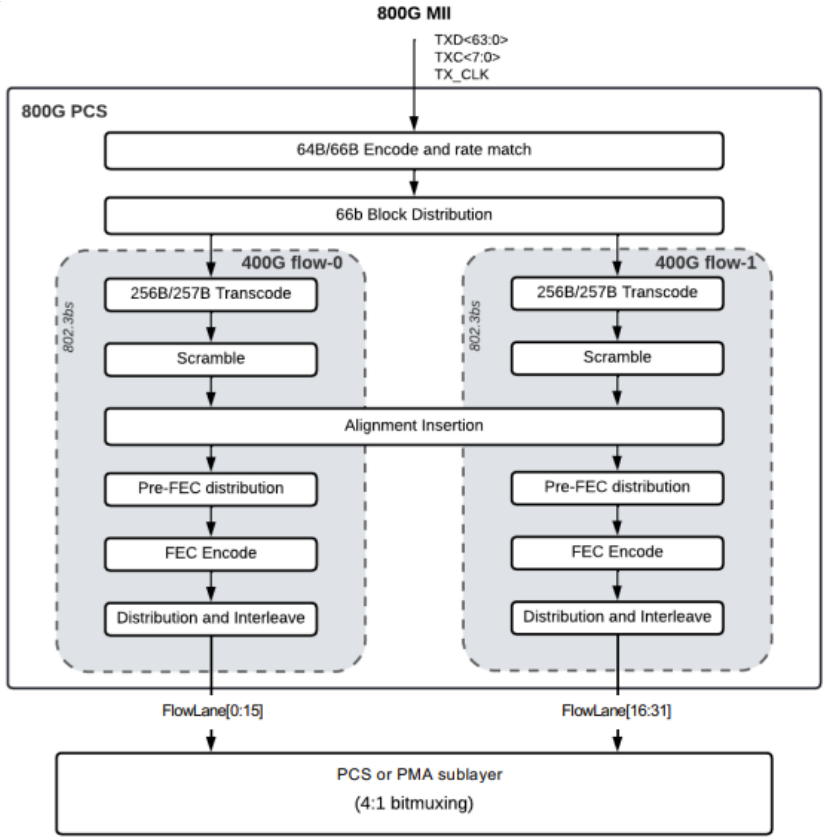


Diagram of Convolution De-Interleaver

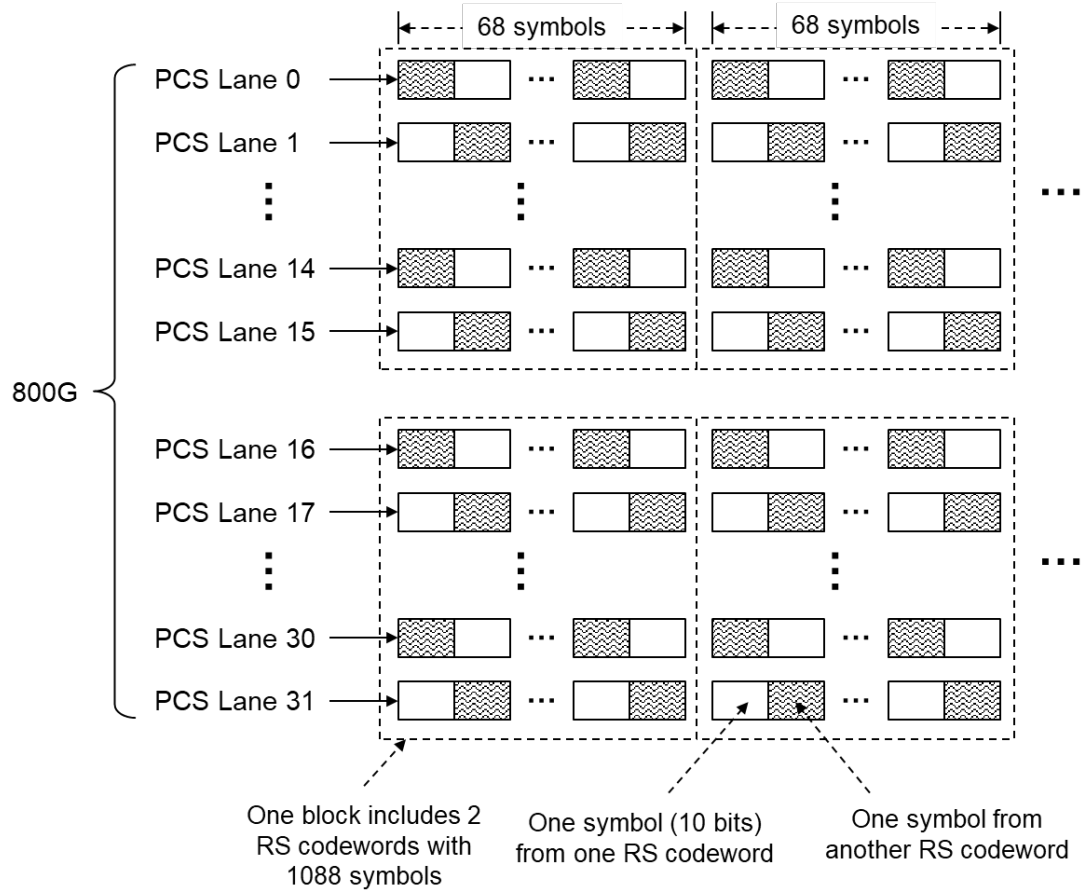
- Take the Convolution Interleaver used in CFEC as example, see IEEE 802.3cw Clause 155.2.4.9, or ITU-T G.709.3 sub-clause 15.4.3 for more details
  - Concatenated Interleaver consists of 16 parallel delay lines; each delay operator “D” represents a storage element of 119 bits; and from one row to the next lower row, two delays operators are deleted;
  - Initialization of the Convolutional Interleave switches to the topmost positions, which occurs at the start of every DSP super frame
  - The switches will wrap around to this topmost position at the start of every ZR frame; that is, ZR frame synchronization guarantees the synchronization of Convolutional De-Interleaver
- Suggest to have joint design of inner code and Convolutional Interleaver to achieve simple synchronization process in receiver side

Potential Concatenated FEC Solution (1/4)



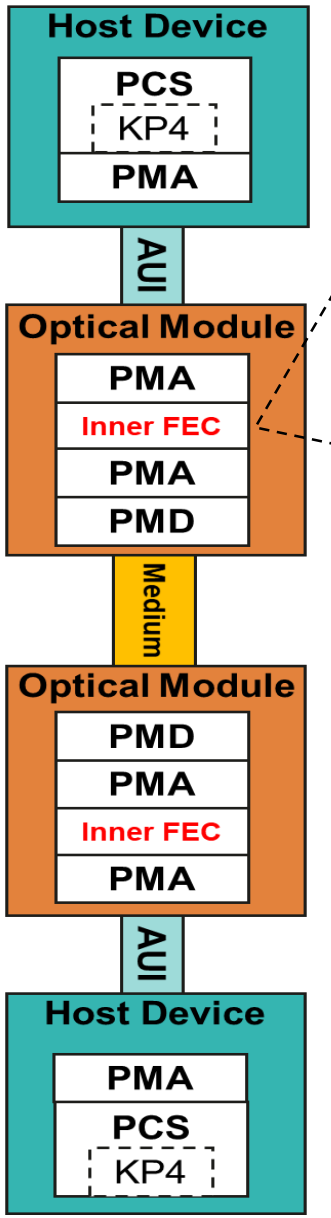


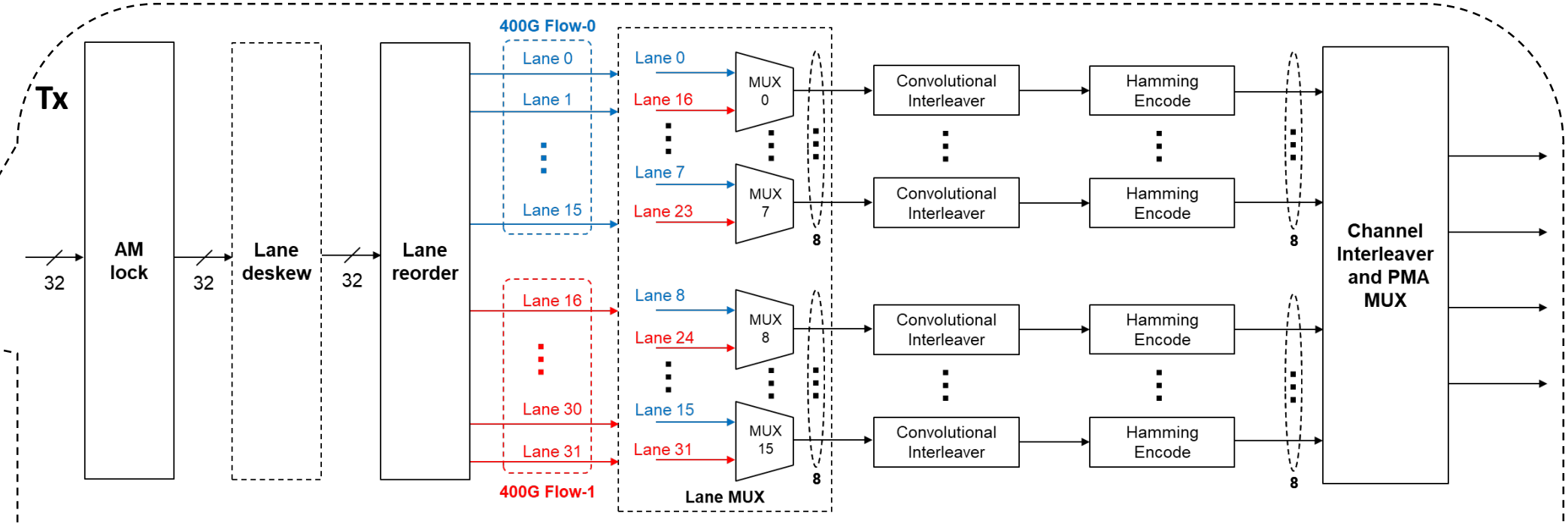
800GbE PCS/FEC/PMA using 8x100G PMD lanes
From page 10 in [shrikhande_3df_01a_221004]



Details on the PCS bit streams

Potential Concatenated FEC Solution (2/4)

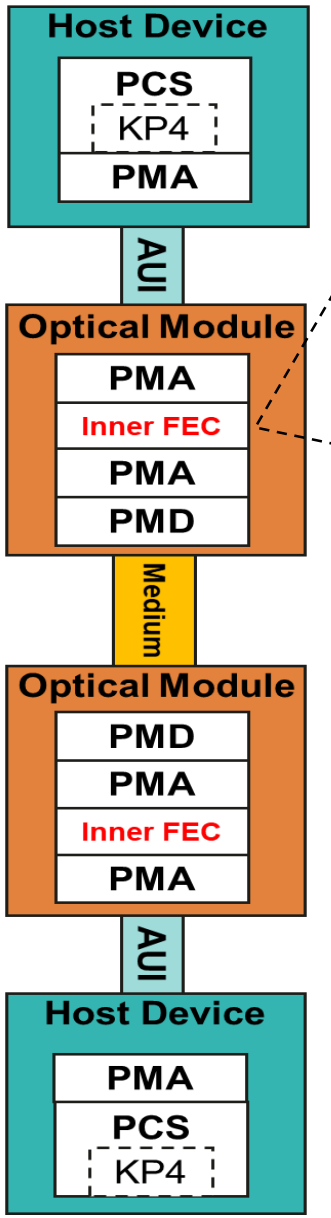


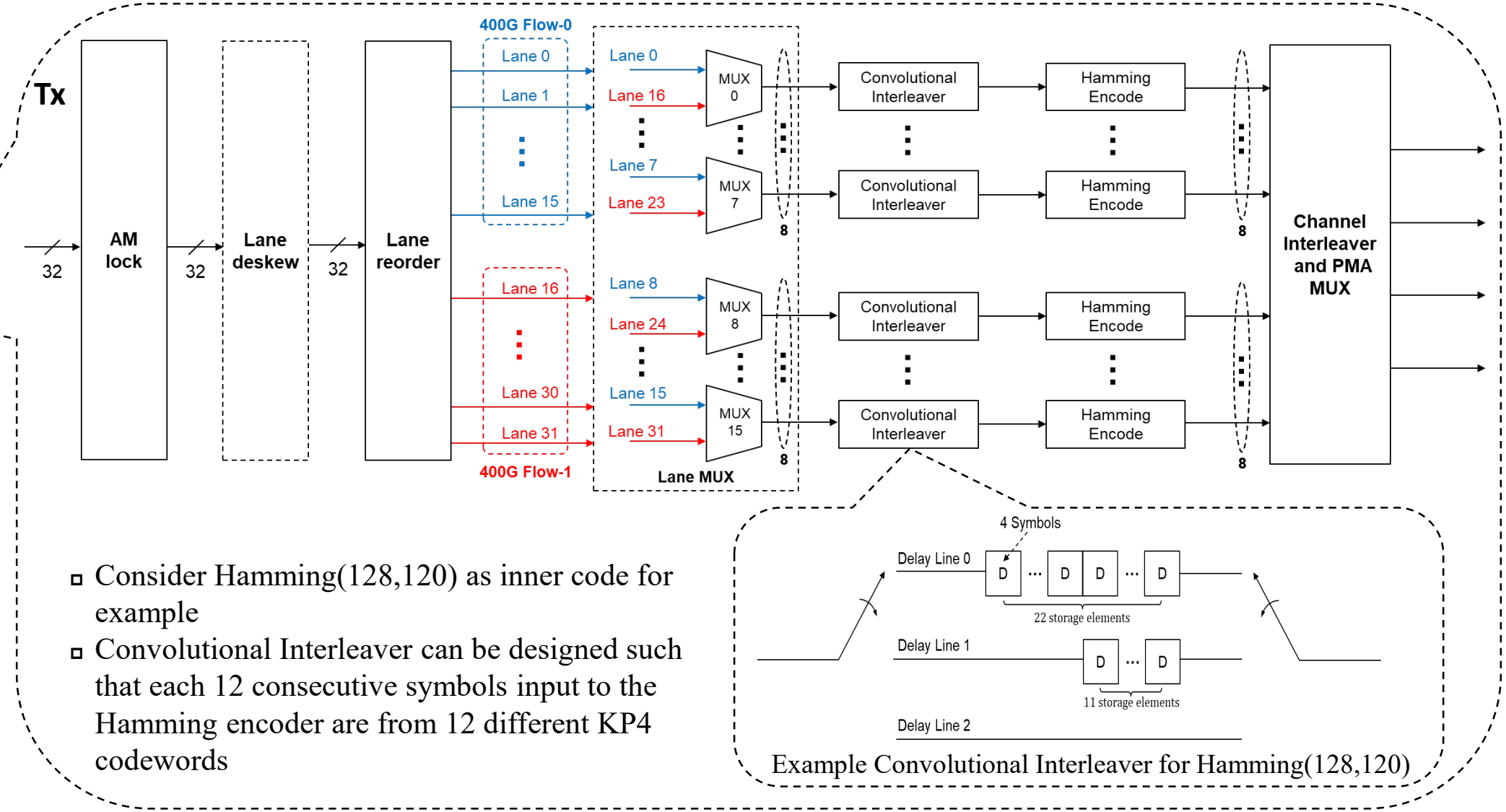


- "Lane deskew" is optional function
- Concatenated Interleaver includes "Lane MUX" and "Convolutional Interleaver"
- "Lane MUX" can be "Symbol MUX" or "Bit MUX"*. Here, take "Symbol MUX" as example
- Before "Lane MUX", each 2 consecutive symbols (each symbol with 10 bits) in any lane are from 2 different KP4 codewords
- In "Lane MUX", 2 input lanes are multiplexed into one output lane, resulting in that each 4 consecutive symbols (each symbol with 10 bits) in the output lane are from 4 different KP4 codeword

* "Bit MUX" before Convolutional Interleaver was introduced in patra_3df_01a_2207 to achieve almost same FEC implementation in optical module for 400G/2x200G PCS with both 100G and 200G AUI.

Potential Concatenated FEC Solution (3/4)

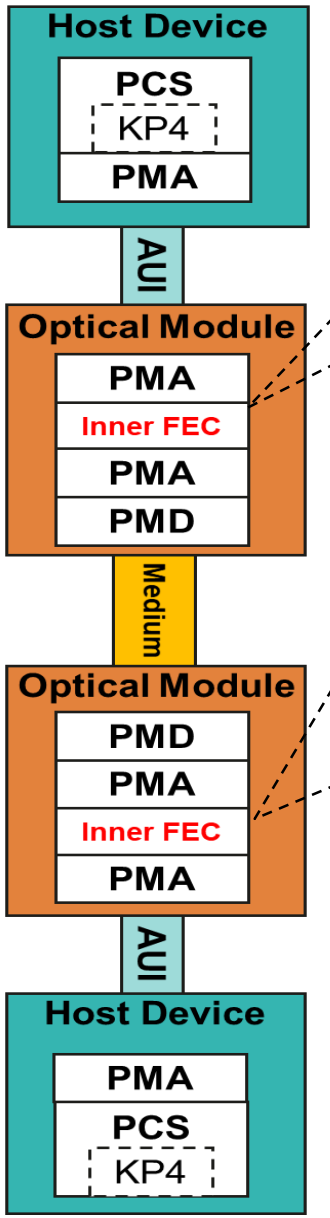


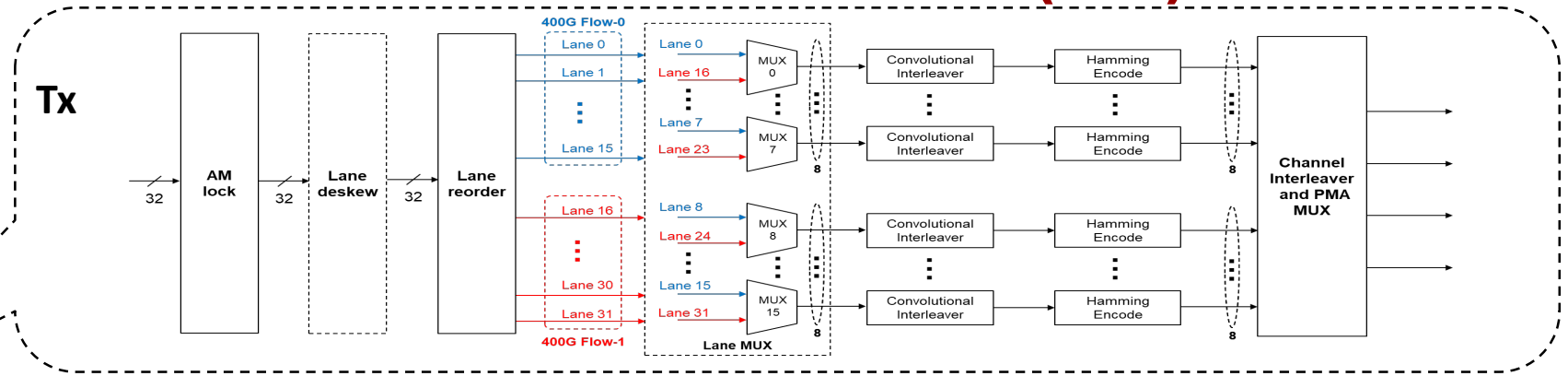


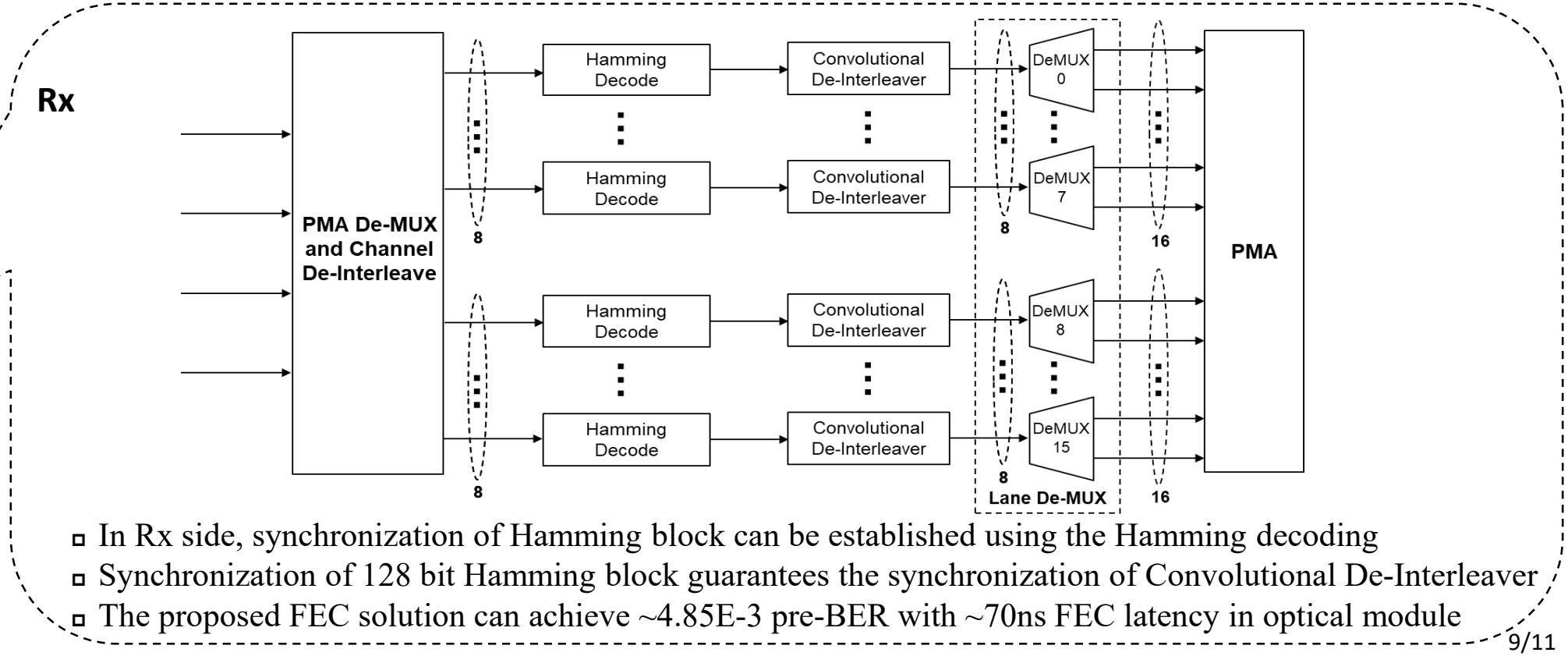
- Consider Hamming(128,120) as inner code for example
- Convolutional Interleaver can be designed such that each 12 consecutive symbols input to the Hamming encoder are from 12 different KP4 codewords

Example Convolutional Interleaver for Hamming(128,120)

Potential Concatenated FEC Solution (4/4)







- In Rx side, synchronization of Hamming block can be established using the Hamming decoding
- Synchronization of 128 bit Hamming block guarantees the synchronization of Convolutional De-Interleaver
- The proposed FEC solution can achieve ~4.85E-3 pre-BER with ~70ns FEC latency in optical module

Summary

- The consideration on concatenated FEC architecture for 800G FR4 and LR4 is discussed
  - Suggest to design the concatenated FEC solution that can be easily extended to future 800GE host using 200G/lane AUI
  - Suggest to take the receive function of optical module into consideration when designing the inner code and concatenated interleaver
- One concatenated FEC architecture for 800G FR4 and LR4 is proposed
  - First consider the 800GbE host using 100G/lane AUI
  - KP4 RS(544,514) code in the host acts as the outer code
  - Soft Hamming code in optical module acts as the inner code
  - Concatenated Interleaver includes “Lane MUX” and “Convolutional Interleaver”
- Next steps:
  - To further optimize the solution based on the following discussion about 800G host using 200G/lane AUI
  - To work on Channel Interleaver design, and synchronization analysis

Thank you