Power Considerations for 200G/L AUI

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Outline

- Potential Loss Targets for 200G/L AUI C2M
- 100G/L SerDes Power Survey
- 200G/L Module Power Discussion

Background

- **Assessing AUI C2M loss direction is in a rush to progress PCS, FEC architecture, and optical PHYs**
- **key debates of lusted_3df_01_220927 are associated with the channel construction and the state-of-the-art of PCB/package design**
- **Potential loss targets of 200G/L AUI C2M**

	Loss Target	Channel Construction	FEC	Electrical Spec
Medium loss	~22 dB	• Advance package or medium radix • Advance PCB, CPC, or NPC	W/o termination	DER = 1e-5 Weaker SerDes (Similar to 100G/L C2M)
High loss	~36 dB	• Conventional package or large radix • Conventional PCB	Termination of RS544	DER = 1e-4 Stronger SerDes (Similar to 100G/L CR)
			W/o termination	DER = 1e-5 Even Stronger SerDes (>100G/L CR, possibly MLSE)
Others	~12 dB or ~18 dB	Co-packaged with or without 1st level package		

→ SerDes power challenge and potential solutions can be observed by balancing TX/RX EQ

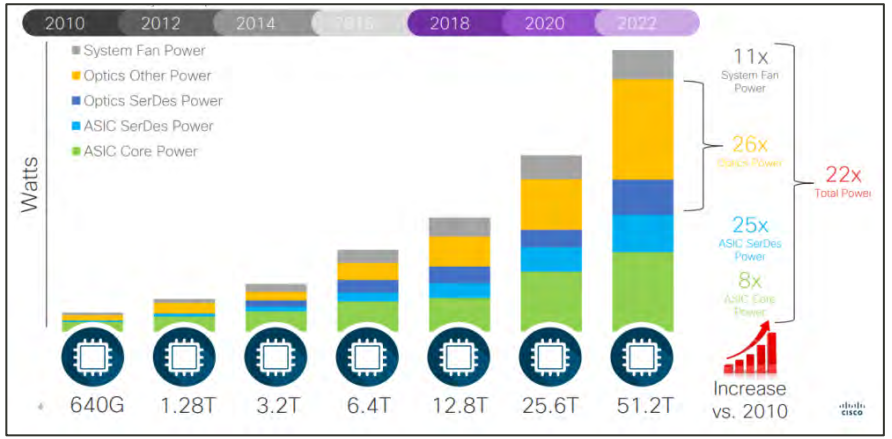
Evolution of System Power

- **Power objectives for next-generation modules**
  - **Based on OSFP-XD form factor**

Capacity	Reach	Expectation
1.6T or 3.2T	ZR	Up to 40W

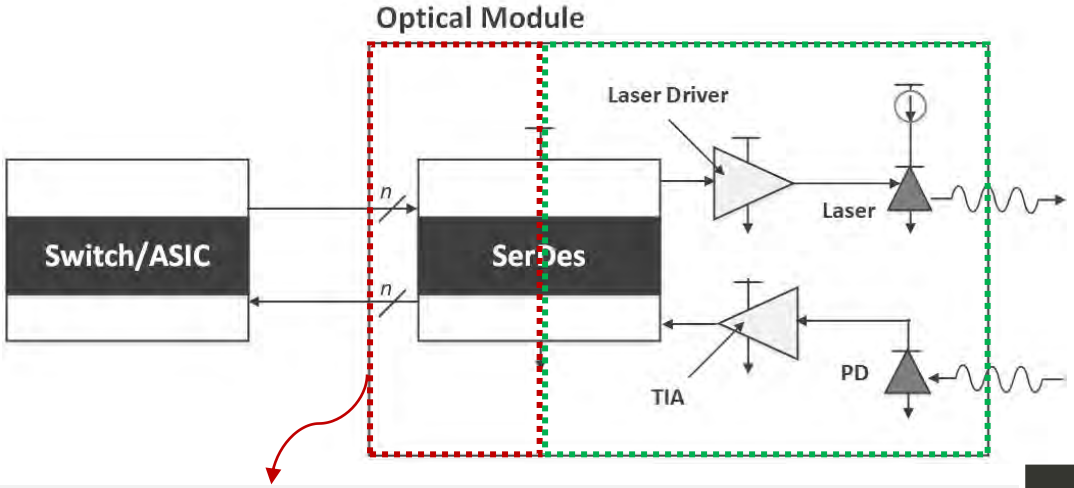
** Ref: [The Next Generation of Pluggable Optical Module Solutions](), OSFP MSA, Sept. 2022*

- **For higher-speed, power proportion at electrical-side becomes larger**
- **For longer reach at optical side, power proportion at line-side becomes larger**



** Source: [chopra_b400g_01_210208]()*

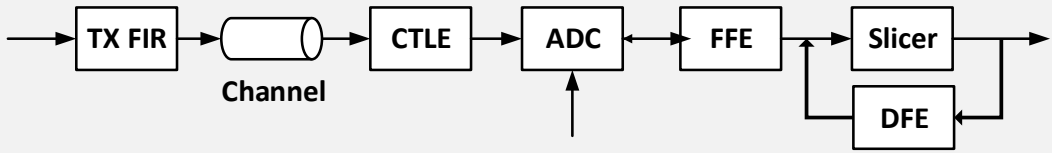
Power Composition



200G/L optical power?
→ Call to action

Major blocks of a typical SerDes

- *Take **ADC-based diagram for 100G-LR** as example*



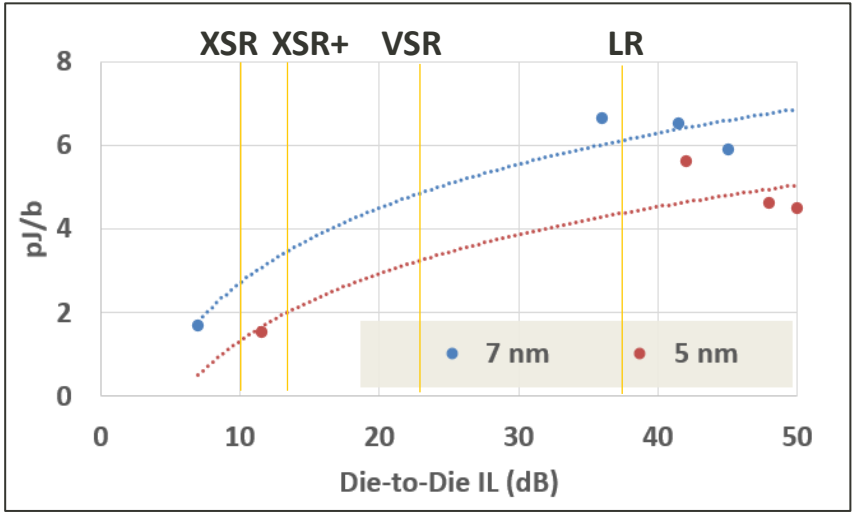
	Loss Target	FEC Termination	Electrical Spec
Medium Loss	~22 dB	X	Weaker SerDes (**Similar to 100G/L C2M**)
High Loss	~36 dB	V	Stronger SerDes (**Similar to 100G/L CR**)
		X	Even Stronger SerDes (**Stronger than 100G/L CR, possibly MLSE**)

100G/L SerDes Power Survey

	ISSCC 2023 [1]	ISSCC 2022 [2]	VLSI 2022 [3]	ISSCC 2021 [4]	ISSCC 2021 [5]	ISSCC 2022 [6]	ISSCC 2021 [7]
Company	MediaTek	Marvell	Cadence	Huawei Ottawa Research and Development Centre	Inphi	Marvell	MediaTek
Process node	5nm	5nm	5nm	7nm	7nm	5nm	7nm
Data rate	112.5G	112G	112.5G	112G	112G	113G	112G
Loss [dB]	48 (LR)	50 (LR)	42 (LR)	45 (LR)	41.5 (LR)	11.5 (XSR)	7 (XSR)
TX topology	7-bit DAC	7.5-bit DAC	7-bit DAC	7-bit DAC	7-bit DAC	Analog FFE	5-bit DAC
TX FFE taps	6	6	5	7	4+7	4+2	5
RX topology	7-bit ADC A: ATT/VGA/CTLE	7-bit ADC A: CTLE	7-bit ADC A: VGA1/VGA2	7-bit ADC A: ATT/CTLE/VGA	8-bit ADC A: CTLE/VGA	A: CTLE/VGA	A: CTLE/VGA
RX FFE taps	24 + 8 FLT	22 + 8 FLT	30	25	DSP	-	-
DFE taps	1	1	1	2	DSP	-	-
Area/lane [mm^2]	0.461	0.49	0.372	0.531	0.92	0.264	0.228
Power/lane [pJ/bit]	4.63	4.5	5.62	5.91	6.51	1.55	1.71
Total power [mW]	A: 348.4 D: 172.6	A: 302.4 D: 201.6	A: 395 D: 237	A: 450 D: 212	729.1		A: 153 D: 38

SerDes Energy Efficiency

- **200G/L SerDes power?**
  - Analog power mainly limits the energy efficiency as process improved
  - Power forecast: 4~5 pJ/b
    - Except for power consumption of FEC termination at module side



	Loss Target	FEC Termination	Electrical Spec	100G/L Energy Efficiency	200G/L Energy Efficiency	200G/L Power Prediction
Medium Loss	~22 dB	X	DER = 1e-5, Weaker SerDes (**Similar to 100G/L C2M**)	4~5pJ/b	~ 3.5 pJ/b	3.5pJ/b*1.6Tb/s = 5.6W
High Loss	~36 dB	V	DER = 1e-4, Stronger SerDes (**Similar to 100G/L CR**)	5~6pJ/b	~ 4.5 pJ/b	4.5pJ/b*1.6Tb/s = 7.2W
		X	DER = 1e-5, Even Stronger SerDes (**> 100G/L CR, possibly MLSE**)		> 4.5 pJ/b	> 7.2W

** This contribution is mainly based on published papers [1-6] and general design rules*

Summary

- **Power challenge in 200G/L optical PMD SerDes to line-side (optical fiber) can help set a C2M AUI loss direction**

	Loss Target	200G/L SerDes Power Prediction
Medium Loss	~22 dB	~5.6W
High Loss	~36 dB	~7.2W or higher

Call to Action

- **Buck converter is under-determined**
  - Efficiency of a DC/DC converter: η (%) = Output Power (W) / Input Power (W) x 100
- **Power consumption of FEC termination at module side is under-determined**
- **Power consumption of optical I/O is under-determined**
  → 200G/L optical PMD power landscape?

Reference

[1] H. Park et al., “A 4.63pJ/b 112Gbps DSP-based PAM-4 Transceiver for a Large-Scale Integration in 5nm FinFET”, to be appeared in ISSCC, 2023

[2] Z. Guo et al., “A 112.5Gb/s ADC-DSP-Based PAM-4 Long-Reach Transceiver with >50dB Channel Loss in 5nm FinFET”, ISSCC, pp. 116-118, Feb. 2022

[3] A. Varzaghani et al., “A 1-to-112Gb/s DSP-Based Wireline Transceiver with a Flexible Clocking Scheme in 5nm FinFET”, VLSI, pp. 132-134, June. 2022

[4] M. LaCroix et al., “A 116Gb/s DSP-Based Wireline Transceiver in 7nm CMOS Achieving 6pJ/b at 45dB Loss in PAM-4/Duo-PAM-4 and 52dB in PAM-2”, ISSCC, pp. 132-134, Feb. 2021

[5] P. Mishra et al., “A 112Gb/s ADC-DSP-Based PAM-4 Transceiver for Long-Reach Applications with >40dB Channel Loss in 7nm FinFET”, ISSCC, pp. 138-140, Feb. 2021

[6] G. Gangasani, et al. “A 1.6 Tb/s Chiplet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Dynamic Receiver-Driven Adaptation of TX-FFE and Programmable Roaming Taps in 5nm CMOS”, ISSCC, pp. 122-124, Feb. 2022

[7] R. Yousry et al., “A 1.7pJ/b 112Gb/s XSR Transceiver for Intra-Package Communication in 7nm FinFET Technology”, ISSCC, pp. 180-182, Feb. 2021

Thank you

Questions and Discussions

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