Characteristics of a 224Gbps Chip to Module Channel with Various Host Architectures

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EVERY CONNECTION COUNTS

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Overview

A preliminary investigation into chip to module channels, based on conventional and unconventional architecture concepts, is presented to help guide P802.3df architecture discussions.

Development work is on-going, updates and refinements are anticipated in future contributions

This is not intended to be a final position or a proposal on a chip to module channel performance

The intent of this presentation is to provide directional input at this early stage of the project and promote discussion among the participants

Additional development is in process on the connectors and cables

Host Architecture Background

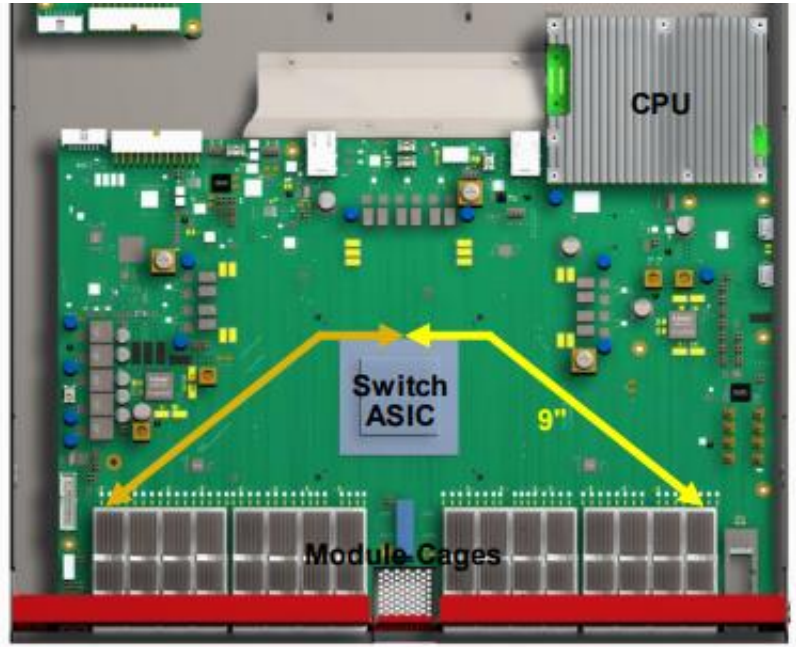
From IEEE 802.3 Beyond 400G Study Group:
https://www.ieee802.org/3/B400G/public/21_08/kocsis_b400g_01a_210826.pdf :

Typical physical length for a host ASIC to IO port in a 32 port 1RU form factor:

- 18 ports out of 32 ports <5”
  - 8 out of 32 ports <3”
- 6 ports out of 32 ports 5-7”
- 8 ports out of 32 ports 7-9”

Although PCB traces have been the conventional media from ASIC to IO port, there are multiple alternates that can be considered

Any improved channel alternate would be beneficial for consideration of both VSR and LR (copper cable) applications

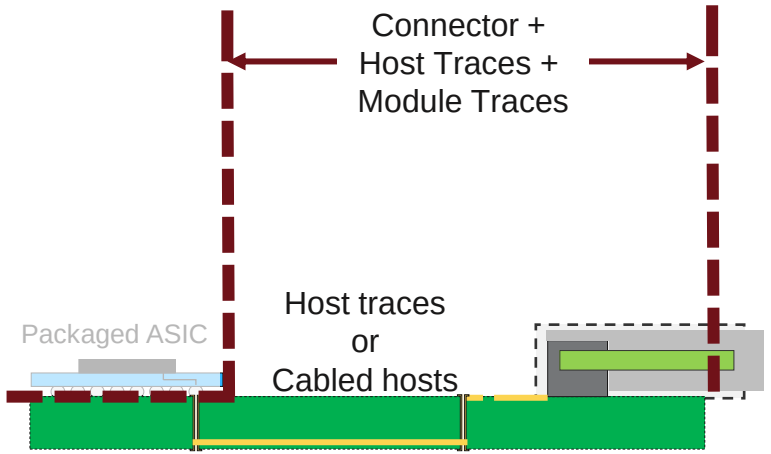


There are multiple presentations on ASIC to port reach that support the cited numbers:

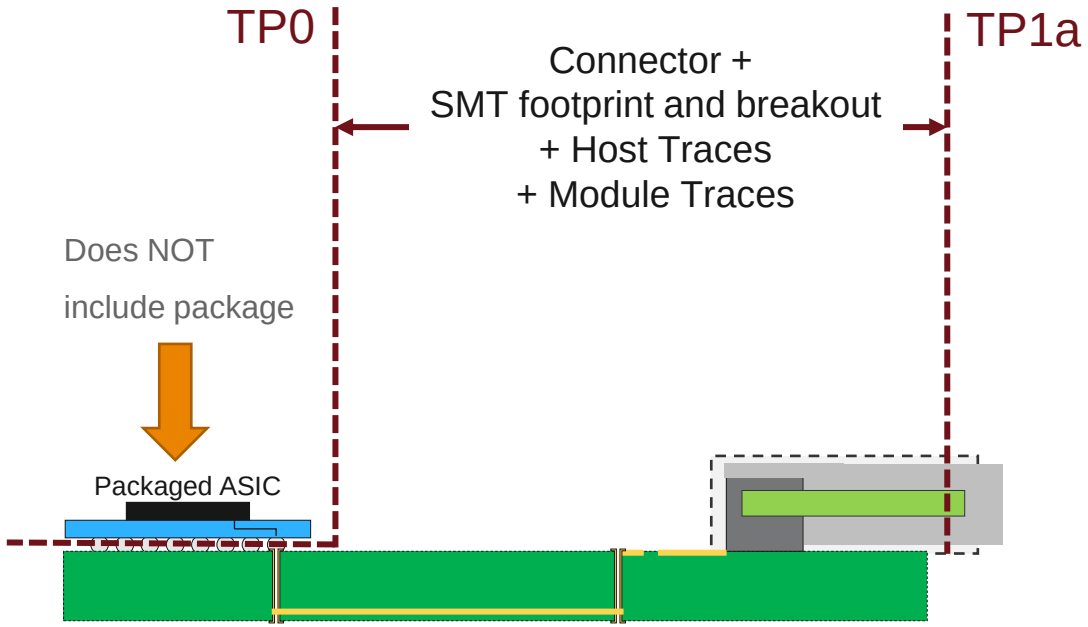
https://www.ieee802.org/3/100GEL/public/18_03/stone_100GEL_01_0318.pdf
https://www.ieee802.org/3/B400G/public/21_05/noujeim_b400g_01_210517.pdf
https://www.ieee802.org/3/ck/public/21_07/dawe_3ck_01_0721.pdf

Description

- Simulation for 200G chip to module channels using concept connector with various host architecture options
- Includes BGA escape model provided by Regee Petaja of Broadcom
- Does NOT include silicon package
- Current view of Chip to Module performance in various host implementations
- What this presentation is NOT:
  - Modulation proposal
  - Channel or host loss proposal
  - Compliance board proposal
  - A specific host architecture proposal;
    - comparative performance options are presented, i.e., traces vs. cabled host to “near ASIC” vs. co-package copper
  - Asymmetric architectures (managed deployment)

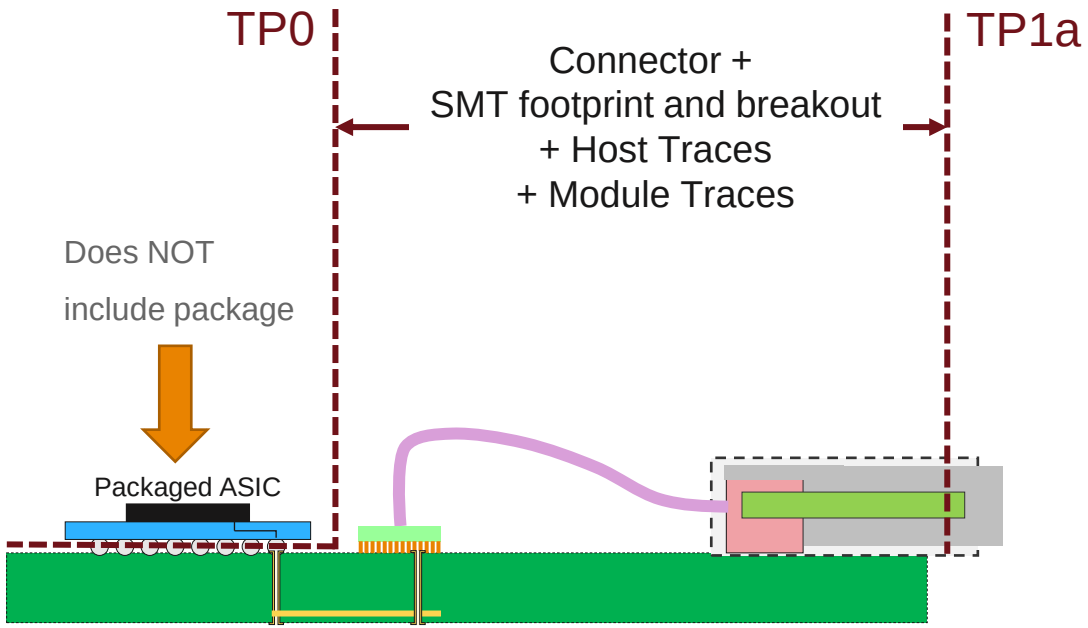


Conventional Host



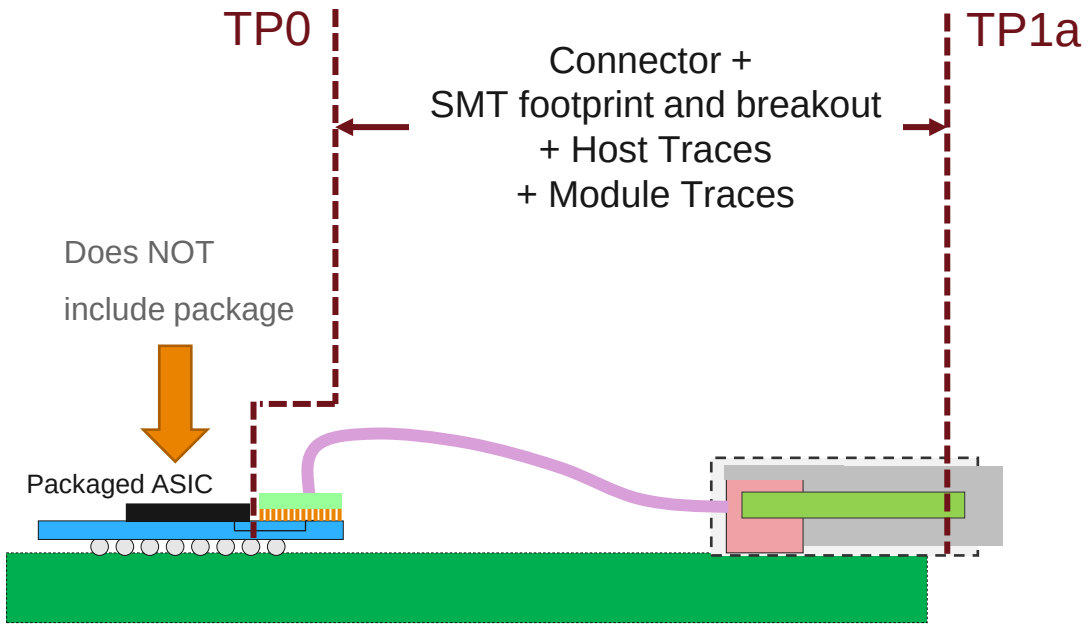
- OSFP SMT 200G Connector
- Host Footprint and via transition, 1mm via with ~5mil stub included
- Host Traces, 5” or 7” or 13” long [5.8mil wide], ~1.08dB/in loss at 53.125GHz
- Module Traces, 2” long [5.8mil wide], ~1.08dB/in loss at 53.125GHz
- BGA footprint + breakout

Near Chip Copper [NCC] Host



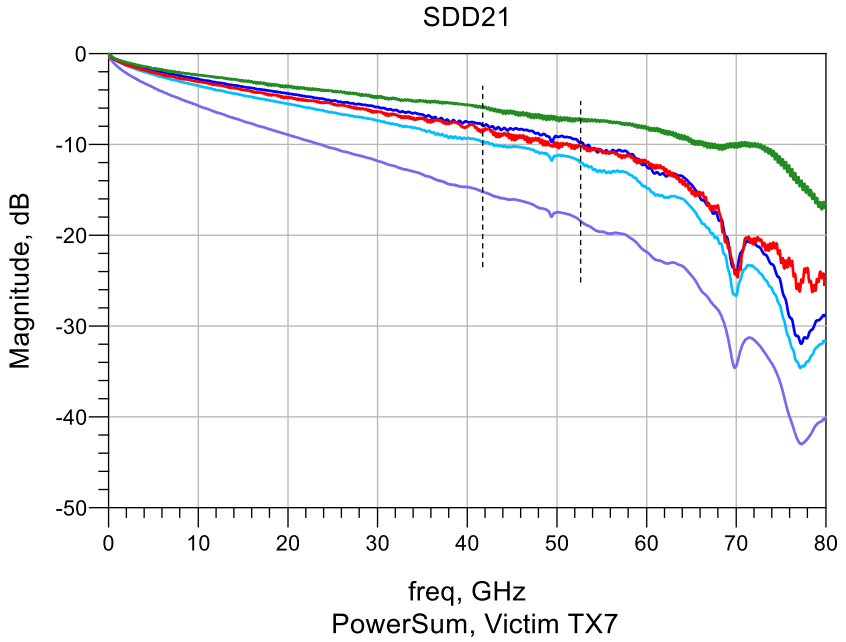
- OSFP OTB 200G Connector
- Cable Termination to OTB Connector
- 10”, 30AWG Cable
- Cable termination to NCC connector
- NCC connector
- NCC transition via and breakout traces, ~3.3mm via, ~6mil stub
- Host Traces, 50mm long [5.8mil wide], ~1.08dB/in loss at 53.125GHz
- Module Traces, 2” long [5.8mil wide], ~1.08dB/in loss at 53.125GHz
- BGA footprint + breakout

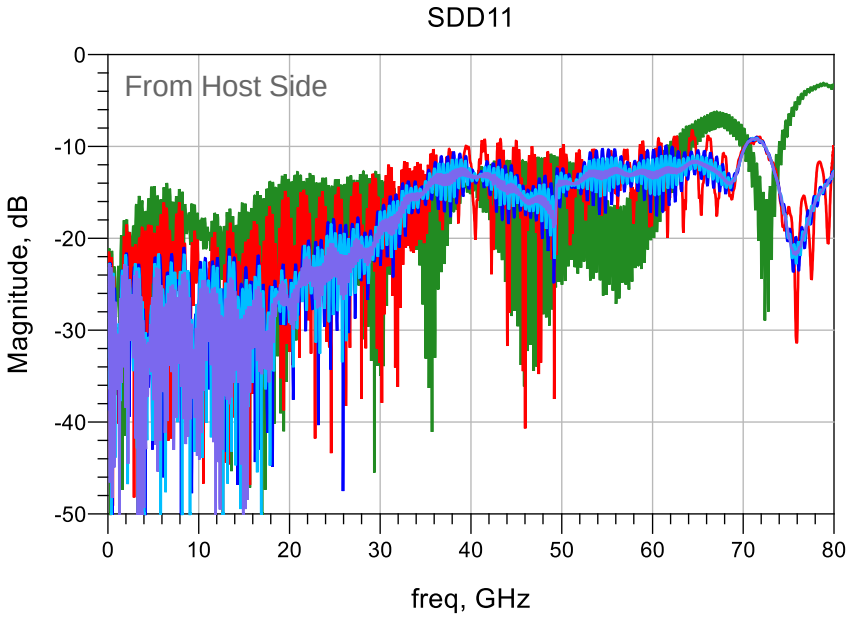
CoPackage Copper [CPC] Host

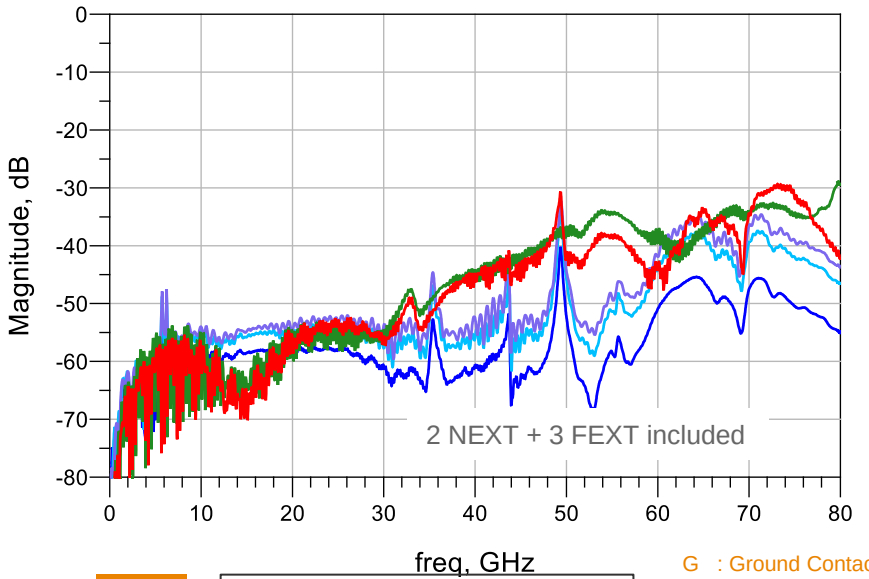


- OSFP OTB 200G Connector
- Cable Termination to OTB Connector
- 10”, 30AWG Cable
- Cable termination to CPC Socket
- CPC Socket
- CPC transition, ~3.3mm via, ~6mil stub
- Module Traces, 2” long [5.8mil wide], ~1.08dB/in loss at 53.125GHz
- Does NOT include package routing

Performance Comparison



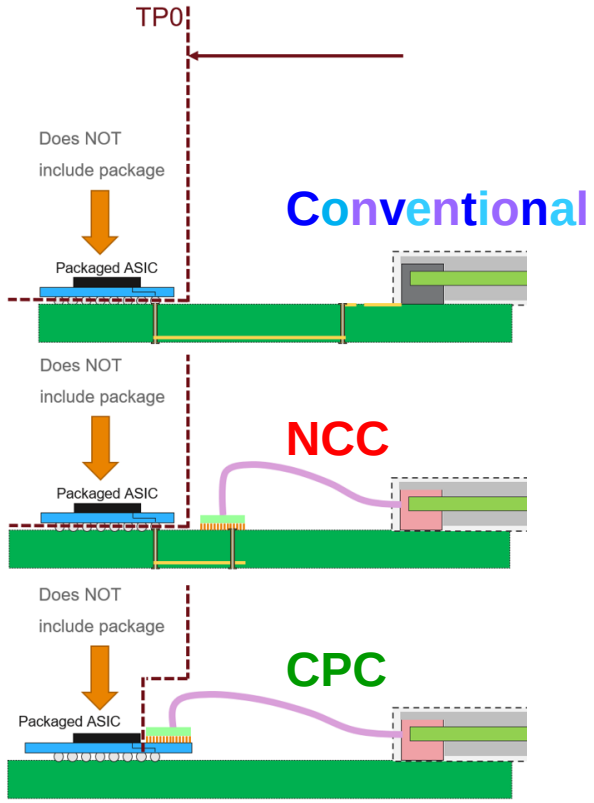




G S S G L L L L G S S G S S G
G S S G L L L L G S S G S S G

G : Ground Contact
S : High Speed Contact
L : Low Speed Contact
: Victim Pair

	TP0 – TP1a IL, dB @42.5GHz	TP0 – TP1a IL, dB @53.125GHz
Conv. 13”	15.5	18.8
Conv. 7”	10	12.4
Conv. 5”	8.1	10.3
NCC	8.3	10.4
CPC	6.1	7.3



Summary

- Simulation results have been provided for 224G channels consisting of:
  - OSFP 224G concept connector, Both conventional SMT and cabled OTB versions
  - Host connector footprint and via
  - 5, 7 and 13 inches of host trace
  - 10 inches of OTB internal cable assembly to NCC host connector
  - 10 inches of OTB internal cable assembly to CPC socket
  - BGA footprint and breakout model
- Not a final position on component or channel performance, further development is in process
- Intent is to provide meaningful input for OIF 224G CEI architecture discussions
- A range of host implementation architectures/technologies may be useful to enable 224G based systems
  - Internal cables (OTB) can provide meaningful channel improvement and reach