802.3df D1.1
Comment Resolution

P802.3df editorial team
Introduction

- This slide package is put together by the 802.3df editorial team to provide background and detailed resolutions to aid in comment resolution.
Clause 167
Fiber optics cabling
Comments 13, 14, 116 (part 1)

- Three comments were received highlighting issues with the clause 167 “Characteristics of the fiber optic cabling and MDI” PICS table
  - Comments 13, 14, and 116
## Fiber optics cabling

**Comments 13, 14, 116 (part 2)**

### D1.1 167.11.4.6 PICS Table

<table>
<thead>
<tr>
<th>Item</th>
<th>Feature</th>
<th>Subclause</th>
<th>Value/Comment</th>
<th>Status</th>
<th>Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC5</td>
<td>MDI layout for 40GIGBASE-X4 and 40GIGBASE-SR4</td>
<td>167.10.3.1 a</td>
<td>Optical link assignments per Figure 167-8</td>
<td>VBR,</td>
<td>N/A</td>
</tr>
<tr>
<td>OC5a</td>
<td>MDI layout for 100GIGBASE-X4 and 100GIGBASE-SR4 option A</td>
<td>167.10.3.1 a</td>
<td>Optical link assignments per Figure 167-8a</td>
<td>VBR,</td>
<td>N/A</td>
</tr>
<tr>
<td>OC5b</td>
<td>MDI layout for 100GIGBASE-X4 and 100GIGBASE-SR4 option B</td>
<td>167.10.3.1 a</td>
<td>Optical link assignments per Figure 167-8a</td>
<td>VBR,</td>
<td>N/A</td>
</tr>
<tr>
<td>OC6</td>
<td>MDI mating, 100GIGBASE-X1 and 100GIGBASE-SR1, with single optical fiber connector</td>
<td>167.10.3.2</td>
<td>MDI optically muting with plug on the cabling, performance grade Bun/2m</td>
<td>VBR1</td>
<td>N/A</td>
</tr>
</tbody>
</table>

| OC15 | MDI requirements, with multifiber connector | 167.10.3.3 | Per IEC 6126-1, performance grade Bun/1m | INS and VBR, SR1, SR2, V6, or Sr6+AF1M | N/A |
| OC16 | MDI mating, with multifiber connector | 167.10.3.4 | MDI optically muting with plug on the cabling, performance grade Bun/2m | VBR, | N/A | SR6+AF1M |
| OC17 | MDI dimensions, with multifiber connector | 167.10.3.4 | Per IEC 61754-7:1, interface 7-1:1-3 or interface 7-5:1:10 | VBR, | N/A | SR6+AF1M |
| OC18 | MDI dimensions, with multifiber connector | 167.10.3.4 | Per IEC 61754:7-2 interfaces 7-2:3 or 7-2:10, or per ANSI/IEEE 608:10-A designation FOCIS 18 A-1-9 or FOCIS 18 Btxt0-1-9:1-2:9 | VBR, | N/A | SR6+AF1M |
| OC19 | Cabling connector, dimensions, with multifiber connector | 167.10.3.4 | Per IEC 61754-7:2 interface 7-2-4 or ANSI/IEEE 608:c-L-A designation FOCIS 18 Btxt16-1-0-2:2:0 | INS+VBR | N/A | SR6+AF1M |
| OC20 | MDI requirements, with multifiber connector | 167.10.3.4 | Per IEC 61754-1 and IEC 61755-822-2, performance grade Bun/2m | INS+VBR | N/A | SR6+AF1M |

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January 30, 2023

IEEE P802.3df Task Force, January 2023
## Fiber optics cabling

Comments 13, 14, 116 (part 3)

**Proposed D1.2 167.11.4.6 PICS Table**

<table>
<thead>
<tr>
<th>Item</th>
<th>Feature</th>
<th>Subclause</th>
<th>Value/Comment</th>
<th>Status</th>
<th>Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC1</td>
<td>MDI layout for 400GBASE-VR4 and 400GBASE-SR4</td>
<td>167.10.3.1</td>
<td>Optical line assignments per Figure 167-8</td>
<td>(VR4 or SR4)M</td>
<td>Yes</td>
</tr>
<tr>
<td>OC2</td>
<td>MDI layout for 100GBASE-VR8 and 100GBASE-SR8, option A</td>
<td>167.10.3.1a</td>
<td>Optical line assignments per Figure 167-8a</td>
<td>(VR8 or SR8)M</td>
<td>Yes</td>
</tr>
<tr>
<td>OC3</td>
<td>MDI layout for 100GBASE-VR8 and 100GBASE-SR8, option B</td>
<td>167.10.3.1a</td>
<td>Optical line assignments per Figure 167-8a</td>
<td>(VR8 or SR8)M</td>
<td>Yes</td>
</tr>
<tr>
<td>OC4</td>
<td>MDI mating, 100GBASE-VR1 and 100GBASE-SR1, with duplex optical fiber connector</td>
<td>167.10.3.2</td>
<td>MDI optically mates with plug on the cabling, performance grade Brun2m</td>
<td>(VR1 or SR1)M</td>
<td>Yes</td>
</tr>
<tr>
<td>OC5</td>
<td>MDI requirements, with multimode connector</td>
<td>167.10.3.3</td>
<td>Per IEC 61267-1, performance grade Brun1m</td>
<td>INS and (VR1, SR1, VR2, SR2, VR4, or SR4)AFM</td>
<td>Yes</td>
</tr>
<tr>
<td>OC6</td>
<td>MDI mating, with multimode connector</td>
<td>167.10.3.4</td>
<td>MDI optically mates with plug on the cabling, performance grade Brun2m</td>
<td>(VR8 or SR8)AFM</td>
<td>Yes</td>
</tr>
<tr>
<td>OC7</td>
<td>MDI mating, with multimode connector</td>
<td>167.10.3.4</td>
<td>MDI optically mates with plug on the cabling, performance grade Brun2m</td>
<td>(VR8 or SR8)AFM</td>
<td>Yes</td>
</tr>
<tr>
<td>OC8</td>
<td>MDI dimensions, with multimode connector</td>
<td>167.10.3.4</td>
<td>Per IEC 61754-5-2 interface 7-3 or interface 7-2-2b</td>
<td>(VR8 or SR8)AFM</td>
<td>Yes</td>
</tr>
<tr>
<td>OC9</td>
<td>MDI dimensions, with multimode connector</td>
<td>167.10.3.4</td>
<td>Per IEC 61754-5-4 interface 7-4 or interface 7-4-4b</td>
<td>(VR8 or SR8)AFM</td>
<td>Yes</td>
</tr>
<tr>
<td>OC10</td>
<td>Cabging connector dimensions, with multimode connector</td>
<td>167.10.3.4</td>
<td>Per IEC 61754-5-2 interface 5-2-4</td>
<td>INS and (VR8 or SR8)AFM</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Item | Feature | Subclause | Value/Comment | Status | Support**
--- | --- | --- | --- | --- | ---
OC21 | Cabling connector dimensions, with multimode connector | 167.10.3.4 | Per IEC 61754-7-4 interface 7-4-4 | INS and (VR8 or SR8)AFM | Yes | N/A |
OC22 | Cabling connector dimensions, with multimode connector | 167.10.3.4 | Per IEC 61754-7-4 and IEC 61754-7-6, performance grade Brun2m | INS and (VR8 or SR8)AFM | Yes | N/A |
OC23 | Cabling connector dimensions, with multimode connector | 167.10.3.4 | Per IEC 61754-7-1, performance grade Brun1m | INS and (VR8 or SR8)AFM | Yes | N/A |
Fiber optics cabling
Comments 13, 14, 116 (part 4)

Proposed D1.2 PICS Table Updates

- The value/comments of OC16 through OC23 now align with the updated text in 167.10.3.4
- The use of !AFI for flat connectors and AFI for angled connectors is consistent with 802.3db-2022

<table>
<thead>
<tr>
<th>OC14</th>
<th>MDI requirements, with multifiber connector</th>
<th>167.10.3.3</th>
<th>Per IEC 61753-1 and IEC 61753-022-2, performance grade Bm/2m</th>
<th>INS and (VR1, SR1, VR2, SR2, VR4, or SR4)!AFI/M</th>
<th>Yes [ ]</th>
<th>N/A [ ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC15</td>
<td>MDI requirements, with multifiber connector</td>
<td>167.10.3.3</td>
<td>Per IEC 63267-1, performance grade Bm/1m</td>
<td>INS and (VR1, SR1, VR2, SR2, VR4, or SR4)!AFI/M</td>
<td>Yes [ ]</td>
<td>N/A [ ]</td>
</tr>
</tbody>
</table>

- The resolution of comment #115 could affect the final PICS table
Clause 173
PCSL Grouping
Comment #84

Adapt the PCSL (PCS lane) formatted signal to the appropriate number of abstract or physical lanes

Adapt the PCSL (PCS lane) formatted signal to the appropriate number and grouping of abstract or physical lanes

PROPOSED ACCEPT IN PRINCIPLE.
The constrained grouping of lanes is part of the "adapt" process and does not need to be listed as a detail here. Instead, this detail is specified in 173.4. The proposed change is not necessary.
However, the acronym PCSL is not properly introduced in this clause. Change "PCSL (PCS lane)" to "PCS lane (PCS lane)."

173.1.3 Summary of functions

- Adapt the PCSL (PCS lane) formatted signal to the appropriate number of abstract or physical lanes
- Provide per input lane clock and data recovery
- Provide bit-level multiplexing
PSCS Grouping
Comment #87 (part 1)

Figure 173-3 32:8 PMA
(PMA Clause)

Figure 172-2
(PCS Clause)
PCSL Grouping - Comment #87 (part 2)

Existing Figure 173-3 (PMA 32:8)

Proposed Figure 173-3 (PMA 32:8)
173.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

- Adapt the PCSL (PCS lane) formatted signal to the appropriate number of abstract or physical lanes
- Provide per-input-lane clock and data recovery
- Provide bit-level multiplexing
- Provide clock generation
- Provide signal drivers
- Optionally provide local loopback to/from the PMA service interface
- Optionally provide remote loopback to/from the PMD service interface
- Optionally provide test-pattern generation and detection
- Tolerate Skew Variation
- Perform PAM4 encoding and decoding

PROPOSED REJECT.

The opening sentence in 173.1.3 states “The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions.” The phrase “when required” implies that some of the functions listed are conditional upon the PMA type. The requirement for each of the functions listed is specified per PMA type in 173.4.
Clause 172
Test pattern control
Comment #79 (part 1)

The assignment of bits in the BASE-R PCS test-pattern control register is shown in Table 45–248. This register is only required when the BASE-R capability is supported. If both BASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for BASE-R. PRBS9, PRBS31, pseudo random, and square wave test patterns are defined for 10GBASE-E only. Scrambled idle test patterns are defined for 25/40/50/100/200/400GBase-R-PCS only. The test-pattern methodology is described in 49.2.8 and 82.2.11.

172.2.4.9 Test-pattern generators

The PCS shall have the ability to generate a scrambled idle test pattern, which is suitable for receiver tests and for certain transmitter tests. When a scrambled idle pattern is enabled, the test pattern is generated by the PCS. The scrambled idle test pattern is the output of the PCS when the input to the PCS at the 800GMI is a control block with all idle characters.

If a Clause 45 MDIO is implemented, then control of the test-pattern generation is from the BASE-R PCS test-pattern control register (bit 3.42.3).

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.42.1</td>
<td>Transmit-test-pattern enable</td>
<td>1 = Enable transmit test pattern; 0 = Disable</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>transmit test pattern</td>
<td></td>
</tr>
<tr>
<td>3.42.2</td>
<td>Receive-test-pattern enable</td>
<td>1 = Enable receive test-pattern; 0 = Disable</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>receive test-pattern test</td>
<td></td>
</tr>
<tr>
<td>3.42.3</td>
<td>Data pattern select</td>
<td>1 = Square wave test pattern; 0 = Pseudo random</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>test pattern</td>
<td></td>
</tr>
<tr>
<td>3.42.4</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Test pattern control
Comment #79 (part 2)

Proposed changes...

In 45.2.3.19, with appropriate editing instructions amend the last sentence in the first paragraph to:
"Scrambled idle test patterns are defined for 25/40/50/100/200/400/800GBASE-R PCS only. The test-pattern methodology is described in 49.2.8, 82.2.11, and 172.2.4.9."

Change 172.2.4.9 as follows:

172.2.4.9 Test-pattern generators
The PCS shall have the ability to generate a scrambled idle test pattern, which is suitable for receiver tests and for certain transmitter tests. When test pattern generation of a scrambled idle pattern is enabled (tx_test_mode is 1), the scrambled idle test pattern is generated by the PCS. The scrambled idle test pattern is the output of the PCS when the input to the PCS at the 800GMII is a control block with all idle characters. If a Clause 45 MDIO is implemented, then control of the test-pattern generation is from the BASE-R PCS test-pattern control register (bit 3.42.3) the tx_test_mode variable is accessible through the register as shown in Table 172-5.
## Stateless encoder / decoder

### Comments #20, 24

### Existing tables

#### Table 172-1—PCS stateless encoder rules

<table>
<thead>
<tr>
<th>Byte</th>
<th>T_TYPE (in_raw)</th>
<th>T_TYPE (in_coded)</th>
<th>Resulting_t_coded</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>any block type</td>
<td>any block type</td>
<td>LBLOCK_T</td>
</tr>
<tr>
<td>0</td>
<td>C + T</td>
<td>S</td>
<td>ENCODE (in_coded)</td>
</tr>
<tr>
<td>0</td>
<td>S + D</td>
<td>T</td>
<td>ENCODE (in_coded)</td>
</tr>
<tr>
<td>0</td>
<td>C + T</td>
<td>C</td>
<td>ENCODE (in_coded)</td>
</tr>
<tr>
<td>0</td>
<td>any combination not listed above</td>
<td></td>
<td>EBLOCK_T</td>
</tr>
</tbody>
</table>

### Suggested remedy

Add the following row to the table:

| 0 | any combination not listed above | S or C | ENCODE (in_coded) |

#### Table 172-4—PCS stateless decoder rules

<table>
<thead>
<tr>
<th>Byte</th>
<th>R_TYPE (in_coded)</th>
<th>Resulting_rx_crd</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>any block type</td>
<td>LBLOCK_R</td>
</tr>
<tr>
<td>0</td>
<td>any block type</td>
<td>EBLOCK_R</td>
</tr>
<tr>
<td>0</td>
<td>any block type</td>
<td>EBLOCK_R</td>
</tr>
<tr>
<td>0</td>
<td>any combination not listed above</td>
<td>DECODE (in_coded)</td>
</tr>
</tbody>
</table>

### Suggested remedy

- Change the third row to:
  
  "0 | E | any block type | EBLOCK_R"

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January 30, 2023

IEEE P802.3df Task Force, January 2023
Cross-Clause
FEC Degrade
Comments 17, [55, 56], 59

Consensus View on how FEC degrade signaling should work
OTN mapper contribution to FEC degrade signaling is for ITU to decide, but LD, RD must be propagated whether or not the FEC decoder in the OTN mapper contributes to the accumulated LD status

- FEC degrade signals should be retained.
- FEC degrade signal can propagate through OTN network.
- Both FEC degrade signals and FEC bin counters can be used to determine the link quality.

Multiplexing rules
Comments [27, 89, 92] - (part 1)

- Three comments were received proposing additional PMA multiplexing constraints beyond what was agreed to in the adopted baseline: https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf

- Comment #6 against Draft 1.0 made a similar proposal. Straw polls recorded in the response to comment #6 indicated favor for adopting the proposal, but there were many votes for “need more information” and more consensus building was clearly necessary.

- Adee has a new presentation (ran_3df_01a_230130.pdf) which provides more information on the problem (hopefully responding to some of those that voted “needs more information” on the previous straw poll), but essentially proposes the same remedy (but with minor editorial updates).
Multiplexing rules
Comments [27, 89, 92] - (part 2)

- Below is the final response to D1.0 comment #6, including the results of the straw poll.

**REJECT.**

The current text and constrained PCSL multiplexing requirement is consistent with the adopted baseline (see slides 17&18 in https://www.ieee802.org/3/df/public/22_10/22_1004/shrikhande_3df_01a_221004.pdf).

The following presentation was reviewed by the task force: https://www.ieee802.org/3/df/public/22_12/ran_3df_01a_2212.pdf

Based on straw polls #1 and #2 there is no consensus to make the proposed changes at this time. The commenter is encouraged to refine the proposal and build consensus.

**Straw poll #1 (direction)**
I would support the changes proposed on slides 10 in ran_3df_01a_2212.
Yes: 19
No: 6
Need more information: 27

**Straw poll #2 (direction)**
I would support the changes proposed on slides 11 in ran_3df_01a_2212.
Yes: 13
No: 6
Need more information: 33

**Suggested remedy (modified) – part 1**

173.4.2.1 32:8 PMA bit-level multiplexing
Change the second list item as shown:

- The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from PMA client lanes \( i = 0 \) to 15 and followed by two unique PCSLs from PMA client lanes \( i = 16 \) to 31.

173.4.2.2 8:32 PMA bit-level multiplexing
Change the second list item as shown:

- The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from service interface lanes \( i = 0 \) to 15 and followed by two unique PCSLs from service interface lanes \( i = 16 \) to 31.

**Suggested remedy (modified) – part 2**

173.4.2.3 8:8 PMA bit-level multiplexing
Change the second list item as shown:

- The 4 PCSLs received on any input lane shall be mapped together to an output lane such that the Gray-coded PAM4 symbol sequence on the output is identical to the Gray-coded PAM4 symbol sequence on the input (see 173.4.7.1). The order of PCSLs from an input lane does not have to be maintained on the output lane.
Comment #27 suggested remedy

173.4.2.1 32:8 PMA bit-level multiplexing

Change the second list item as shown:

– The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from PMA client lanes $i = 0$ to 15 and followed by two unique PCSLs from PMA client lanes $i = 16$ to 31.

173.4.2.2 8:32 PMA bit-level multiplexing

Change the second list item as shown:

– The multiplexing function has an additional constraint that each of the 8 output lanes contain two unique PCSLs from service interface lanes $i = 0$ to 15 and followed by two unique PCSLs from service interface lanes $i = 16$ to 31.

173.4.2.3 8:8 PMA bit-level multiplexing

Change the second list item as shown:

– The 4 PCSLs received on any input lane shall be mapped to the same output lane such that the Gray-coded PAM4 symbol sequence on the output lane is identical to the Gray-coded PAM4 symbol sequence on the input lane, except for possible swapping of each bit pair (see 173.4.7.1). The order of PCSLs from an input lane does not have to be maintained on the output lane.
Multiplexing rules
Comments [27, 89, 92] - (part 3 - backup)

PAM4 Retimer options (Today - Clause 120)

Ref: 802.3 120.5.7.1
For input lanes encoded as PAM4 (for 200GBase-R, where the number of input lanes is 4, or for 400GBase-R, where the number of input lanes is 4 or 8), the PMA receive process shall map Gray-coded PAM4 symbols to pairs of bits [A, B], where A is considered to be the first bit as follows:

- 0 maps to (0, 0),
- 1 maps to (0, 1),
- 2 maps to (1, 1), and
- 3 maps to (1, 0).

Ref: 802.3 120.5.7.1
For output lanes encoded as PAM4 (for 200GBase-R, where the number of output lanes is 4, or for 400GBase-R, where the number of output lanes is 4 or 8), the PMA transmit process shall map consecutive pairs of bits [A, B], where A is the bit arriving first, to a Gray-coded symbol as follows:

- (0, 0) maps to 0,
- (0, 1) maps to 1,
- (1, 1) maps to 2, and
- (1, 0) maps to 3.

- Appears to be no requirement for LSB/MSB alignment between PAM4 decoder on input and PAM4 encoder on output
- Depending on how the PAM4 encoder samples the internal bit stream there could be a LSB/MSB swap on output port
- Note, in the encoder description above “A” is simply defined as the first bit arriving at the encoder (independent of whether it was the first bit output from decoder or not)
Multiplexing rules
Comments [27, 89, 92] - (part 4 - backup)

PAM4 Retimer (Adee’s proposal)

- In this case the PAM4 encoder is required to be “LSB/MSB locked (aligned)” to the PAM4 decoder
- Output PAM4 symbol stream is always the same as the input PAM4 symbol stream (assuming no errors)
- Note, how LSB/MSB aligned is achieved is an implementation choice (there are many possible options)
  - Including having a wide internal bus that is always LSB/MSB aligned (both at decoder and encoder)