200G/Lane AUI FEC Proposal

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Logic ad hoc

Mark Gustlin – Cisco

Introduction

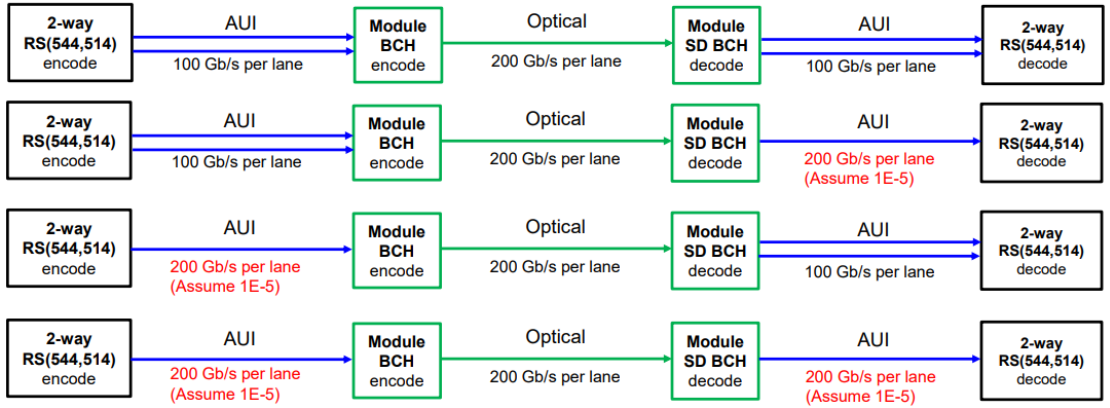
- I think we could quickly adopt the FEC code for 200G/lanes, at least for the AUI interfaces
  - As a stake in the ground
- This explores an option to adopt the AUI FEC, leaving the optical span for further study

Starting Place for 200G/Lane FEC

- We should propose an initial FEC code, fill out the details, and then see if it stands the test of time/analysis
- Several presentations have proposed to reuse the RS544 from previous projects (to list a couple of the presentations):

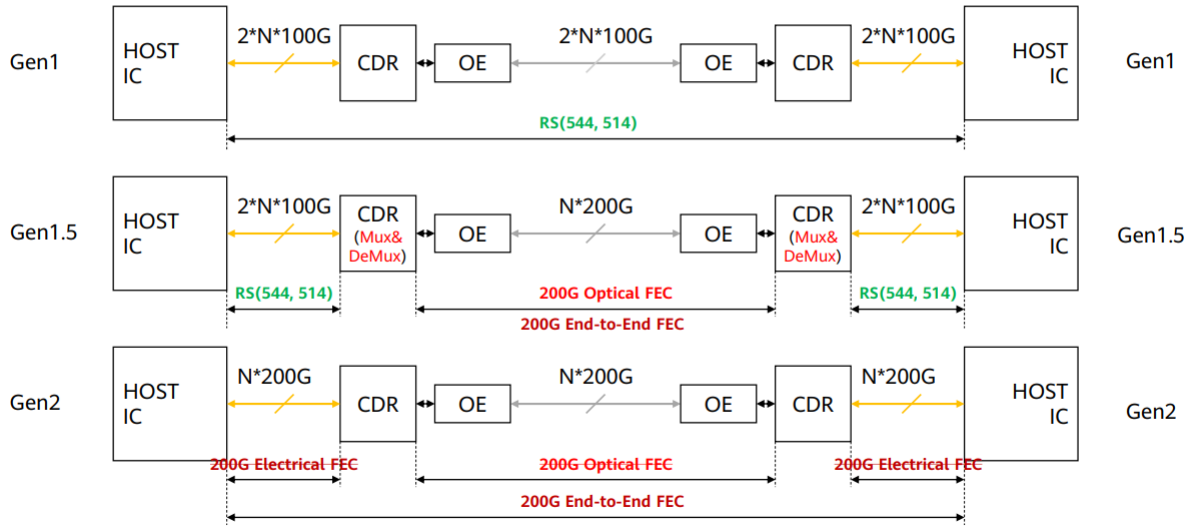
FEC Scheme Example with Concatenated FEC Code

- Assuming 200 Gb/s per lane AUI has similar BER (~1E-5) and error behavior as 100 Gb/s per lane AUI, it will make FEC scheme simple, just doubling the bit rate.
- Assuming 200 Gb/s per lane optical link operates at ~2E-3, the inner code can help to lower this raw BER to match the far end outer decode RS(544,514) performance.
  - This inner code has a short codeword, operating on a per-lane style to enable simple FEC scheme conversion.



wang_3df_01_220215.pdf

FEC architectures for 800GbE/1.6TbE



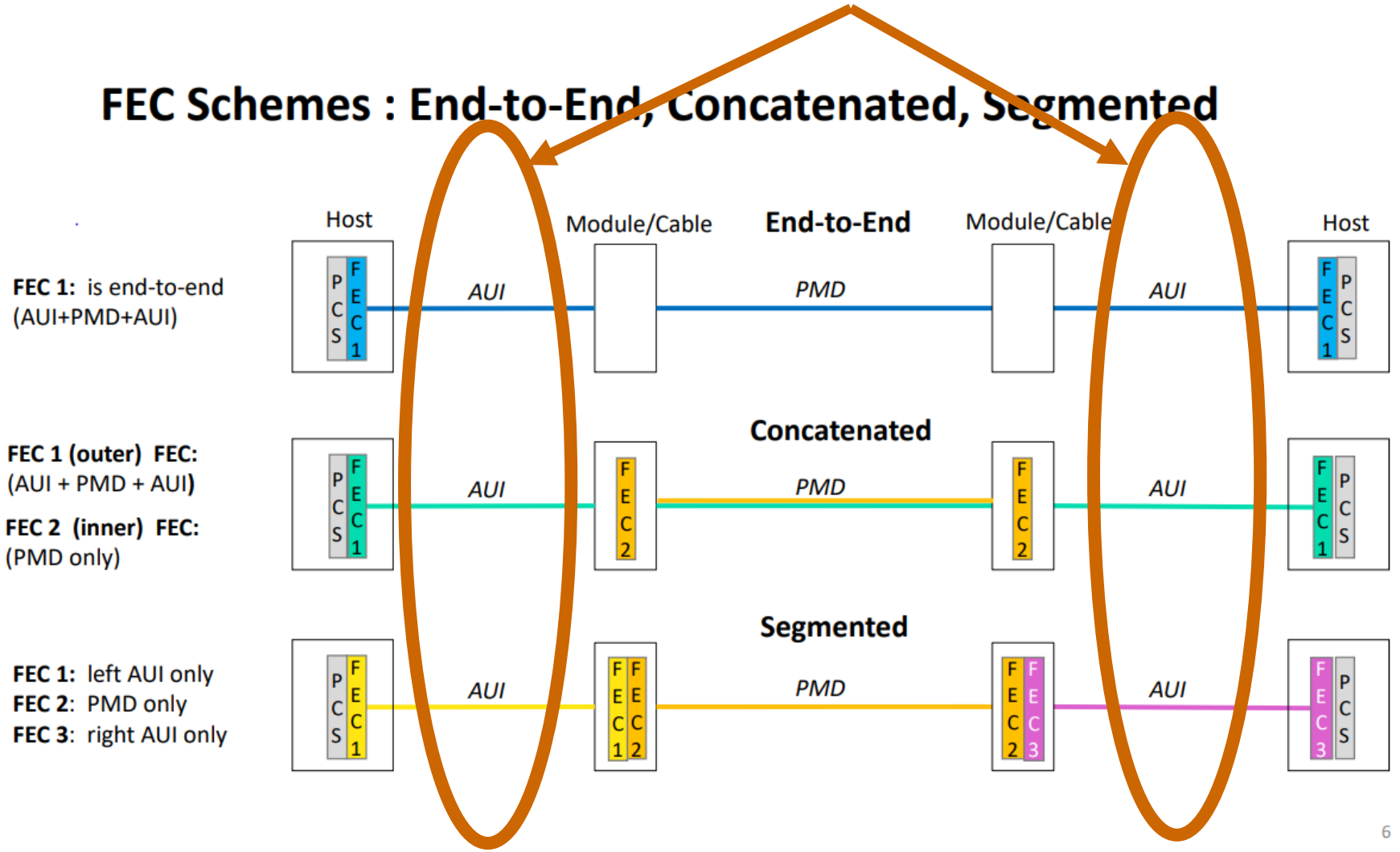
lu_3df_01b_220215.pdf

Proposal: Adopt RS544 FEC in the Large ASIC for 200G/lane

- Great reuse from today's ASICs
- RS544 is very likely to be able to support at least the 200G/Lane AUI(s) on one side of the module
- If we adopt this, the options going forward will be:
  1. Use the RS544 end to end as suggested in lu_3df_01b_220215, by applying increased equalization; MLSE, DFE, FFE etc.
  2. Use RS544 in a segmented mode, optical span has its own TBD FEC; RS544 FEC per AUI
  3. Use RS544 in a concatenated mode, RS544 FEC covers AUIs on both side, added FEC for the optical span as needed

Location of RS544 FEC

Use RS(544,514,10) for the AUIs, for both 200G/lane and 100G/lane



From: shrikhande_3df_01a_220203.pdf

Raw BER That Can be Supported

- Analysis needs to be done
- Assumptions need to be made, details matter
- To the right is some work from Pete Anslow in the 802.3bs task force
  - Degree of muxing matters
  - Do we have precoding
  - Burst error assumptions matter
  - Etc…

Results for RS(544,514) 50G, all gain used for PAM4

For reference, if all of the coding gain were to be used for the 50G PAM4 link, the BERs at the slicer output and FEC input required to give FLRs equivalent to that of a BER of 1E-13 and 1E-15 are:

	At slicer output		At FEC input	
	FLR = 6.2E-11	FLR = 6.2E-13	FLR = 6.2E-11	FLR = 6.2E-13
No FEC	1E-13	1E-15	1E-13	1E-15
Same cwd (1), a = 0.75			7.6E-6*	1.6E-7*
Same cwd, symb inter (2), a = 0.75			2E-5*	4.9E-7*
Same cwd (1), a = 0.5			9E-5*	3.9E-5*
1:4 Pre-interleaved (4), a=0.75			1.1E-4*	5.5E-5*
1:2 Pre-interleaved (8), a=0.75			1.8E-4*	8.6E-5*
Diff cwd (FOM) (7), a = 0.75			1.9E-4*	1E-4*
Same cwd precoded, a=0.75	2.3E-4*	1.3E-4*	1.1E-4	6.3E-5
1:4 Pre-interleaved (6), a=0.75			2.5E-4*	1.5E-4*
1:2 Pre-int, sym mux (10), a=0.75			3.5E-4*	1.9E-4*
1:4 Pre-int, sym mux (9), a=0.75			4.2E-4*	2.6E-4*
Random errors			3.2E-4	2.3E-4

Note – these values are the BER **including** the additional errors due to the bursts. To account for burst errors, the values marked with "*" have been multiplied by 4 when a = 0.75 and 2 when a = 0.5.

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From: https://www.ieee802.org/3/bs/public/15_09/anslow_3bs_03_0915.pdf

Adopt RS544 FEC in the Large ASIC for 200G/lane

- Reasons **to** do this soon:
  - Gives guidance to the industry for developing large ASICs
  - RS544 FEC is very likely to be able to support at least one AUI and is therefore viable for at least one segment
  - Fully evaluating the raw BER targets for optical and electrical links is a long pole, but giving a good target to the task force to coalesce around is valuable
  - We don’t want a higher overhead FEC on the AUI anyhow, impact on NCG due to speed increases reaches diminishing returns
  - Having a common RS(544,514,10) strategy across 100G/Lane for all interfaces (AUIs and PMDs) and for the AUIs for 200G/Lane is a big benefit

- Reasons **not** to do this soon:
  - What if it does not work? Then we adjust…
  - It does not address the FEC requirement for CR links (but we don’t know those are at this point)

Architectural Details

Architecture Details

- If we went down this path, what is the architecture for each speed??

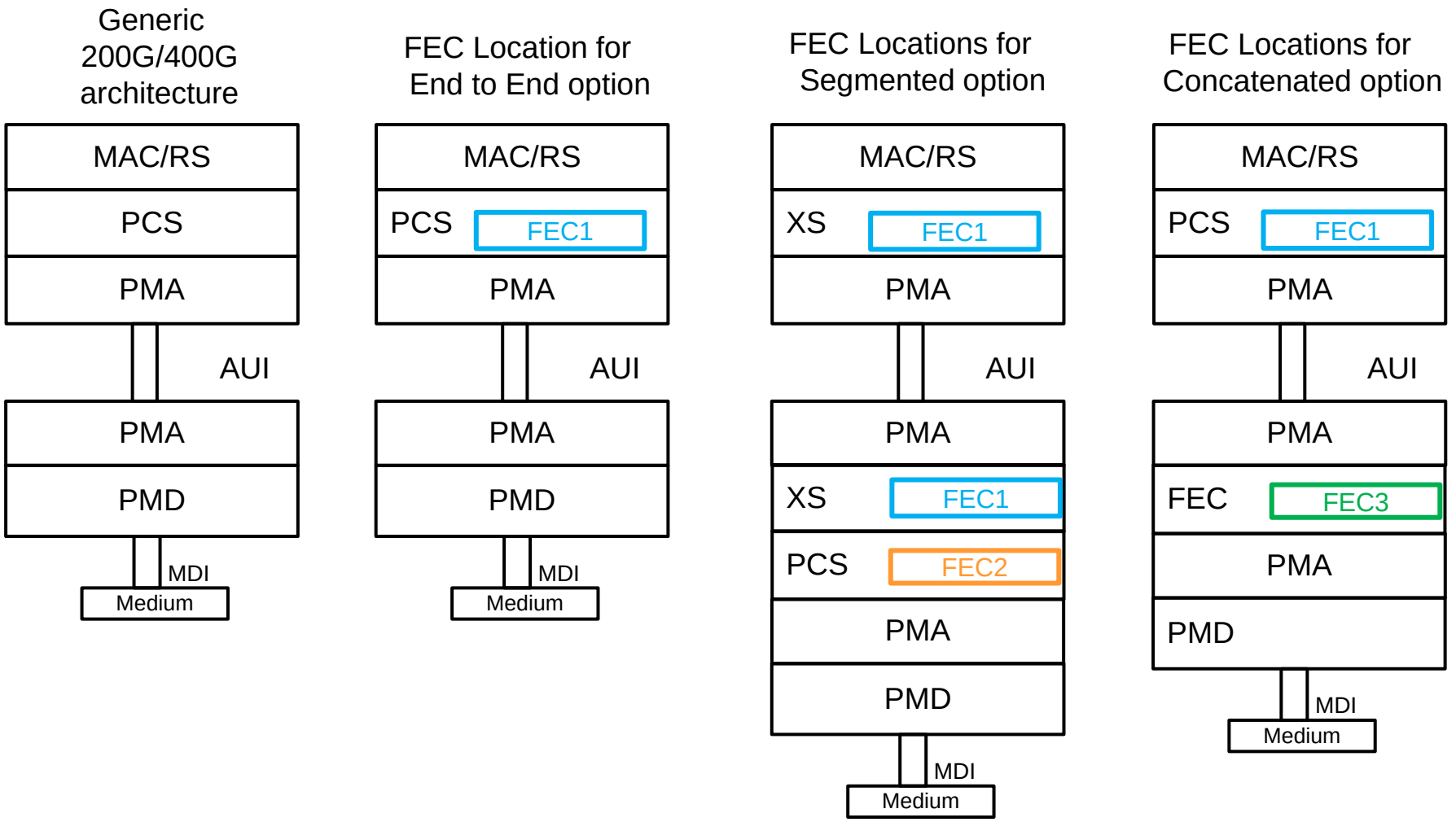
200GbE/400GbE Architecture

- How 200G/Lane FEC options fit into the architecture

FEC1 = RS544 FEC as in clause 119

FEC2 = New FEC, TBD, if needed

FEC3 = New FEC, TBD, if needed



200GbE/400GbE Details for Above the AUI

- Reuse clause 118/119 (XS/PCS) as is
- 200GbE: 8 PCS lanes, 8:1 bit muxing to get to 200G lanes
- 400GbE: 16 PCS lanes, 8:1 bit muxing to get to 200G lanes
- Slight changes to the PMA (Clause 120)
- Need to study clock content, burst error impact etc.
- Could use precoding to reduce burst error impacts

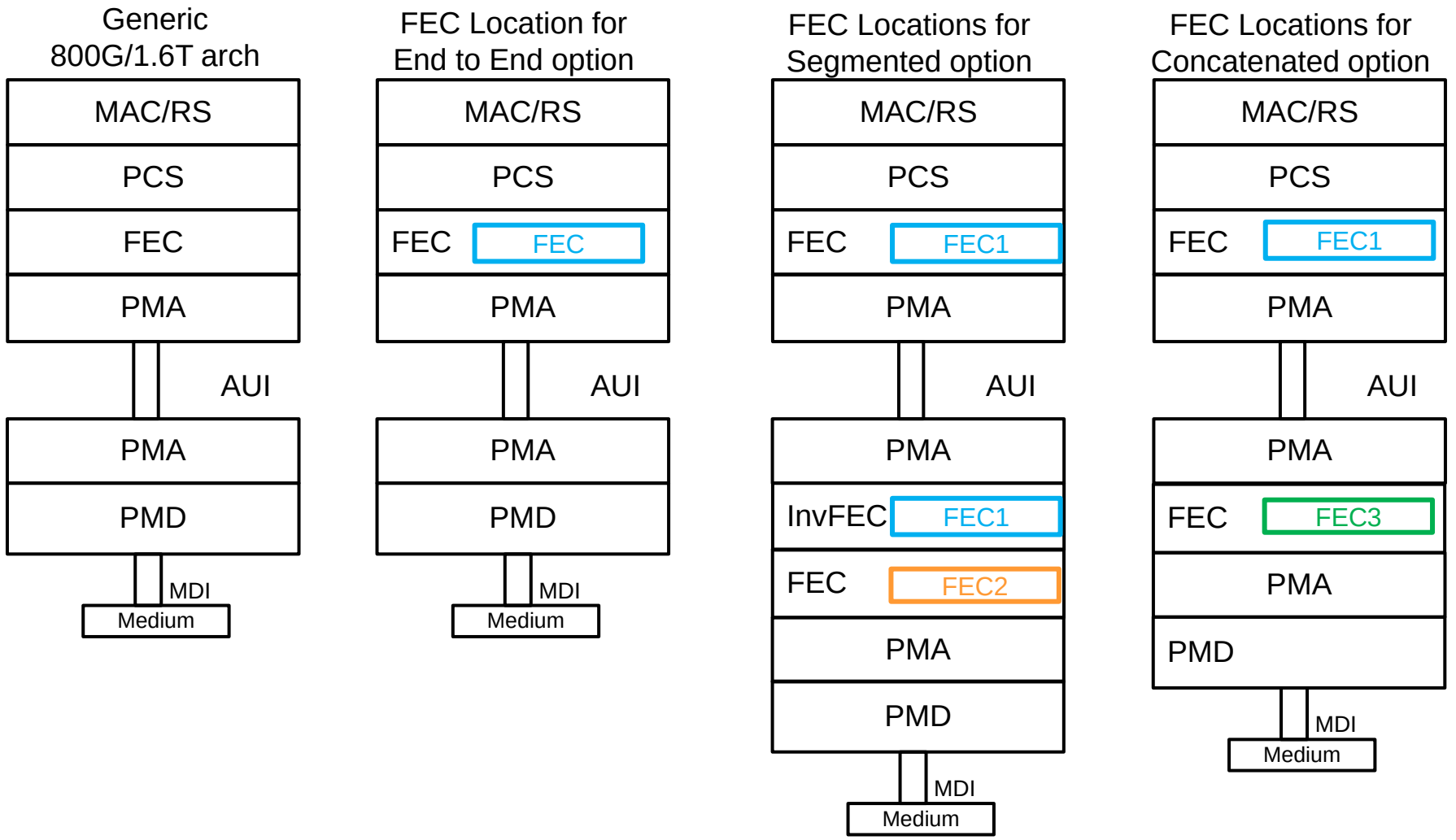
800GbE/1.6TbE Architecture

- How 200G/Lane FEC options fit into the architecture

FEC1 = RS544 FEC as in clause 119

FEC2 = New FEC, TBD, if needed

FEC3 = New FEC, TBD, if needed



800GbE Details for Above the AUI

- Two options:
  - 2xParallel 119 clauses as in shrikhande_3df_01_220329.pdf
    - 32 FEC lanes, 8:1 bit muxing to get to 200G lanes
  - Sped up clause 119 as in wang_b400g_01_210208.pdf
    - 8 or 16 FEC lanes, 2:1 or 4:1 bit muxing to get to 200G lanes
    - 16 FEC lanes if we want 50G lane support
  - RS544 FEC strategy should be the same as the 100G/lane strategy
- PMA similar to Clause 120
- Need to study clock content, burst error impact etc.
- Could use precoding to reduce burst error impacts

1.6TbE Details

- Options:
  - 4xParallel 119 clauses, an extension of shrikhande_3df_01_220329.pdf
    - 16 FEC lanes, 2:1 bit muxing to get to 200G lanes
  - Sped up clause 119 as in wang_b400g_01_210208.pdf
    - 16 FEC lanes, 2:1 bit muxing to get to 200G lanes
  - Other choices??
- PMA similar to Clause 120

Conclusion

- We should soon adopt the FEC code for 200G/lanes at least for the AUI interfaces
  - Reusing RS(544,514,10)
  - Some details still to be worked out for 800GbE
  - At least as a stake in the ground
  - We can validate the choice over time, fill in the optical span details etc.

Thanks!