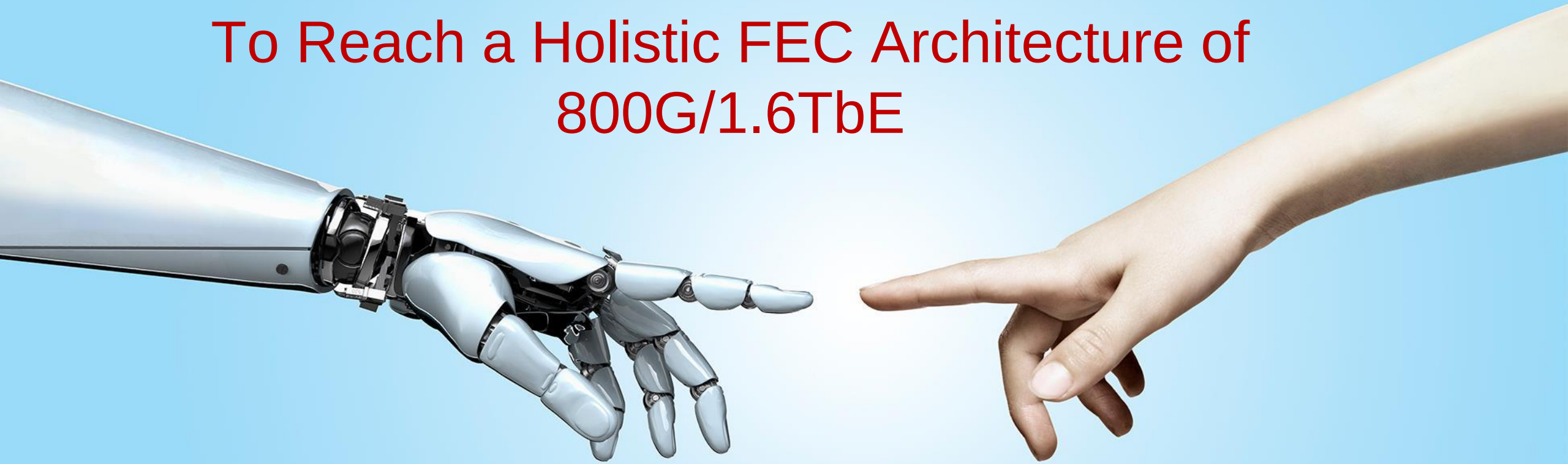
To Reach a Holistic FEC Architecture of 800G/1.6TbE



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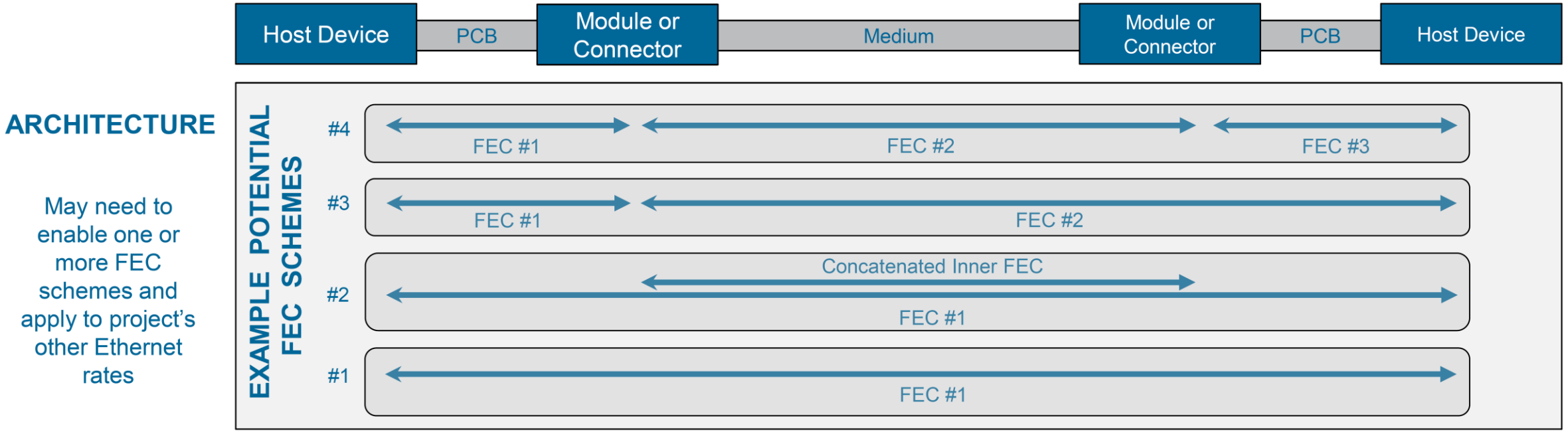
Expectation:

- Overview at the end of study group:
  - "An initial holistic approach to start is recommended to develop an architecture that would support one or more FEC schemes"
- Some statements at the start of Task Force:
  - In gustlin_3df_01_220118: Desire is a single high-level architecture which gives us the flexibility to do all the above.
    - Same architecture is desirable even if this project is split into different timelines.
  - In shrikhande_3df_01a_220203: Decisions around FEC schemes will have consequences that span multiple generations and deployment scenarios.
  - In wang_3df_01_220215, observation on FEC code and three FEC schemes, End-to-End, Encapsulated(Concatenated) and Segmented.
- Motivation: Analyze FEC schemes for a holistic architecture of 800GbE and 1.6TbE

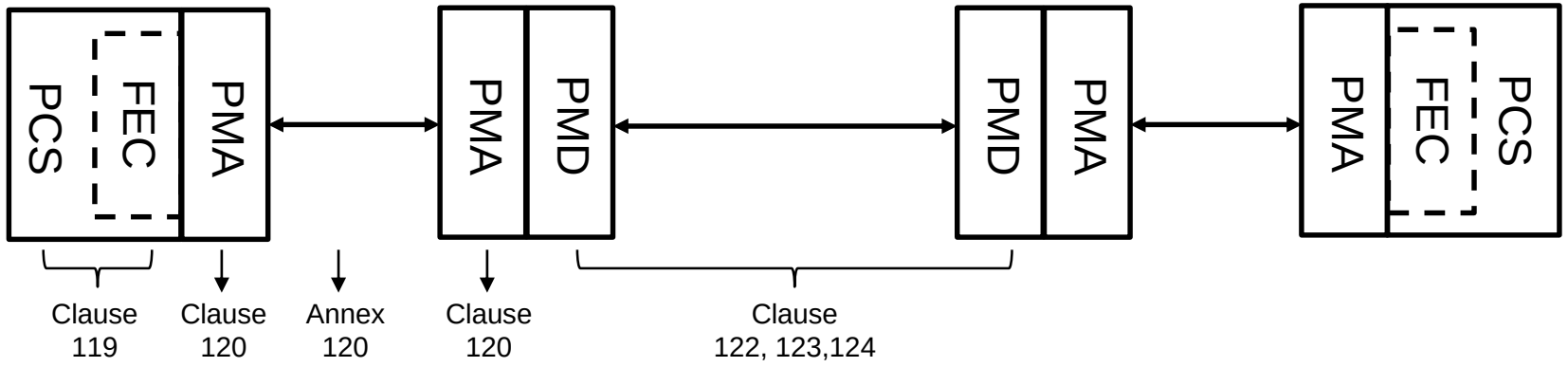
Observation:

- For FEC schemes, End-to-End, Encapsulated or Concatenated, Segmented:
  - What is the definition for each one from standard developing perspective?
  - What is their relationship with diversified implementations and interoperating scenarios?



Revisit IEEE 802.3bs Architecture: End-to-End

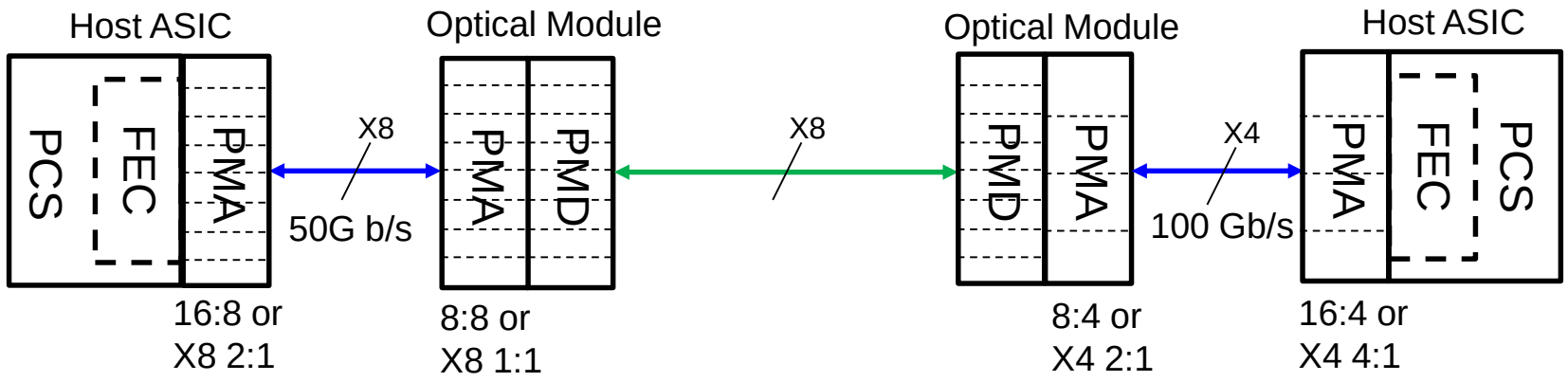
- IEEE 802.3bs was a good example of successful practice in defining an End-to-End FEC architecture from standard specification perspective.



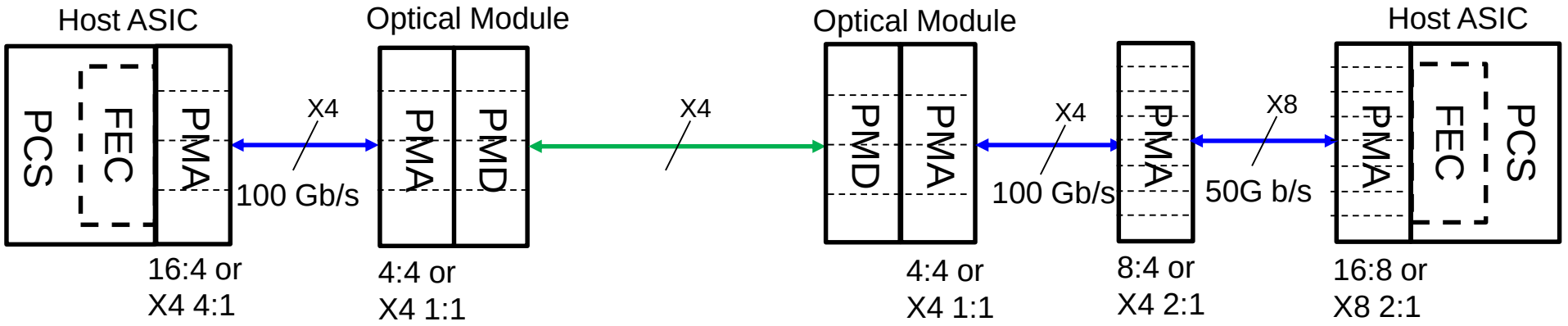
- IEEE 802.3ck extended this architecture for 100 Gb/s per lane AUIs and copper PHYs, and 802.3cu extended it for 100 Gb/s per lane optical PHYs.
  - Both are compatible to IEEE 802.3bs PCS/FEC/PMA sub-layer.

Implementation Examples Based on IEEE 802.3bs Architecture

- 400GAUI-8 C2M ↔ 400GBASE-LR8 ↔ 400GAUI-4 C2M



- 400GAUI-4 C2M ↔ 400GBASE-FR4 ↔ 400GAUI-4 C2M ↔ 400GAUI-8 C2C

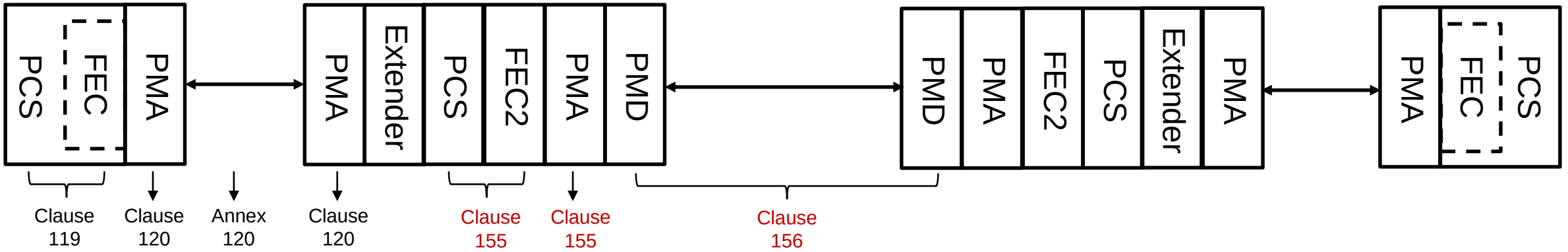


Definition of End-to-End FEC Scheme

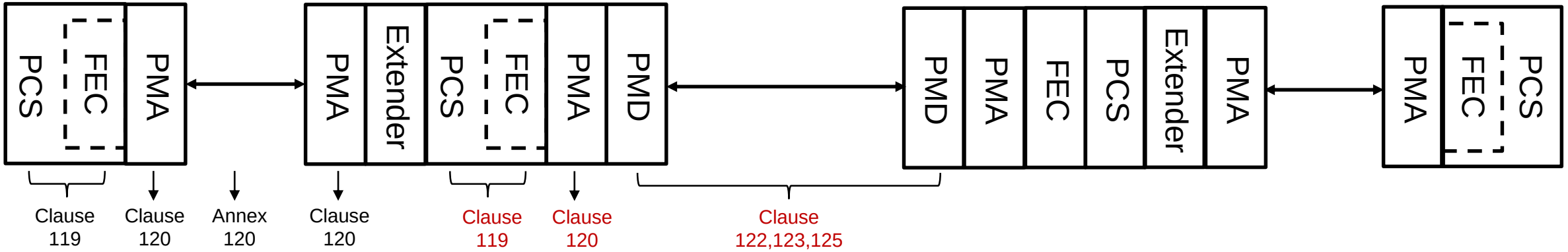
- **One FEC code only, requires all AUI instances and PHY PMDs operating at same overhead ratio.**
- At the receive side host, one decoder corrects all errors caused by the whole link, such as two instances of AUI and the optical or copper cable link **to achieve target BER/FLR and MTTFPA.**
  - Pre-FEC BER: 1E-5 for AUIs and 2.4E-4 for Optical, or same error correct capability for
  - Pre-FEC BER: 4E-5 for AUIs and 1.8E-4 for Optical, example to explain End-to-End
- **PMA: Bit Multiplexing** for n:n, n:m translating
  - Enables protocol agnostic optical module for simplify validation, reuse in multiple applications.
  - Enables breakout in optical module, for example 4 instances of 2:1 PMA to get equivalent 8:4 PMA, either acting as 4X100GbE or 400GbE.
  - Due to the same pre-FEC BER and overhead ratio for 400GAUI-16/8/4, PMA sublayer can be transparent to FEC scheme.

Revisit IEEE 802.3bs/cw Architecture: to be Segmented

- End-to-End scheme translates to segmented with new PCS/FEC/PMA.



- End-to-End scheme can translate to segmented by reusing PCS/FEC/PMA.



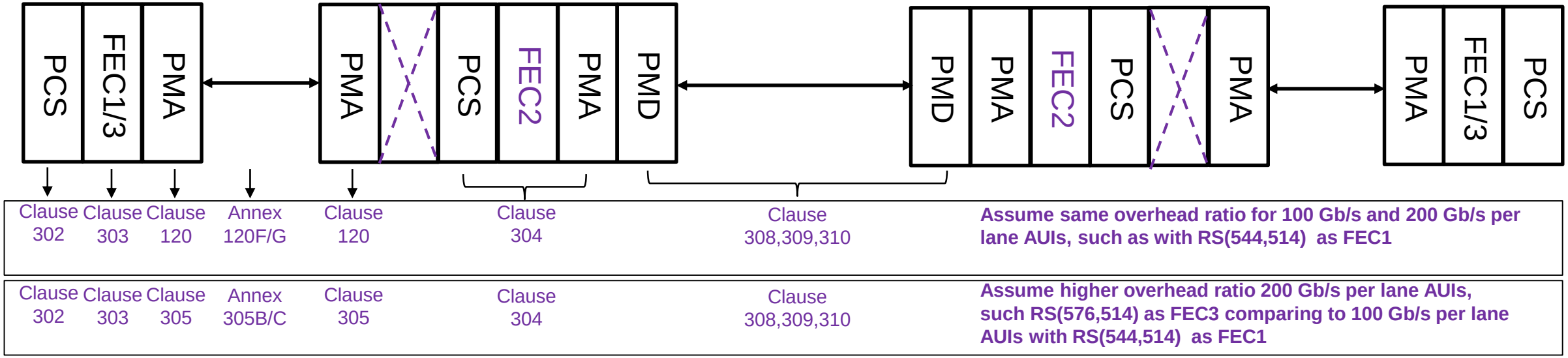
- End-to-End scheme permits diversified segmented implementations.

Definition of Segmented FEC Scheme

- **Independent FEC codes for each segments (part of a link) and isolated with each other, no restrictions on operating overhead ratios for each AUI instances and PHY PMDs.**
- At receive side of each segment, such as AUI or PHY PMDs, the decoders will correct errors caused by its corresponding segment only.
  - **Each segmented FEC code must have proper MTTFPA in order to meet the overall MTTFPA requirement.**
  - **Each segmented FEC code must have proper post-FEC BER/FLR in order to meet the overall target BER/FLR requirement.**
- PMA:
  - **Can be different for each segment according to its corresponding FEC code.**

Encapsulated as a New Candidate FEC Scheme

- Encapsulated scheme from standard specification perspective:
  - Separated FEC sublayer within logic layer stacks as an example.
  - 200 Gb/s per lane AUI, IM-DD and potential single carrier DP-16QAM for 800GbE 10km.
  - 200 Gb/s per lane CR PMD will be further analyzed for DAC.
  - FEC2 as the inner code, wrapped by FEC1 or FEC3 as the outer code, floating to each other.

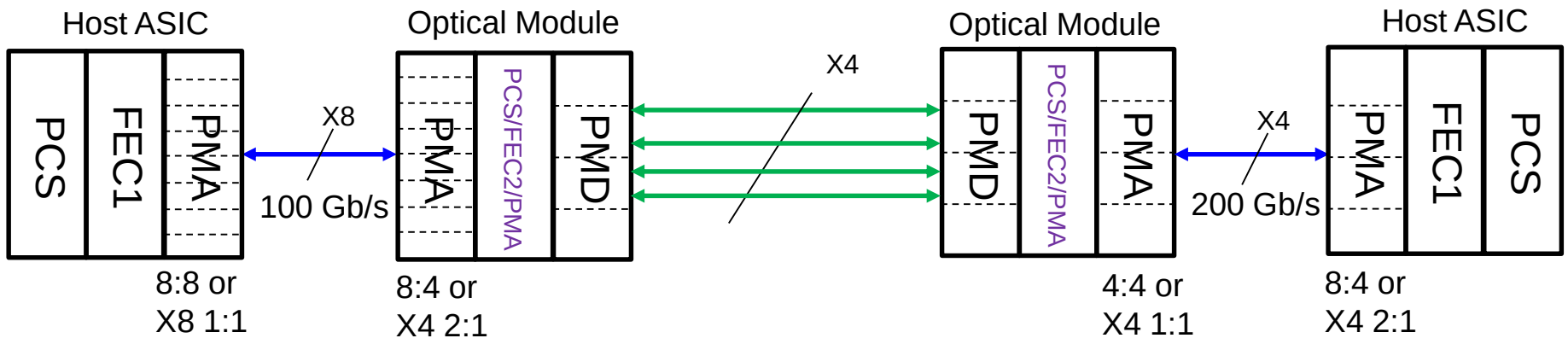


- Refer to brown_3df_02a_220111 for document, clauses and annexes

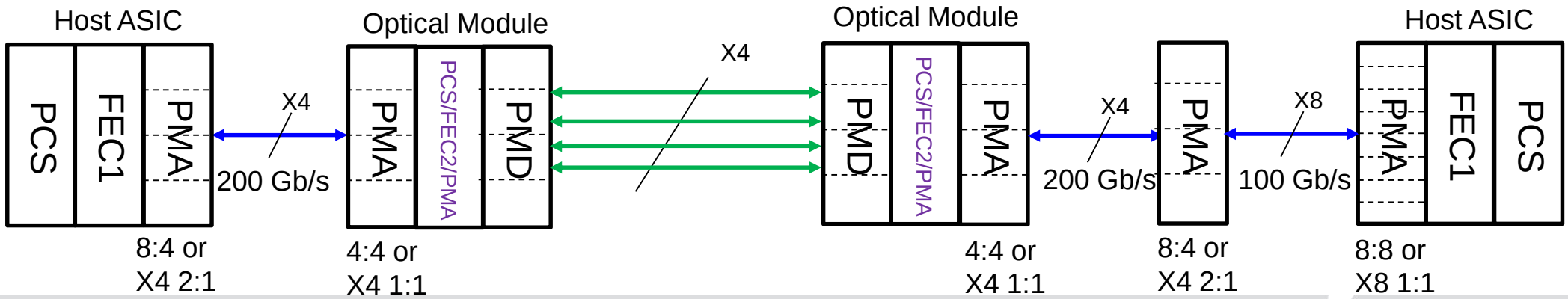
Implementation Examples: Same Overhead Ratio for 100 Gb/s and 200 Gb/s per lane AUIs

- Bit-transparent mapping in optical module from FEC1 lanes to FEC2, with FEC2 operating in per-optical-lane style, similar to End-to-End scheme for breakout.

- 800GAUI-8 C2M ↔ 800GBASE-FR4 ↔ 800GAUI-4 C2M

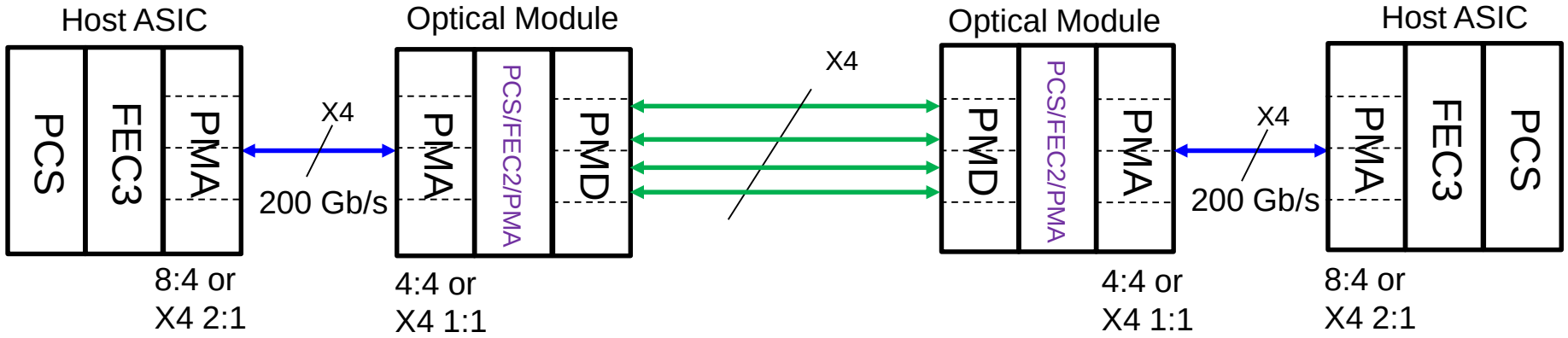


- 800GAUI-4 C2M ↔ 800GBASE-FR4 ↔ 800GAUI-4 C2M ↔ 800GAUI-8 C2C



Implementation Examples: Different Overhead Ratio for 100 Gb/s and 200 Gb/s per lane AUIs

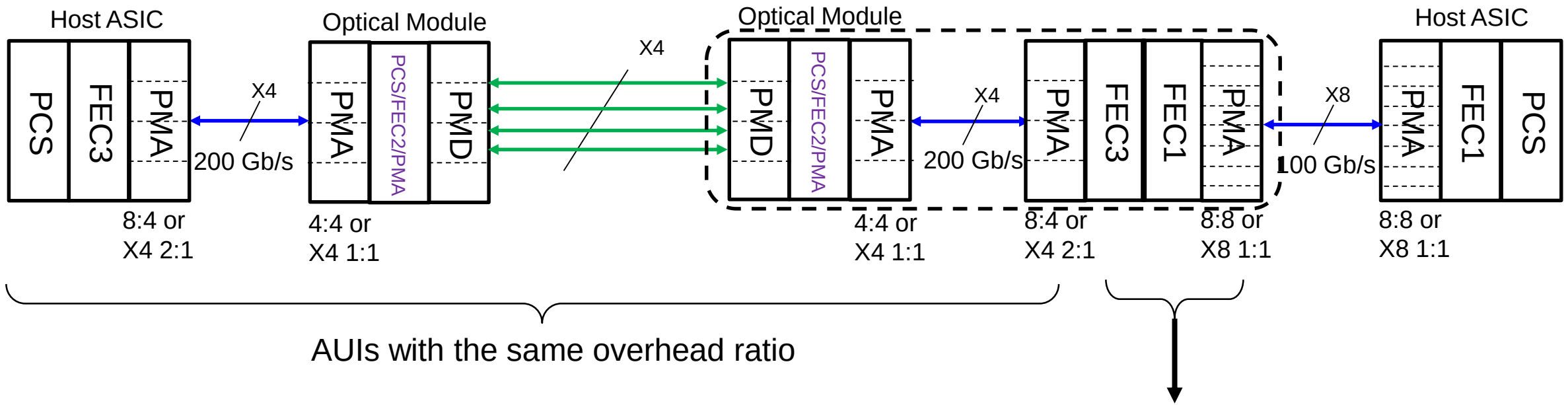
- 100 Gb/s per lane AUI uses RS(544,514) as FEC1
- 200 Gb/s per lane AUI uses RS(576,514), or concatenated FEC code with the same overhead, such as RS(544,514)+ HD BCH(144,136) for FEC3.
- 800GAUI-4 C2M ↔ 800GBASE-FR4 ↔ 800GAUI-4 C2M



- For scenario with 200 Gb/s per lane AUIs on both ends, same bit transparent mapping can be used in optical modules from FEC3 lanes to FEC2 operating in per-optical-lane style, similar to End-to-End scheme for breakout.

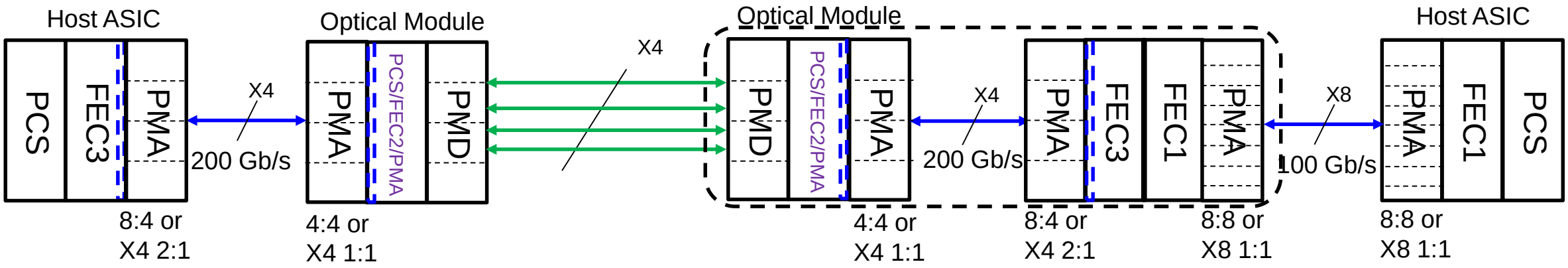
Implementation Examples: Different Overhead Ratio for 100 Gb/s and 200 Gb/s per lane AUIs

- 800GAUI-4 C2M ↔ 800GBASE-FR4 ↔ 800GAUI-4 C2M ↔ 800GAUI-8 C2C



- FEC3 ↔ FEC1 translating required for interconnecting AUIs with different overhead ratios
  - If using RS(576,514) as FEC3, all of decode functions are required to terminated this encapsulated scheme.
  - This implementation scenario will change from encapsulated scheme to segment scheme, similar to the relationship between IEEE 802.3bs and 802.3cw.

Implementation Examples: Different Overhead Ratio for 100 Gb/s and 200 Gb/s per lane AUIs



- FEC3 ↔ FEC1 translating required for interconnecting AUIs with different overhead ratios
  - If using RS(544,514)+HD BCH(144,136) as FEC3, only inner HD BCH(144,136) encode/decode functions are required, as illustrated with dashed blue lines above, while keeping encapsulated scheme with FEC1 as the outer code at interconnected hosts, as in Slide #14 of wang_b400g_01a_210315.
  - Lower latency and power advantages, with the requirement of ~1E-4 pre-FEC BER for 200 Gb/s per lane AUIs.
  - Host data flow to FEC2 has the same overhead ratio for 100 Gb/s and 200 Gb/s per lane AUIs scenarios.
  - Same bit transparent mapping used in optical modules from FEC3 lanes to FEC2 operating in per-optical-lane style, inner code acting as a black box, similar to End-to-End scheme for breakout.

Definition of Encapsulated FEC Scheme

- **One FEC code only, Concatenated, with two sub codes – outer code and inner code.**
- **No restrictions on the operating overhead ratios of each AUI instances and PHY PMDs.**
- At receive side of the inner decoder, it corrects partial errors caused by the inner link only, such as the optical PMD, with left-over errors to the outer code.
- At receive side of the outer decoder, it corrects errors caused by the whole link, such as two instances of AUIs and the left-over errors from the optical or copper cable PMD, **to meet the target BER/FLR and MTTFPA, without knowing the existence of the inner code.**
  - Trade-offs between pre-FEC BER requirement for AUI instances and PMY PMDs, similar to End-to-End scheme.
  - In general, outer code has higher coding gain than inner code. For example, outer code can fully reuse the hard decision RS(544,514) in current IEEE 802.3 standard.

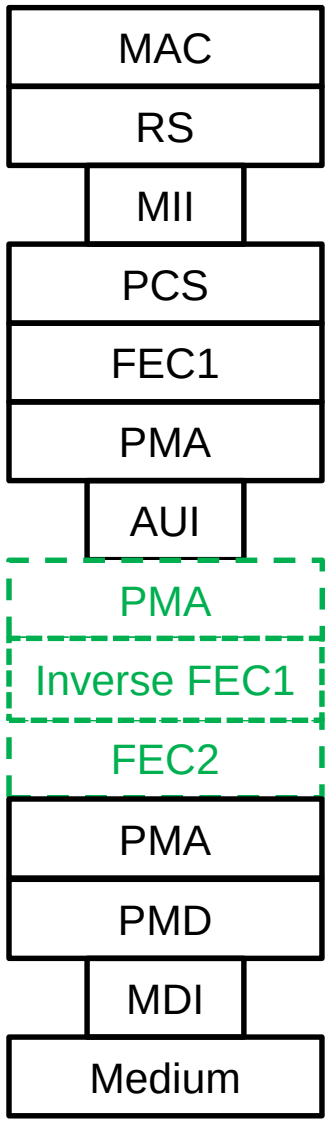
Definition of Encapsulated FEC Scheme

- **Bit transparent mapping in optical module from outer code (FEC1/3) lanes to FEC2 operating in per-optical-lane style, similar to End-to-End scheme.**
  - Enables protocol agnostic optical module for simple validation, reuse in multiple applications.
  - Enables breakout in optical module, for example 4 instances of 2:1 PMA to get an equivalent 8:4 PMA, operating as 800GbE, 4X200GbE or 2X400GbE.
  - Signal modulation agnostic: IM-DD or coherent optical, PAM4 or PAM6.
- Compatible to the 100 Gb/s per lane AUIs and PMDs as adopted in Task Force.
- Supports forward evolution with diversified inner code candidates, with hard or soft decision implementations.
- Potentially lower latency and power as fully capability of FEC code, AUI and PHY.

Comparison of Different FEC Schemes

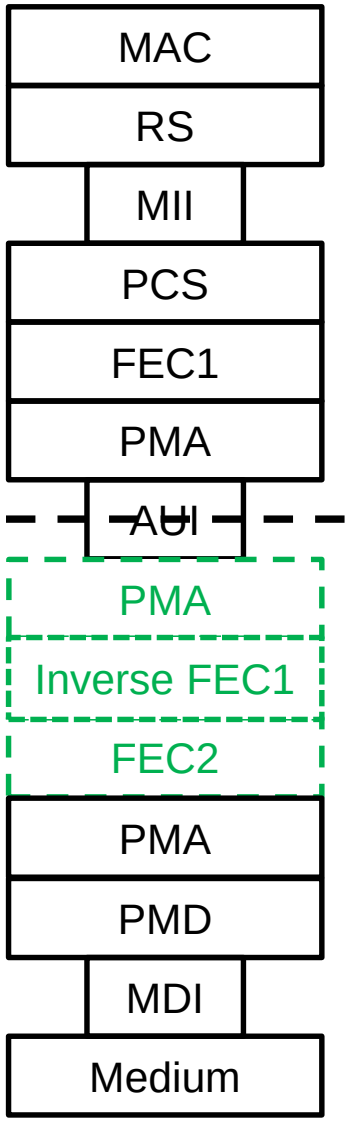
	FEC Codes	Overhead Ratios of AUIs	Overhead Ratios of AUIs and PHY PMD	High NCG Capability	Latency/ Power	Simiplifed Optical Module	Breakout
End-to-End	1	Identical	Identical	Restricted	Potential Lower	Yes	Yes
Encapsulated (Concatenated)	1 with 2 sub code	Identical or Different	Identical or Different	Potential Higher	Potential Lower	Yes	Yes
Segmented	at least 2	Identical or Different	Identical or Different	Potential Higher	Potential Higher	No	Challenge

Suggested Logic Layer Architecture



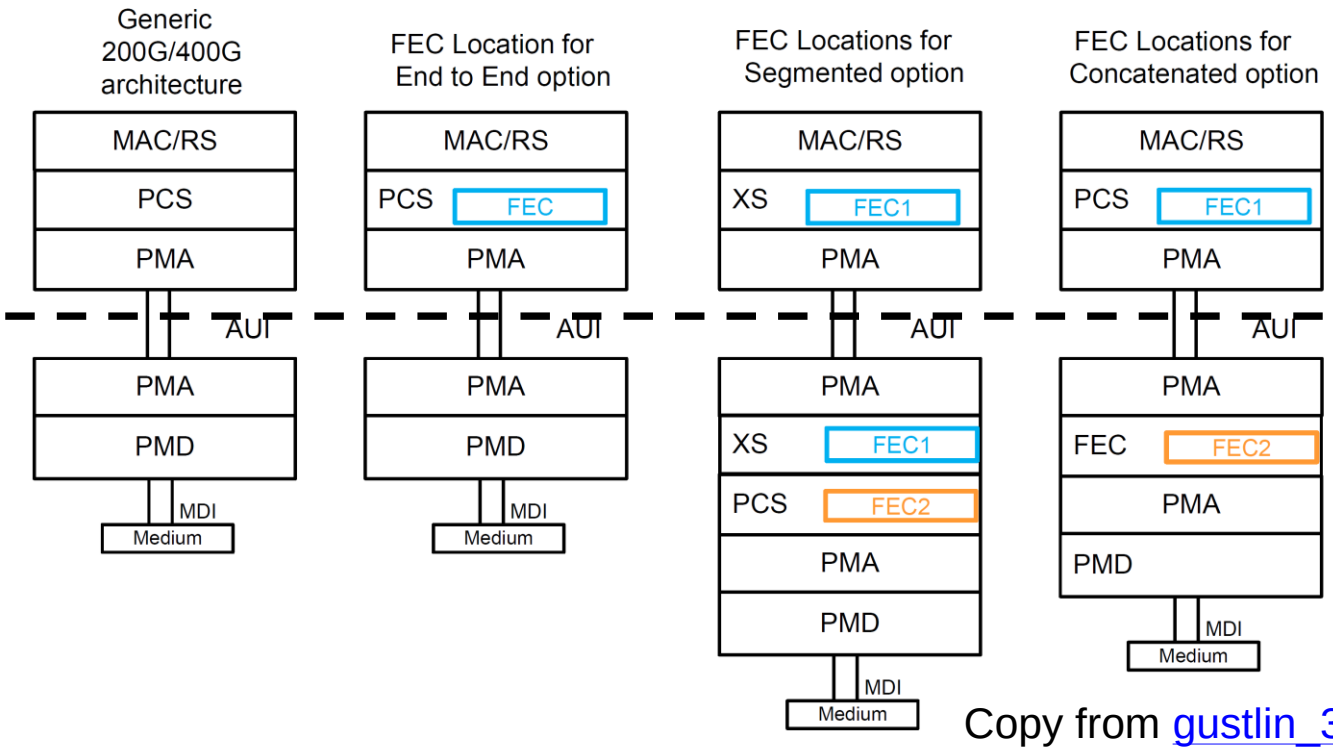
- A holistic architecture to enable all FEC schemes based on a separated FEC sublayer within logic layer stack
- 100 Gb/s and 200 Gb/s SerDes based AUI
  - Pre-FEC BER @ 1E-5, **or ~1E-4**
- FEC Scheme: End-to-End, without PMA, Inverse FEC1, FEC2
- FEC Scheme: Encapsulated or Concatenated, without Inverse FEC1
  - **Outer code and its configuration, for example RS(544,514) with interleaving, lane distribution mechanism is related to inner code**
  - **Candidate inner code: BCH/Hamming, hard or soft decision, etc.**
- FEC Scheme: Segment, with PMA, Inverse FEC1, FEC2.
- **FEC architecture enables all FEC schemes and interconnect implementations.**

To Enable 200/400GbE PHY based on 200 Gb/s per Lane



FEC in a the 200GbE/400GbE Architecture

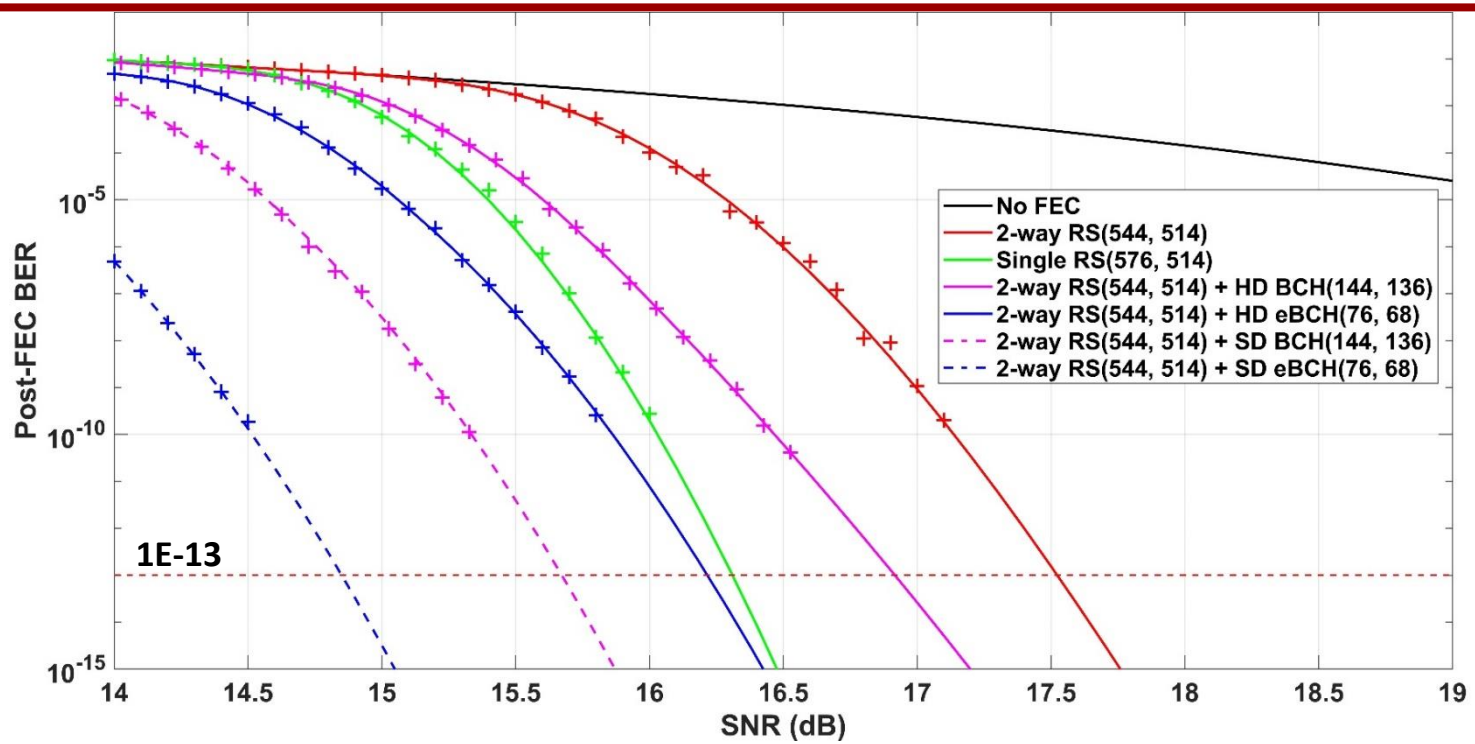
- How 200G/Lane FEC options fit into the architecture



Copy from gustlin_3df_01_220118

- The encapsulated or segmented scheme of 800G/1.6TbE can work together with IEEE 802.3bs to support new 200/400GbE PMDs.

FEC Code Examples to Support Holistic Architecture



Refer to [he_3df_01_220308]

FEC Code	Pre-FEC BER	AUI BER	Post-FEC BER	NCG (dB)	FEC Latency	Inner Code Rate	AUI Rate	Optical Rate
2-way RS(544,514)	2.89E-4	1E-5	1E-13	6.50	51.2 ns	--	8x106.25 Gb/s or 4x212.5 Gb/s	4x212.5 Gb/s
Single RS(576,514)	1.29E-3			7.46	70.4 ns		8x112.5 Gb/s or 4x225 Gb/s	4x225 Gb/s
2-way RS(544,514) + HD BCH(144,136)	6.60E-4			6.86	52.8 ns	18/17	8x106.25 Gb/s or 4x212.5 Gb/s	
2-way RS(544,514) + SD BCH(144,136)	2.47E-3			8.11	60.8 ns			
2-way RS(544,514) + HD eBCH(76,68)	1.43E-3			7.33	52.8 ns	19/17		4x237.5 Gb/s or 1x950 Gb/s
2-way RS(544,514) + SD eBCH(76,68)	5.04E-3			8.69	60.8 ns			

Summary:

- A holistic architecture for both 800GbE and 1.6TbE FEC/PMA is achievable.
- FEC schemes, End-to-End, Encapsulated(Concatenated) and Segmented, can be supported by this architecture as in Slide #17.
- This architecture can work together with proposed PCS function blocks, such as encode and decode, FEC lane distribution, alignment and reorder mechanism from IEEE 802.3bs for FEC 1.
- More detailed work can start from AUI and PMD capability and implementation requirement perspective.

Thank you