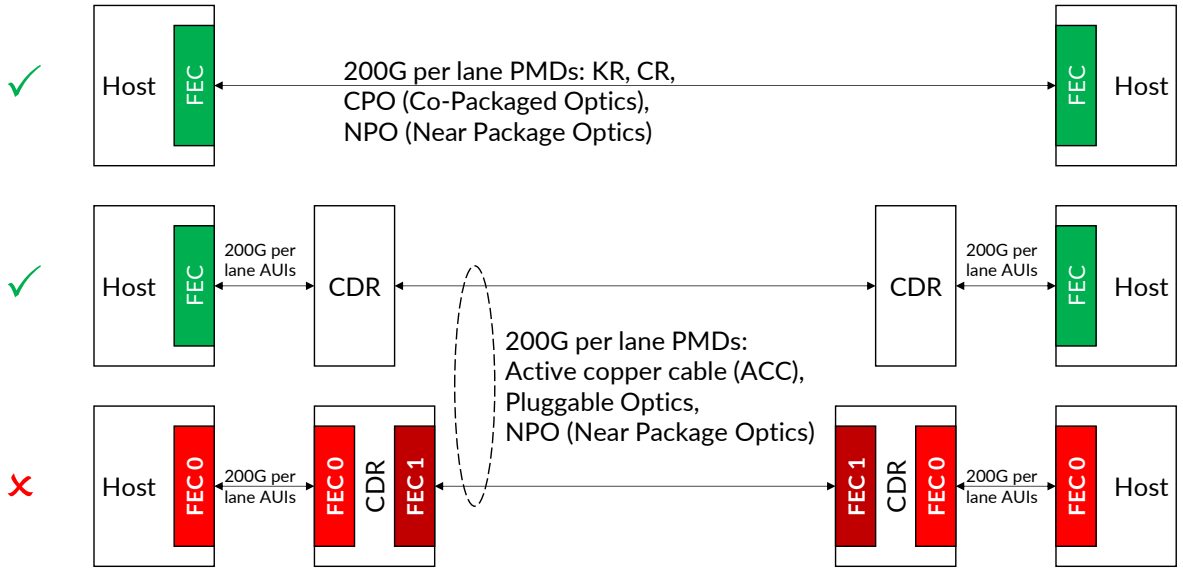
FEC architecture and performance investigation for 800GbE and 1.6TbE

Yuchun LU, Liang LI, Yan ZHUANG, Huawei Technologies

IEEE P802.3df Task Force Architecture & Logic Ad Hoc

April 25 2022

End-to-end FEC for 200G AUIs and PMDs to guarantee the competitiveness of mainstream 200G solutions



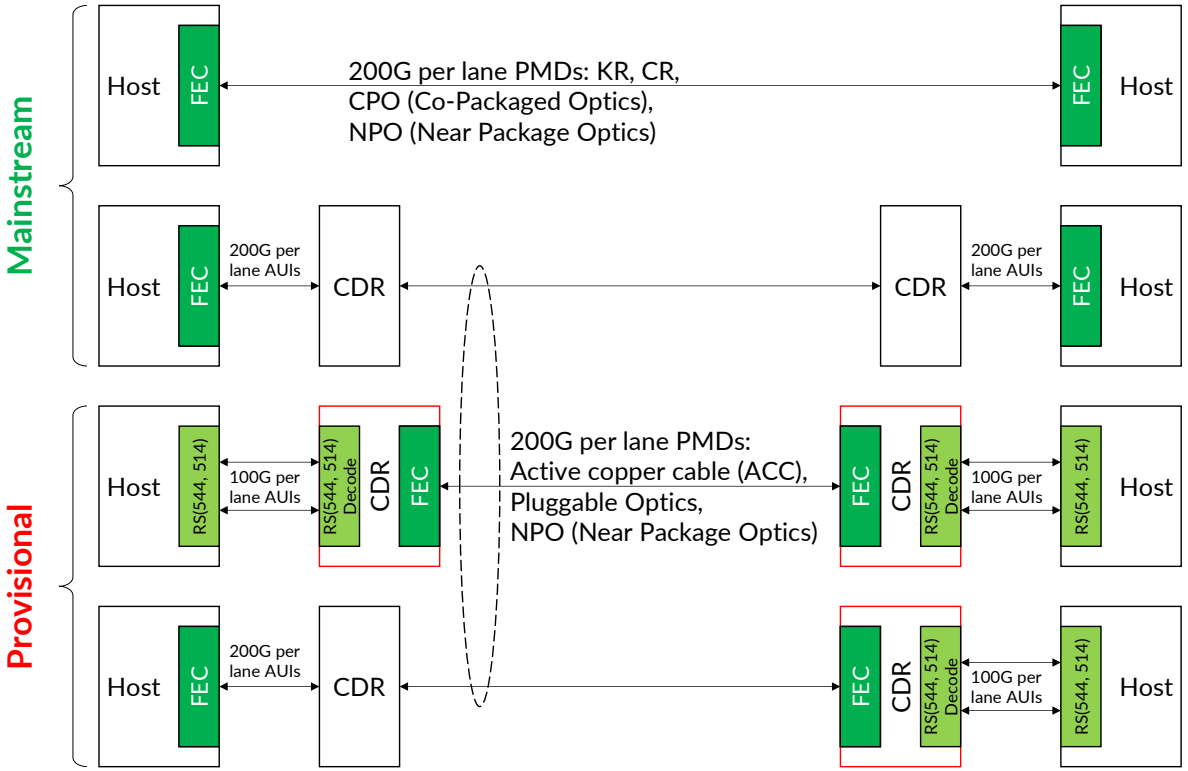
- FEC conversion (or encoding/decoding) inside the CDR introduce extra cost, power consumption and latency.
- If new frequency is introduced i.e. the line rates on both sides of CDR are different, an extra PLL is required.

The competitiveness of solutions of 200G AUIs and PMDs should be guaranteed.

1. **End-to-End FEC architecture to cover both electrical and optical links.**
2. **Bit-transparent CDR (no FEC/PCS processing inside the CDR).**

- 200G AUIs & PMDs are mainstream solutions for 800GbE & 1.6TbE. End-to-end FEC is preferred for low latency, low power consumption and low cost.
- FEC processing (termination, concatenation, conversion, etc.) inside CDR for 200G AUIs and PMDs is not acceptable.
  - Not necessary for segmented links.
    - As shown on page 11 of lu_3df_01b_220215.
  - Not competitive compared with bit-transparent CDR.
    - Extra cost, power consumption and latency.
    - Extra PLL to support new frequency point.
- Soft-decision FEC can not support bit-transparent CDR, it needs mandatory FEC processing inside the CDR with huge burden. With advanced DSP algorithm considered, it is probably the worst in performance (lu_3df_01b_220215).

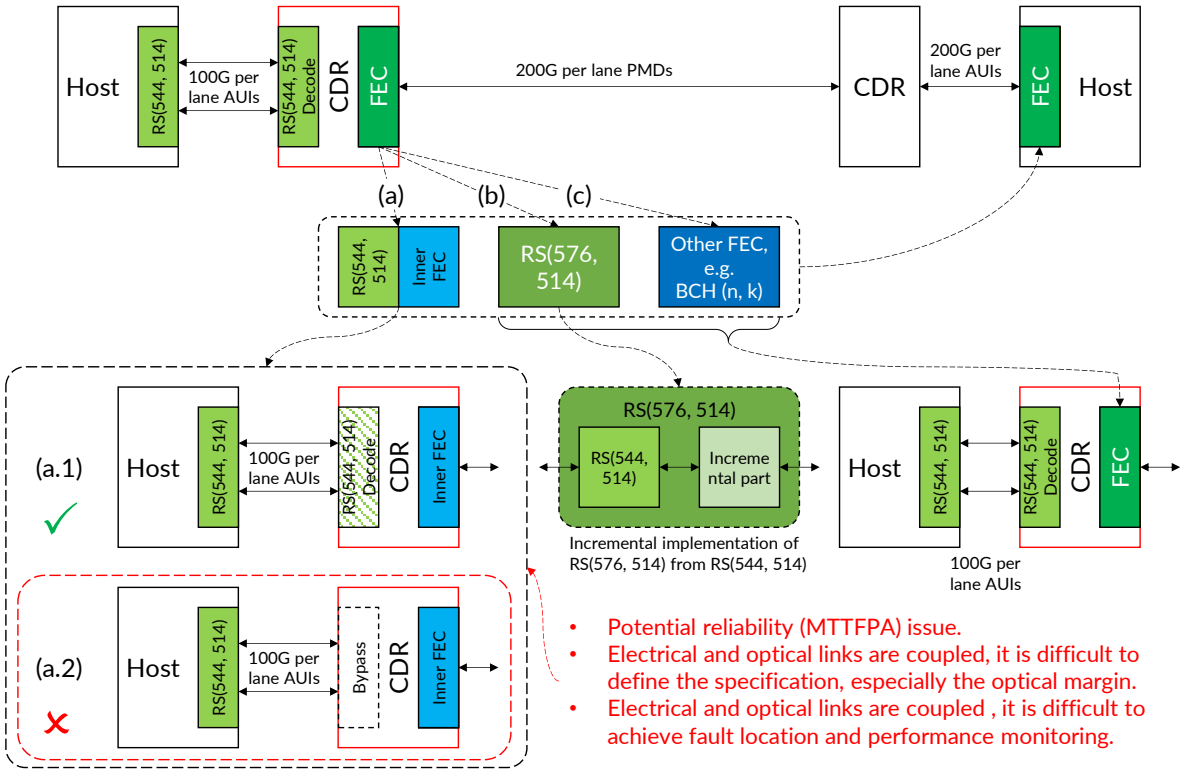
Choosing the proper end-to-end FEC is the key



The key is to find a proper end-to-end FEC for 200G AUI and PMD solutions.

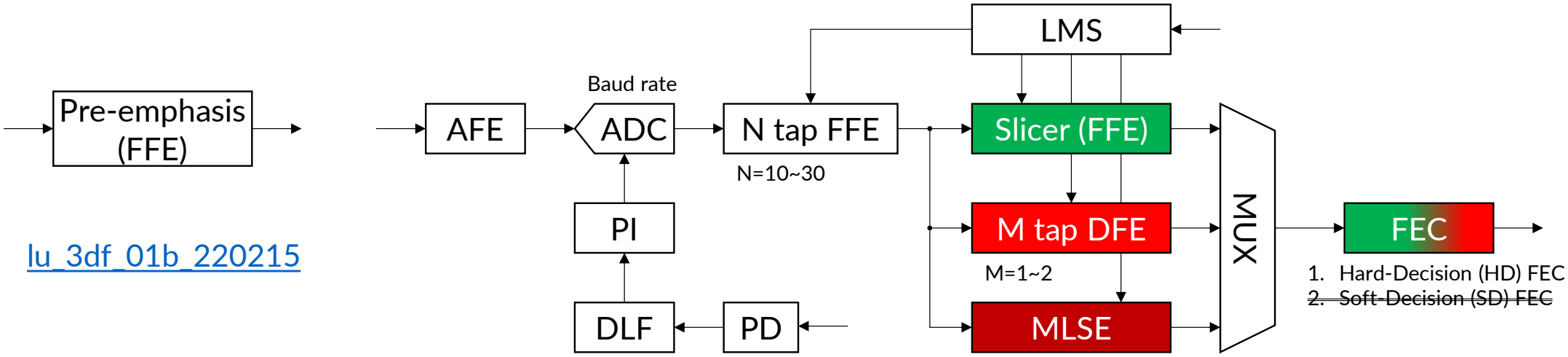
- 200G AUIs and PMDs are mainstream solutions in the future, they are the most important scenarios.
- The application window of the provisional solutions of 100G AUIs and 200G PMDs is narrow. As a transition application, it should not be selected as starting point of the discussion and should not decide the key optimization direction.
  - It is not competitive with 100G solutions in early stage.
  - It is not competitive with 200G solutions as well as the improved 100G solutions overtime, in the end-of-life phase .
- Backward compatibility issues can be easily resolved by introducing PCS processing in the CDR with gearbox, which is natural and necessary for this scenario.
- Impact of burst errors should be considered for both 200G electrical and optical links.
  - It has been fully considered in 100G era.
  - It will be more serious in 200G era.

Concatenation of RS(544, 514) with an inner FEC code has implementation “trick” in CDR with gearbox



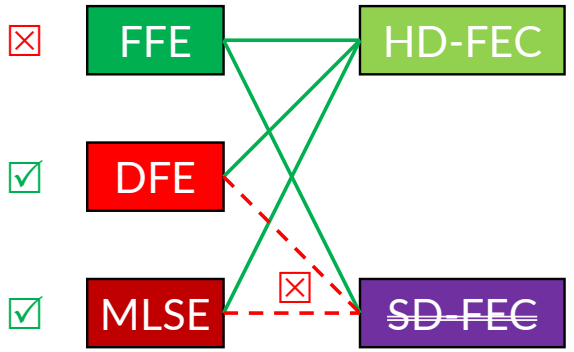
- RS(576, 514)
  - Pros: Reasonable net coding gain. Reuse the RS(544, 514) logics.
  - Cons: need to terminate the RS(544, 514) FEC in CDR?
- RS(544, 514) + Inner FEC
  - Pros: Re-use RS(544, 514) code in the CDR and save a pair of RS(544, 514) encoders, lower latency compared with RS(576, 514)?
  - Cons: Net coding gain is not sufficient for 200G AUIs and PMDs.
- Other FEC, e.g. BCH(n, k)
  - Pros: May provide better net coding gain than RS(576, 514), lower latency compared with RS(576, 514).
  - Cons: Can not reuse RS(544, 514) logic in any cases, high complexity and power consumption.
- Issues need to be resolved for the “trick” of concatenation of RS(544, 514) + inner FEC code.
  - Potential reliability (mean time to false packet acceptance, MTTFPA) issue, the error detection capability is not improved, but the channel for RS(544, 514) is much more bursty.
  - How to consider the penalty of 100G & 200 AUIs errors. The AUI error characteristics are too complicated to be covered by a simple model.
  - How to support fault location and performance monitoring over different link segments with complicated FEC scheme.

DSP considered in the investigation



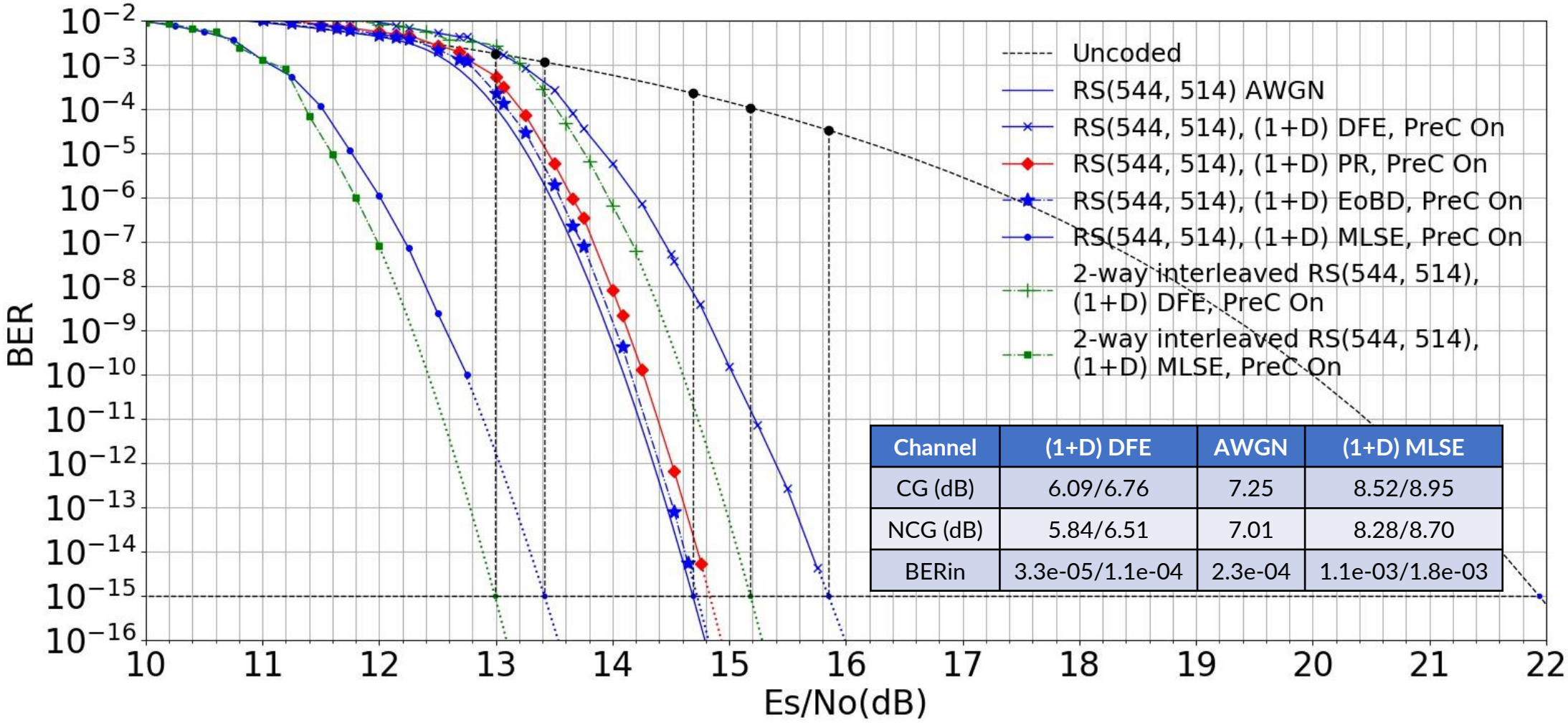
lu_3df_01b_220215

- Three channel models are considered:
  - AWGN channel with FFE (Random)
  - (1+D) channel with DFE (Burst)
  - (1+D) channel with MLSE (Burst)
- Precoding is on for (1+D) channel and is off for AWGN channel.
- Soft-decision FEC decoding is not considered due to the incompatible with DFE and MLSE and it is probably the worst in performance (lu_3df_01b_220215).



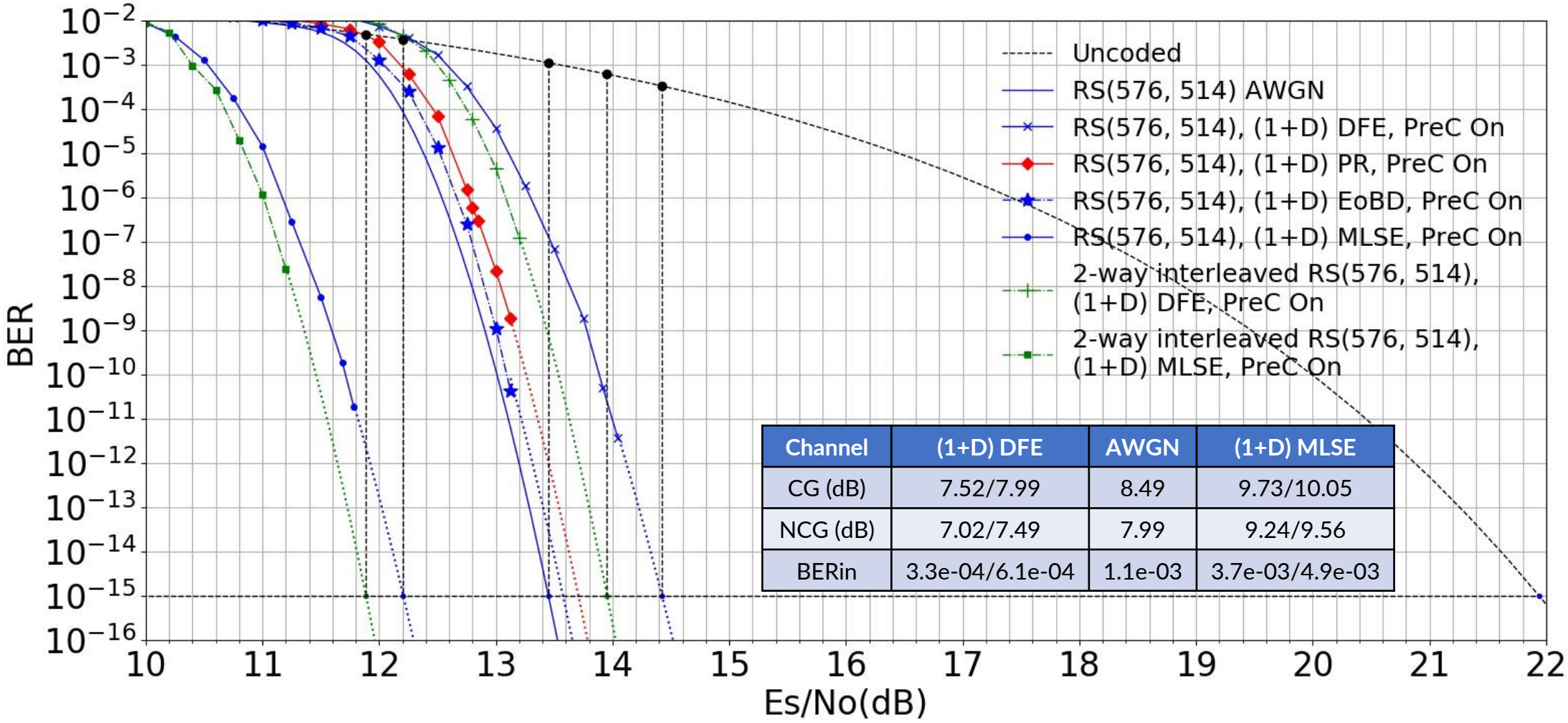
Exclusive relationships of DSP and FEC

6% overhead RS(544, 514)



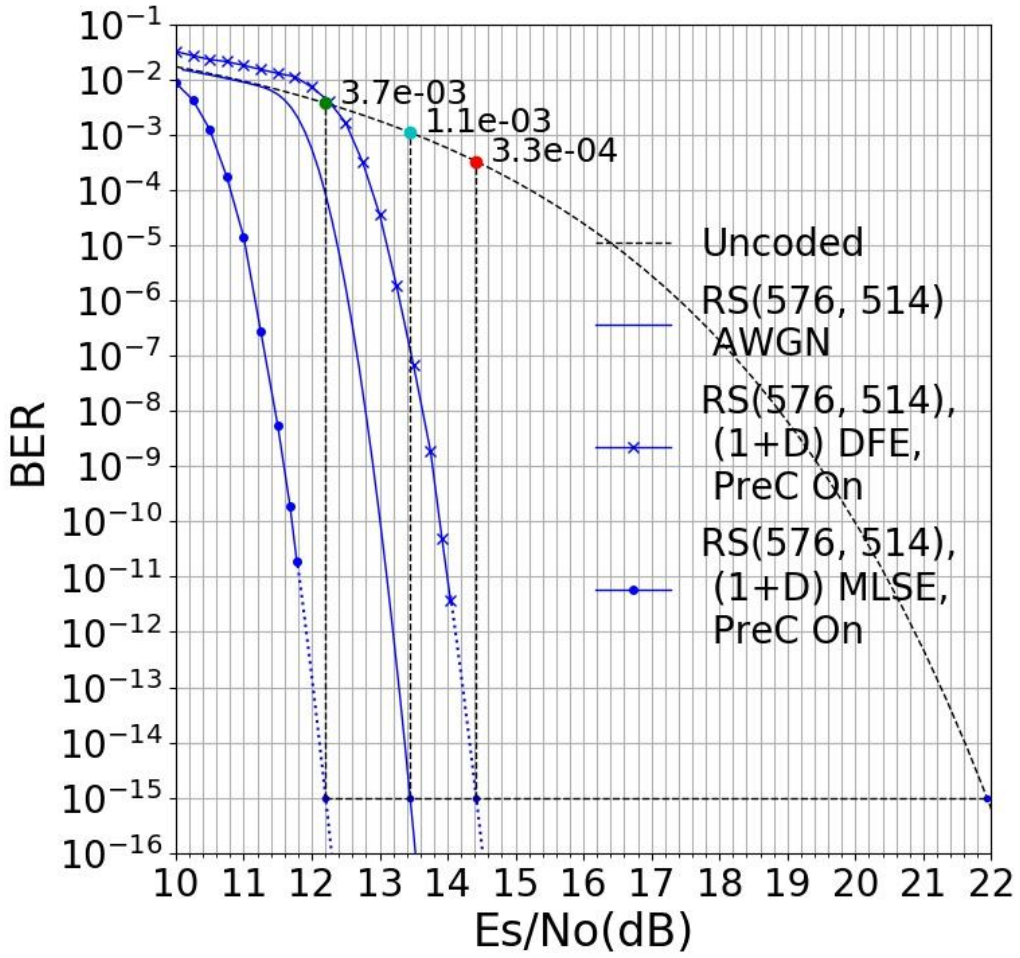
Channel	(1+D) DFE	AWGN	(1+D) MLSE
CG (dB)	6.09/6.76	7.25	8.52/8.95
NCG (dB)	5.84/6.51	7.01	8.28/8.70
BERin	3.3e-05/1.1e-04	2.3e-04	1.1e-03/1.8e-03

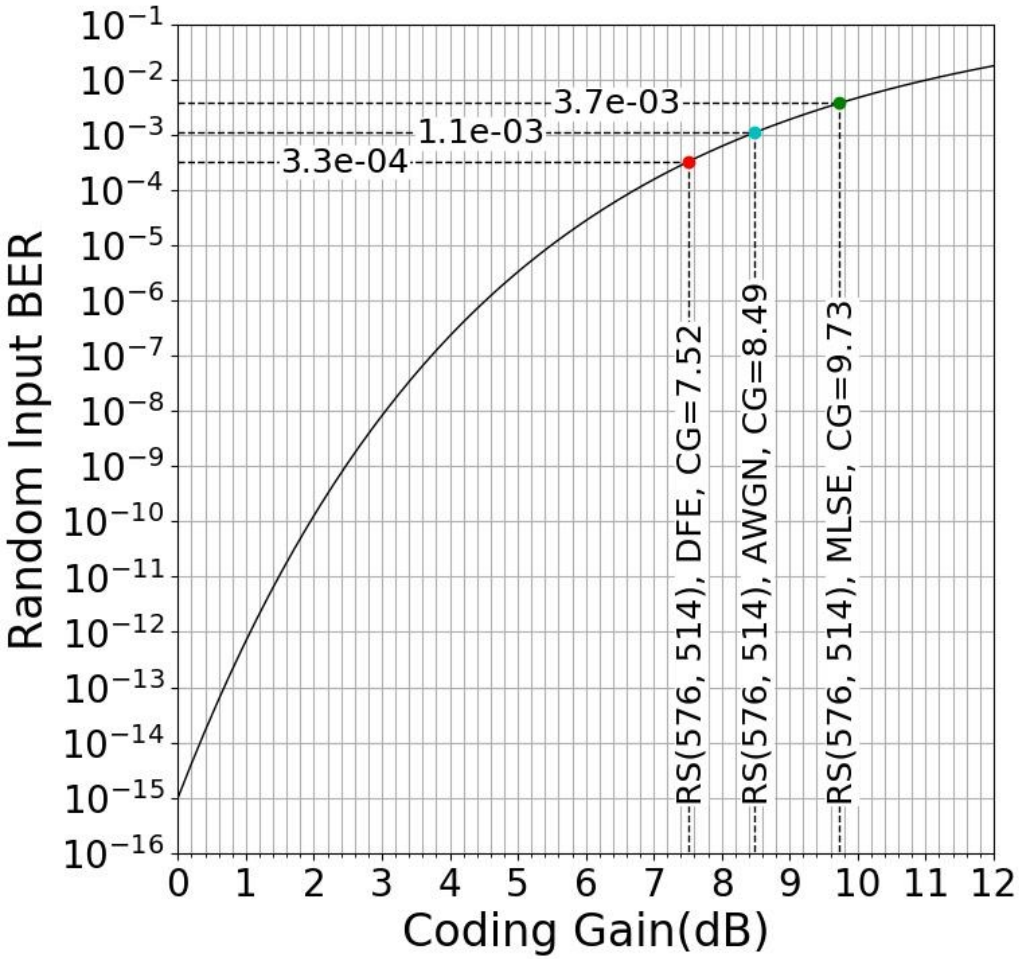
12% overhead RS(576, 514)



Channel	(1+D) DFE	AWGN	(1+D) MLSE
CG (dB)	7.52/7.99	8.49	9.73/10.05
NCG (dB)	7.02/7.49	7.99	9.24/9.56
BERin	3.3e-04/6.1e-04	1.1e-03	3.7e-03/4.9e-03

Coding gain versus random input BER





The random input BER is projected from the coding gain (CG) curve, which are obtained by Monte-Carlo simulation with DSP considered.
If FEC with different overhead is compared, we should use net coding gain (NCG) as a proper metric.

FEC schemes and performance (CG & NCG)

The concatenated FEC can only provide <**0.6dB** net coding gain over the RS(544, 514) with burst errors considered.

FEC candidates			Overhead	Data Rate	CG (dB) @ BERout=1e-15			NCG (dB) @ BERout=1e-15		
					(1+D) DFE	AWGN	(1+D) MLSE	(1+D) DFE	AWGN	(1+D) MLSE
RS(544, 514)			6%	212.5Gbps	6.09	7.25	8.52	5.84	7.01	8.28
RS(544, 514) 2-way interleaved			6%	212.5Gbps	6.76	7.25	8.95	6.51	7.01	8.70
RS(576, 514)		ΔNCG > 0.85dB	12%	225Gbps	7.52	8.49	9.73	7.02	7.99	9.24
RS(576, 514) 2-way interleaved			12%	225Gbps	7.99	8.49	10.05	7.49	7.99	9.56
RS(544, 514)	BCH(144, 136, t=1)	ΔNCG < 0dB vs. RS(544, 514)	12%	225Gbps	6.20	7.98	8.64	**5.71**	7.49	**8.14**
	BCH(180, 170, t=1)		12%	225Gbps	6.28	7.89	8.62	**5.79**	7.39	**8.12**
	BCH(360, 340, t=2)	ΔNCG < 0.5dB vs. RS(544, 514)	12%	225Gbps	6.62	7.93	9.07	6.12	7.43	8.58
	BCH(720, 680, t=4)		12%	225Gbps	6.77	7.87	9.20	6.28	7.38	8.70
RS(544, 514) 2-way interleaved	BCH(144, 136, t=1)	ΔNCG < 0dB vs. 2x RS(544, 514)	12%	225Gbps	6.78	8.22	9.00	**6.29**	7.73	**8.51**
	BCH(180, 170, t=1)		12%	225Gbps	6.85	8.09	9.03	**6.36**	7.60	**8.54**
	BCH(360, 340, t=2)	ΔNCG < 0.6dB vs. 2x RS(544, 514)	12%	225Gbps	7.36	8.22	9.62	6.86	7.72	9.13
	BCH(720, 680, t=4)		12%	225Gbps	7.48	8.33	9.70	6.99	7.83	9.21
RS(544, 514)	RS(36, 34, m=10, t=1)	ΔNCG < 0.2dB vs. RS(544, 514)	12%	225Gbps	6.24	7.59	8.54	5.75	7.10	8.04
	RS(72, 68, m=10, t=2)		12%	225Gbps	6.60	7.52	8.85	**6.10**	7.03	**8.36**
	RS(144, 136, m=10, t=4)		12%	225Gbps	6.47	7.48	8.80	5.98	6.98	8.30
RS(544, 514) 2-way interleaved	RS(36, 34, m=10, t=1)	ΔNCG < 0.2dB vs. 2x RS(544, 514)	12%	225Gbps	6.81	7.80	9.08	6.32	7.30	8.58
	RS(72, 68, m=10, t=2)		12%	225Gbps	7.13	7.84	9.38	**6.63**	7.34	**8.89**
	RS(144, 136, m=10, t=4)		12%	225Gbps	7.14	7.90	9.35	6.64	7.40	8.85
BCH(2870, 2570, m=12, t=25), 10-bit pads			12%	225Gbps	7.22	8.68	9.48	6.73	8.18	8.98
BCH(5751, 5140, m=13, t=47), 9-bit pads			12%	225Gbps	7.93	9.20	10.1	7.44	8.71	9.61

Estimation error of +/- 0.1dB may exists due to the extrapolation of the BER vs SNR curves.

FEC schemes and performance (Random BERin)

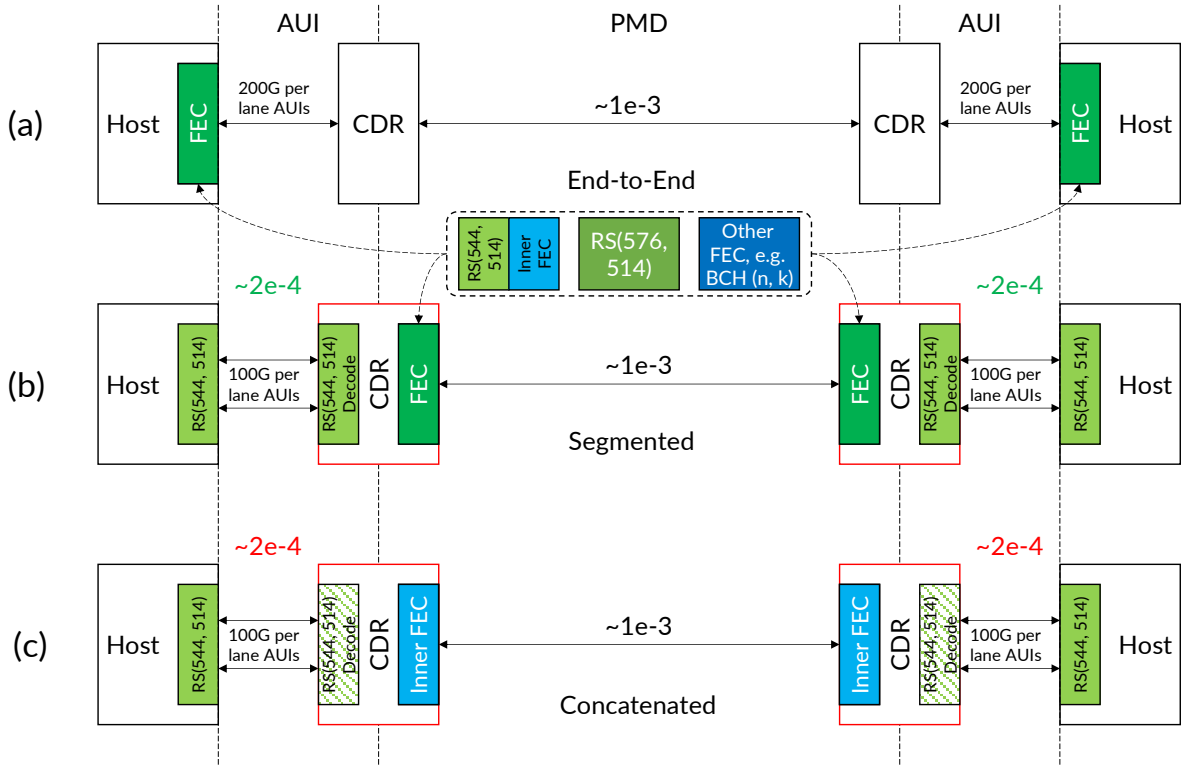
FEC candidates		Overhead	Data Rate	Random BERin @ BERout=1e-15		
				(1+D) DFE	AWGN	(1+D) MLSE
RS(544, 514)		6%	212.5Gbps	3.3e-05	2.3e-04	1.1e-03
RS(544, 514) 2-way interleaved		6%	212.5Gbps	1.1e-04	2.3e-04	1.8e-03
RS(576, 514)		12%	225Gbps	3.3e-04	1.1e-03	3.7e-03
RS(576, 514) 2-way interleaved		12%	225Gbps	6.1e-04	1.1e-03	4.9e-03
RS(544, 514)	BCH(144, 136, t=1)	12%	225Gbps	4.1e-05	6.1e-04	1.3e-03
	BCH(180, 170, t=1)	12%	225Gbps	4.7e-05	5.4e-04	1.3e-03
	BCH(360, 340, t=2)	12%	225Gbps	8.4e-05	5.6e-04	2.0e-03
	BCH(720, 680, t=4)	12%	225Gbps	1.1e-04	5.3e-04	2.3e-03
RS(544, 514) 2-way interleaved	BCH(144, 136, t=1)	12%	225Gbps	1.1e-04	8.1e-04	1.9e-03
	BCH(180, 170, t=1)	12%	225Gbps	1.2e-04	6.9e-04	1.9e-03
	BCH(360, 340, t=2)	12%	225Gbps	2.6e-04	8.0e-04	3.4e-03
	BCH(720, 680, t=4)	12%	225Gbps	3.1e-04	9.2e-04	3.6e-03
RS(544, 514)	RS(36, 34, m=10, t=1)	12%	225Gbps	4.4e-05	3.6e-04	1.2e-03
	RS(72, 68, m=10, t=2)	12%	225Gbps	8.1e-05	3.3e-04	1.6e-03
	RS(144, 136, m=10, t=4)	12%	225Gbps	6.6e-05	3.1e-04	1.5e-03
RS(544, 514) 2-way interleaved	RS(36, 34, m=10, t=1)	12%	225Gbps	1.2e-04	4.8e-04	2.0e-03
	RS(72, 68, m=10, t=2)	12%	225Gbps	1.9e-04	5.0e-04	2.7e-03
	RS(144, 136, m=10, t=4)	12%	225Gbps	1.9e-04	5.4e-04	2.6e-03
BCH(2870, 2570, m=12, t=25), 10-bit pads		12%	225Gbps	2.2e-04	1.3e-03	3.0e-03
BCH(5751, 5140, m=13, t=47), 9-bit pads		12%	225Gbps	5.7e-04	2.3e-03	5.1e-03

The random BERin is projected from the coding gain (CG), which is obtained from the end-to-end Monte-Carlo simulation with DSP considered.

It is improper to use the output BER of inner FEC as an input BER to RS(544, 514) in the performance analysis of concatenated FEC.

It is improper to use the output BER of DFE or MLSE as an input BER for FEC in the performance analysis of DFE/MLSE cascaded with FEC.

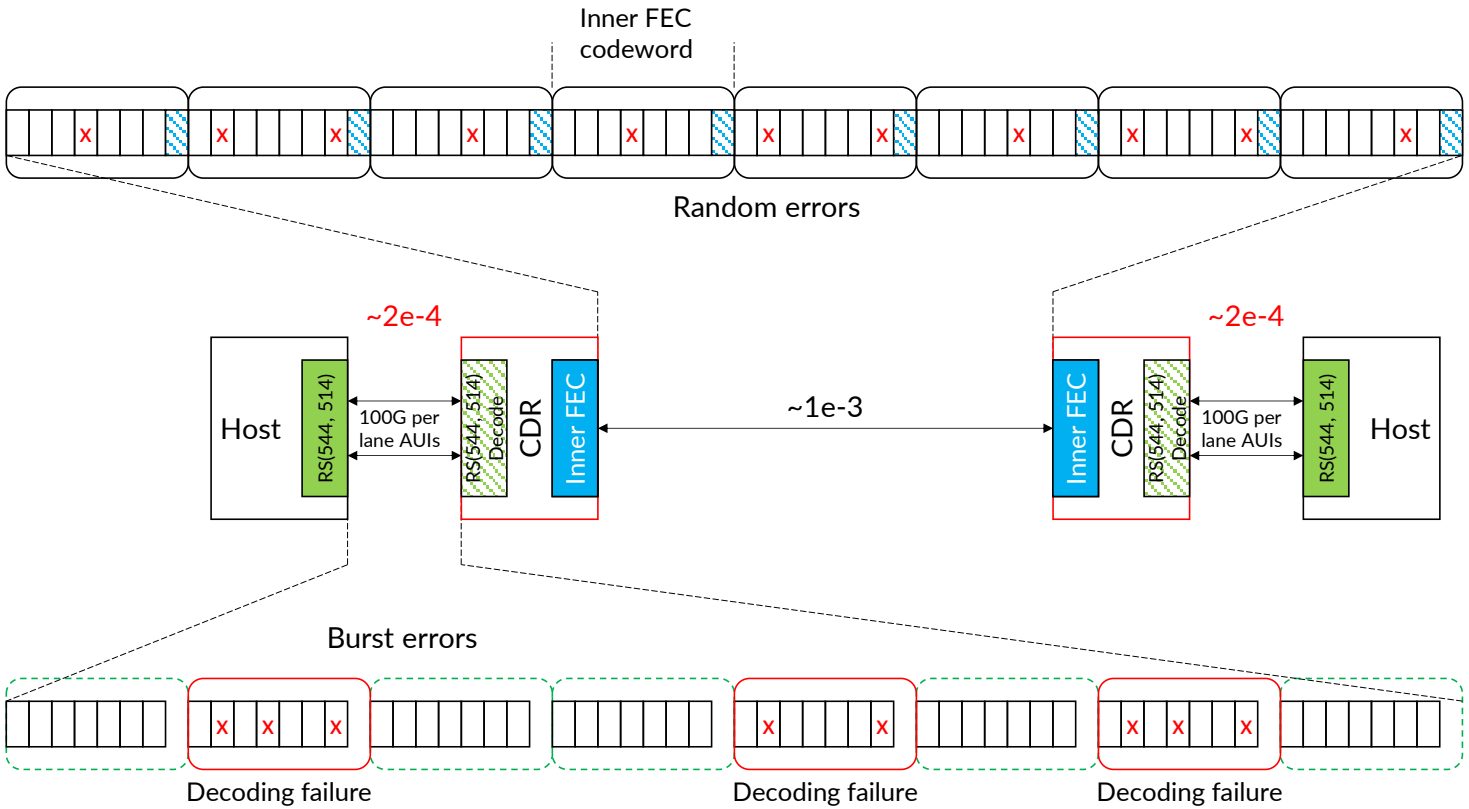
Reliability concern of the ‘trick’ concatenated implementation of RS(544, 514) + Inner FEC.



- For case (a) and (b), the error detection capability of the stronger FEC can be fully utilized for error indication in order to guarantee the predicted MTTFPA larger than the age of the universe.
- For case (b), the RS(544, 514) only needs to cover the electrical link. The uncorrectable FEC blocks can be marked by the stronger FEC inside the CDR.
- For case (c), besides the electrical link, the RS(544, 514) has to cover the burst errors due to the Inner FEC decoding failure, which is bursty. The concatenated scheme cannot leverage the parity bits of inner FEC to indicate the FEC decoding failure.
- The MTTFPA for RS(544, 514) is marginal with random input error distribution assumption (anslow_3ct_01_0519).

AUIs in (b) and (c) are different, even though they have the same BER value.. AUIs in (c) are more bursty due to the decoding failure of the “Inner FEC”.
The input error distribution is critical for FEC. It is incorrect to do “BER relay”, i.e. use output BER of inner FEC as input BER of RS(544, 514) in the analysis.
It is also improper to use measured PreFEC BER to indicate the FEC performance. Net coding gain (NCG) is the correct metric for FEC evaluation.

Inner FEC decoding failure generates burst errors



Even though the “Inner FEC” can correct the PMD link errors from BER of ~1e-3 to an equivalent AUI BER of ~2e-4, it does not mean the RS(544, 514) can achieve end-to-end link BER below 1e-15.
“BERin=2e-4 @ BERout=1e-15” comes from the AWGN assumption.

- Inner FEC decoding failure generates burst errors. The stronger the inner FEC is, the more serious the bust error will be.
- The parity bits of the inner FEC are removed thus it cannot be used for error indication. Half of the parity bits are wasted and cannot be used for decoding failure detection.
- The equivalent channel for RS(544, 514) is more bursty, but the error detection capability is not improved, further more, the MTTFPA for RS(544, 514) is already marginal with random input error distribution assumption (anslow_3ct_01_0519), all these factors arise the concern of the MTTFPA issue.

Summary for the FEC performance

- RS(576, 514) has >**0.85dB** NCG improvement over RS(544, 514) with reasonable cost.
- RS(544, 514) + Inner FEC has <**0.5dB** NCG improvement over RS(544, 514)
  - Delta NCG < 0dB, if Inner FEC is BCH(144, 136, t=1) or BCH(180, 160, t=1).
  - Delta NCG < 0.5dB, if Inner FEC is BCH(360, 340, t=2) or BCH(720, 680, t=4).
  - Delta NCG < 0.2dB, if Inner FEC is RS(36, 34, m=10, t=1) or RS(72, 68, m=10, t=2) or RS(144, 136, m=10, t=4).
- 2-way interleaved RS(544, 514) + Inner FEC has <**0.6dB** NCG improvement over 2-way interleaved RS(544, 514)
  - Delta NCG < 0dB, if Inner FEC is BCH(144, 136, t=1) or BCH(180, 160, t=1).
  - Delta NCG < 0.6dB, if Inner FEC is BCH(360, 340, t=2) or BCH(720, 680, t=4).
  - Delta NCG < 0.2dB, if Inner FEC is RS(36, 34, m=10, t=1) or RS(72, 68, m=10, t=2) or RS(144, 136, m=10, t=4).
- 2-way interleaved RS(544, 514) + BCH(720, 680, t=4) is approaching RS(576, 514) with higher complexity, it still has >=**0.35dB** NCG gap compared with 2-way interleaved RS(576, 514).
  - The complexity of 2-way interleaved RS(544, 514) + BCH(720, 680, t=4) is probably higher than RS(576, 514), which means it is less efficient.
- BCH(5751, 5140, m=13, t=47) has >0.7dB NCG improvement over RS(576, 514) under AWGN channel, but it has negligible NCG improvement over RS(576, 514) with DFE and MLSE. The complexity is large and it cannot reuse the RS(544, 514) logic.
- Soft-decision FEC can not support bit-transparent CDR, it needs mandatory FEC processing inside the CDR. With advanced DSP algorithm considered, it is probably the worst in performance (lu_3df_01b_220215).

Summary for the FEC architecture

- **200G AUIs and PMDs are mainstream solutions, end-to-end FEC is the best choice.**
  - FEC processing (termination, concatenation, conversion, etc.) inside CDR is not acceptable.
  - FEC processing inside CDR is not necessary for segmented links (lu_3df_01b_220215, page 11).
  - FEC processing inside CDR is not competitive compared with bit-transparent CDR.
    - If different FECs for AUIs and PMDs are chosen, we need to pay extra cost, power consumption and latency for nothing.
    - Further, If the line rate on both side of CDR are different, an extra PLL is required to support new frequency point which is overwhelmed.
- **For 100G AUIs and 200G PMDs as provisional solutions, the segmented FEC is the best choice.**
  - As a transition application, it should not be selected as starting point of the discussion and should not decide the key optimization direction.
    - It is not competitive with 100G solutions in early stage.
    - It is not competitive with 200G solutions and the improved 100G solutions overtime, in the end-of-life phase .
  - FEC processing (termination, concatenation, conversion, etc.) inside CDR is natural and necessary for CDR with gearbox. Backward compatibility issues can be easily resolved by introducing PCS processing in the CDR with gearbox, in which it is essential.
- **“Concatenated FEC architecture” has the reliability concerns, i.e. MTTFPA issue.**
  - Basic idea: Implement RS(544, 514) in the host for the AUI interfaces and concatenate an inner FEC in the CDR.
  - The decoding failure of inner FEC generates burst errors. Even if the equivalent BER for AUIs is ~2e-4, it is still highly risky for RS(544, 514).
  - The parity bits of the inner FEC are striped and cannot used for the error indication. **Half of the parity bits of concatenated FEC architecture are wasted and cannot be used to improve the error detection capability**.
  - The MTTFPA for RS(544, 514) is marginal with random input error distribution assumption (anslow_3ct_01_0519).

Summary for some conceptual clarifications

- **Input BER (BERin) is not a good metric**. It cannot reflect the FEC performance with burst channels.
  - The error distribution impacts the FEC performance tremendously. The inner FEC decoding of concatenated FEC scheme, DFE and MLSE impact the error distribution. **The burst errors dominate the performance in FEC investigation**.
  - The input BER cannot reflect the penalty due to the FEC overhead, thus we cannot make a fair comparison if the FEC overhead is different.
  - Net coding gain (NCG) from end-to-end simulation is a proper metric for FEC performance evaluation and comparison.
  - Giving a clear definition for input BER (BERin) metric is important. When we use e.g. 2e-3 as a reference performance for FEC selection, a reasonable definition for input BER requirement is random BER which can be projected to the coding gain (CG) directly.
  - Always keep in mind that there is penalty for "burst channels" when using input BER (BERin) as a FEC performance metric.
- **BER cannot be "relayed"**. It is conceptually wrong to think that as long as the post FEC BER of inner FEC is "2e-4", the end-to-end performance can be guaranteed by RS(544, 514).
  - The FEC performance depends on **the input BER** and **the error distribution**. The error distribution play a more important role, error-floor-free is a mandatory for every new FEC schemes, especially for concatenated FEC.
  - **Inner FEC decoding failure generates burst errors**; DFE and MLSE generate burst errors.
- **Soft-Decision FEC does not mean higher performance**.
  - Soft-decision FEC is bound to the DSP algorithm, if the DSP algorithm is not disclosed, there is no way to evaluate the performance.
  - With nonlinear equalizers such as DFE and MLSE considered, SD-FEC is probably the worst in performance.
- **Concatenation FEC does not means low cost.**
  - To achieve the same performance, it likely has larger complexity than RS(576, 514), e.g. 2-way interleaved RS(544, 514) + BCH(720, 680) .
  - RS(576, 514) can fully reuse the RS(544, 514) logic, incremental encoding/decoding is archivable (similar to concatenated FEC).
  - The reliability concern (MTTFPA issue) should be resolved first to make sure that a proper FEC architecture is selected.

Q & A