Baseline proposals for 800 GbE RS/MII, Extender/XS, Time Sync and PMA, using 100G/lane signaling

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Introduction

This presentation will propose baseline proposals for the following items for 800GbE using 100G/lane signaling:

- RS/MII
- MII Extender/XS
- Time Sync
- PMA

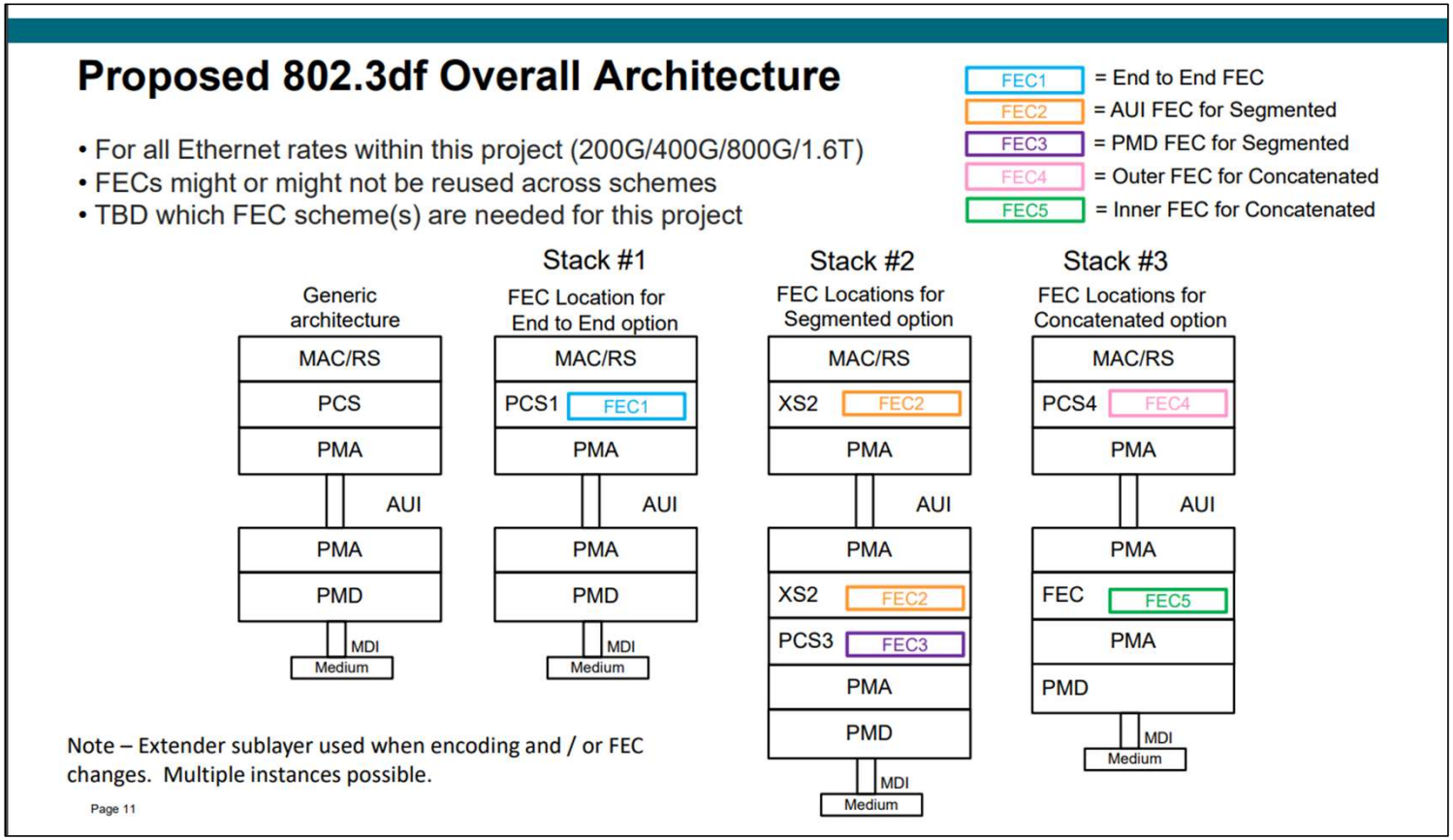
Adopted logic architecture

A logic architecture baseline was adopted during the 802.3df Task Force meeting in May 2022, based on the following presentation:

- gustlin_3df_01a_220517

The baselines in this presentation all support the adopted logic architecture, for 800GbE interfaces using 100G/lane signaling.

Adopted 802.3df architecture



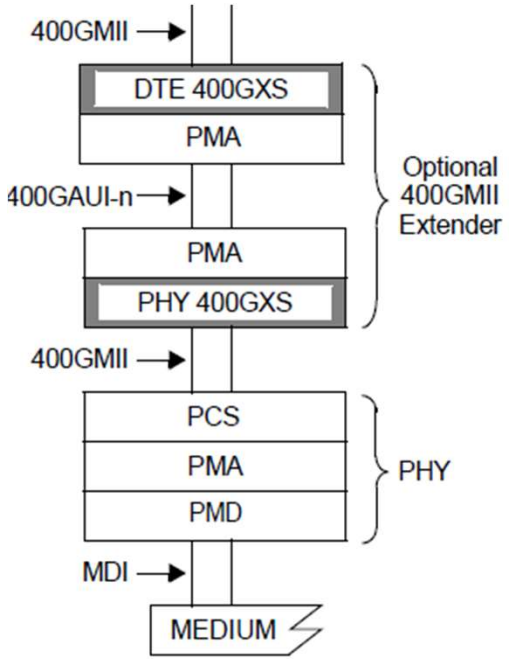
Ref: gustlin_3df_01a_220517

RS/MII

- The RS/MII was changed to be a logical interface (no electrical specification) as part of the 802.3ba (40G/s, 100Gb/s) project.
- The same approach was carried forward for 200GbE and 400GbE in the 802.3bs project.
- Propose that the same approach is used for 800GbE , and that the RS/MII is based on P802.3-2018, Clause 117 “Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII)” with the following changes:
  - ❑ The 800GMII supports a speed of 800 Gb/s
  - ❑ The 800GMII does not support EEE or Low Power Idle (LPI) signaling

MII Extender / Extender Sublayer (XS)

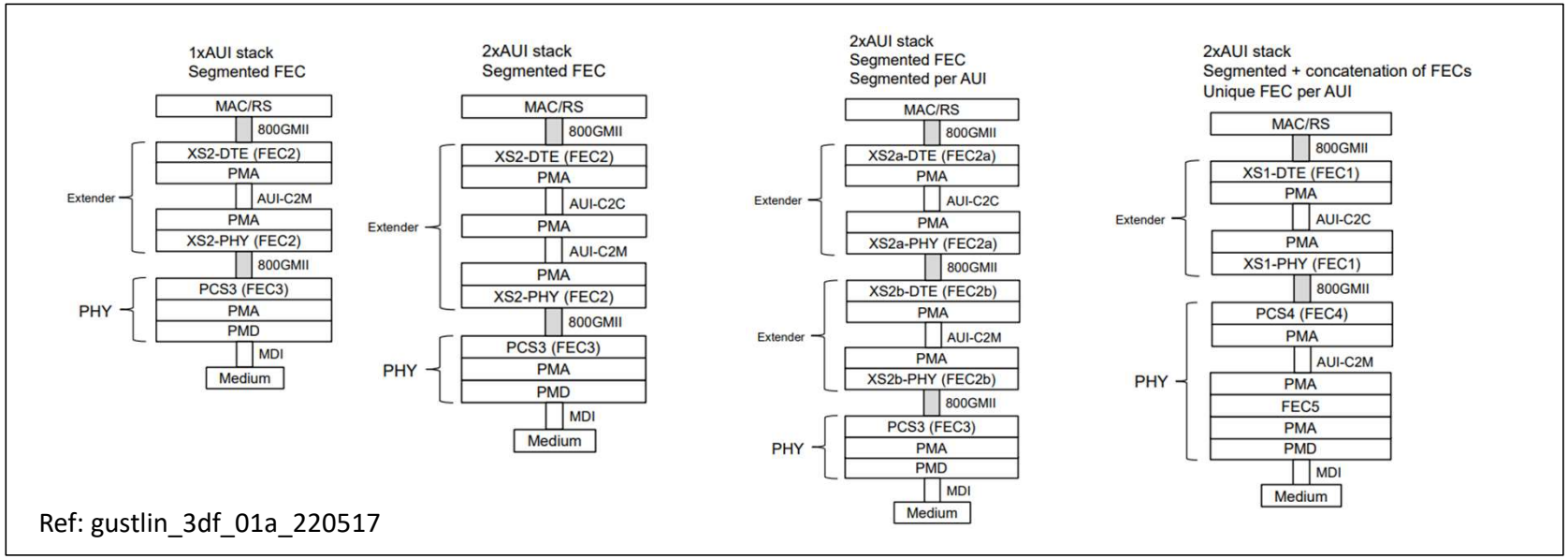
- The concept of an MII Extender (and associated extender sublayers) was first introduced in the 802.3bs (200GbE and 400GbE) project
- The purpose of the MII Extender was to extend the logical MII over an optional physically instantiated AUI, to allow different implementations and/or future PHYs that may require changing FEC (baseline_3bs_0715)
- The MII Extender comprises two sublayers, the “DTE XS” and the “PHY XS”. The “DTE XS” is functionally equivalent to the PCS, whereas the “PHY XS” is an inverted PCS.
- As an example, a MII Extender is used to support one or more optional AUIs with the 400GBASE-ZR PHY defined in 802.3cw.



Ref: 802.3-2018 Clause 118

MII Extender / Extender Sublayer (XS) for 800GbE

- The concept of an MII Extender was also adopted as part of the baseline architecture for 802.3df.
- The primary reason for adopting an MII Extender was to allow the possibility of different FECs for the AUI and the PMD. Some Examples below:



Ref: gustlin_3df_01a_220517

MII Extender / Extender Sublayer (XS) for 800GbE

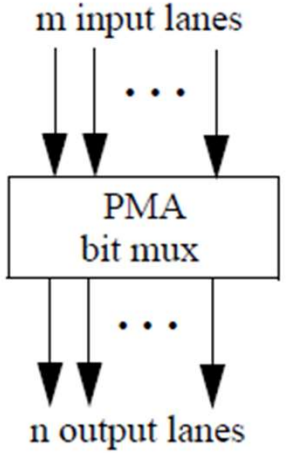
- Propose that the MII Extender for 800GbE using 100G/lane signaling, is based on 802.3-2018 Clause 118 “200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)” with the following changes:
  - ❑ The 800GMII Extender and the 800GXS support a speed of 800Gb/s

Time Synchronization Protocols

- Ethernet support for time synchronization protocols is defined in 802.3-2018 Clause 90 “Ethernet support for time synchronization protocols”
- Propose that this is amended as necessary to support 800GbE using 100G/lane signaling.

PMA

- The concept of a ‘bit muxing” PMA was first adopted in 802.3ba (40GbE and 100GbE) and carried over to 802.3bs (200GbE and 400GbE)
- The PMA accepts m input lanes, where each lane comprises of a bit mux of some number of PCS lanes.
- The PMA first bit demuxes each individual input lane into it’s constituent PCS lanes, and then bit muxes the PCS lanes from all of the input lanes (order not specified) onto the n output lanes.
- The PMA is also responsible for PAM4 encoding and decoding of input and output lanes if required.



Ref: 802.3-2018 Clause 120

PMA for 800GbE

- The 802.3df Task Force has yet to adopt a PCS baseline for 800GbE using 100G/lane signaling.
- There are (at least) two different PCS proposals under consideration, each with a different number of PCS lanes (but all currently assuming a bit muxing PMA).
- Propose that the PMA for 800GbE using 100G/lane signaling, is based on 802.3-2018 Clause 120 “Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R”, but with the number of PCS lanes left as “TBD” and with the following changes:
  - ❑ The PMA supports an aggregate speed of 800Gb/s

Thank You!

Proposed Straw Poll #1

I would support adopting slide 5 of nicholl_3df_logic_01_220623 as the RS/MII baseline, for 800GbE with 100G/lane signaling.

- Y:
- N:
- Need more information:

Proposed Straw Poll #2

I would support adopting slide 8 of nicholl_3df_logic_01_220623 as the MII Extender / Extender Sublayer (XS) baseline, for 800GbE with 100G/lane signaling.

- Y:
- N:
- Need more information:

Proposed Straw Poll #3

I would support adopting slide 9 of nicholl_3df_logic_01_220623 as the Time Synchronization Protocol baseline, for 800GbE with 100G/lane signaling.

- Y:
- N:
- Need more information:

Proposed Straw Poll #4

I would support adopting slide 11 of nicholl_3df_logic_01_220623 as the PMA baseline, for 800GbE with 100G/lane signaling.

- Y:
- N:
- Need more information: