

BER and FLR Analysis of Random and Burst Errors for 800GbE, 8x100 PCS Options

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IEEE 802.3df Logic Ad Hoc

Contributors

- <TBA>

BER and FLR Targets

- BER Objective for 802.3df:
 - “Support a BER of better than or equal to 10^{-13} at the MAC/PLS service interface (or the frame loss ratio equivalent)”
- FLR Target = 6.2×10^{-11} based on BER of 10^{-13}
 - Frame Loss Ratio for 64B packets with minimum IPG
 - $FLR = BER * 620$
 - Reference: Eq. (2) on slide 9 of [anslow 01 0613 logic.pdf](#)

Random Error Calculations

- Calculating the FLR from BER_{in} for random errors:
 - References:
 - [anslow_3bs_02_1114.pdf](#) - slide 11
 - [anslow_01a_1112_mmf.pdf](#) - slide 6
 - [anslow_102616_3cd_adhoc.pdf](#) – slide 3
 - Symbol Error Ratio: $SER = 1 - (1 - BER_{in})^{10}$
 - Codeword Error Ratio: $CER = \sum_{i=t+1}^N \binom{N}{i} SER^i (1 - SER)^{N-i}$ $N=544, t=15$ for RS(544,514)
 - Frame Loss Ratio: $FLR = CER * (1 + X * MFC) / MFC$
 - MFC = MAC frames per codeword
 - One RS(544) CW can hold exactly eight 64B packets (MFC=8)
 - X = X CW FEC interleave (X = 1, 2, or 4)
- FEC “blast radius” and X CW FEC interleave scaling
 - FLR Scaling Factor: $FSF = (1 + X * MFC) / MFC$
 - Single FEC (no interleave): $FLR = 1.125 * CER$
 - 2 CW FEC interleave: $FLR = 2.125 * CER$
 - 4 CW FEC interleave: $FLR = 4.125 * CER$

Calculated FLR for Random Error Input

- 100G/lane PMDs assume $BER_{in} = 2.4E-4$ or better.
 - See “Bit Error Ratio” in Clauses 124, 140, 151, etc.
 - Expand requirement to include two AUI on each end of the link, adds $4 * 1E-5 = 2.8E-4$

RS(544,514)	BER_{in}	SER	CER	FSF	FLR
No Interleave	2.8E-4	2.8E-3	7.86E-12	1.125	8.84E-12
2 CW interleave	2.8E-4	2.8E-3	7.86E-12	2.125	1.67E-11
4 CW interleave	2.8E-4	2.8E-3	7.86E-12	4.125	3.24E-11

- For input BER of 2.8E-4, all above RS FEC interleaves have FLR better than 6.2E-11
- Both 2 CW and 4 CW Interleave meet the BER/FLR requirement for random errors.

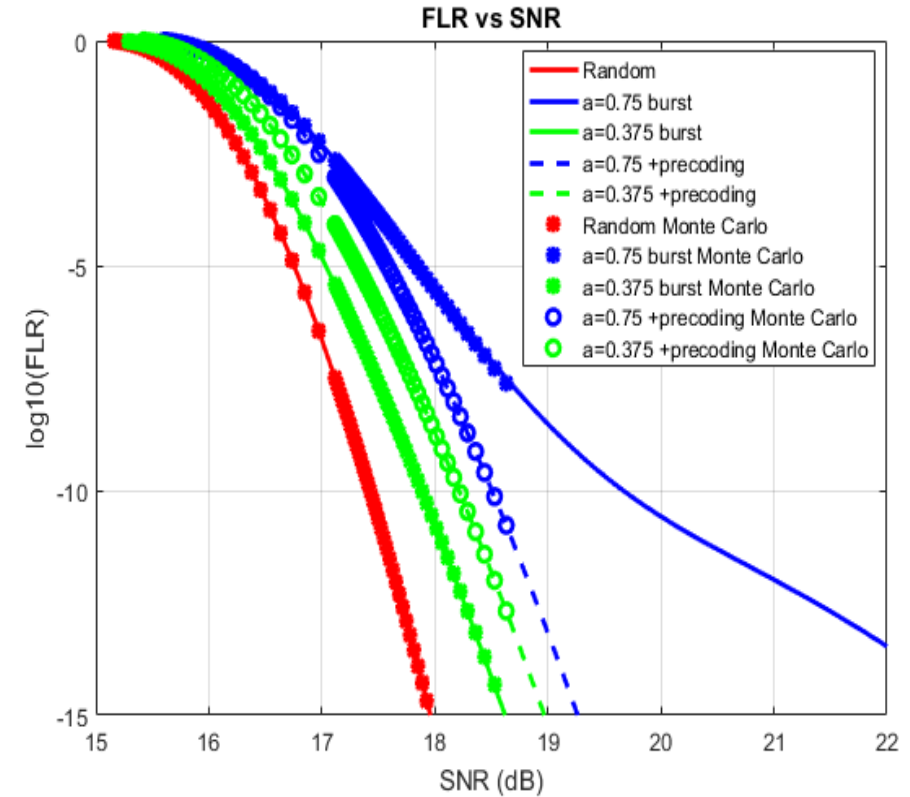
BER_{in} and SNR Requirements with Random Errors

RS(544,514) FEC	FLR Target	FSF	CER Required	BER_{in} Required	PAM4 DER Required	SNR (dB) Required
No Interleave	6.2E-11	1.125	5.49E-11	3.20E-4	6.40e-4	17.45
2 CW Interleave	6.2E-11	2.125	2.92E-11	3.06E-4	6.13E-4	17.48
4 CW Interleave	6.2E-11	4.125	1.50E-11	2.93E-4	5.85E-4	17.52

- Even if BER_{in} is worse than 2.8E-4, all Interleaves meet the 6.2E-11 FLR Target
- SNR increase to meet the same FLR from 2-way to 4-way FEC interleave is $\approx 0.04\text{dB}$ (negligible)

Burst Error Model

- Monte Carlo simulation
 - Apply real random data and DFE tap coefficients
 - Gaussian noise added at the slicer for certain DER0 (1e-4)
 - Insert initial error and capture burst error events through DFE error propagation
 - Extrapolate error signatures over $>10^7$ error events
 - The error signature, $\{p(1), p(2), p(3), \dots, p(t)\}$, is the probability of a burst error causing 1, 2, 3, ... RS symbol errors given an initial error
 - Post-FEC performance with RS(544,514) can be calculated
- Different coding schemes can be implemented
 - Precoding
 - PMA multiplexing
 - Codeword interleaving



Good match between Monte Carlo (*)
and Anslow's analytical models (-)

https://www.ieee802.org/3/cd/public/July16/anslow_3cd_01_0716.pdf

C. Liu, "100+ Gb/s Ethernet Forward Error Correction (FEC) Analysis", DesignCon 2019

8x100 PCS Options for Burst Error Analysis

PCS Option 1: 2 CW Interleave

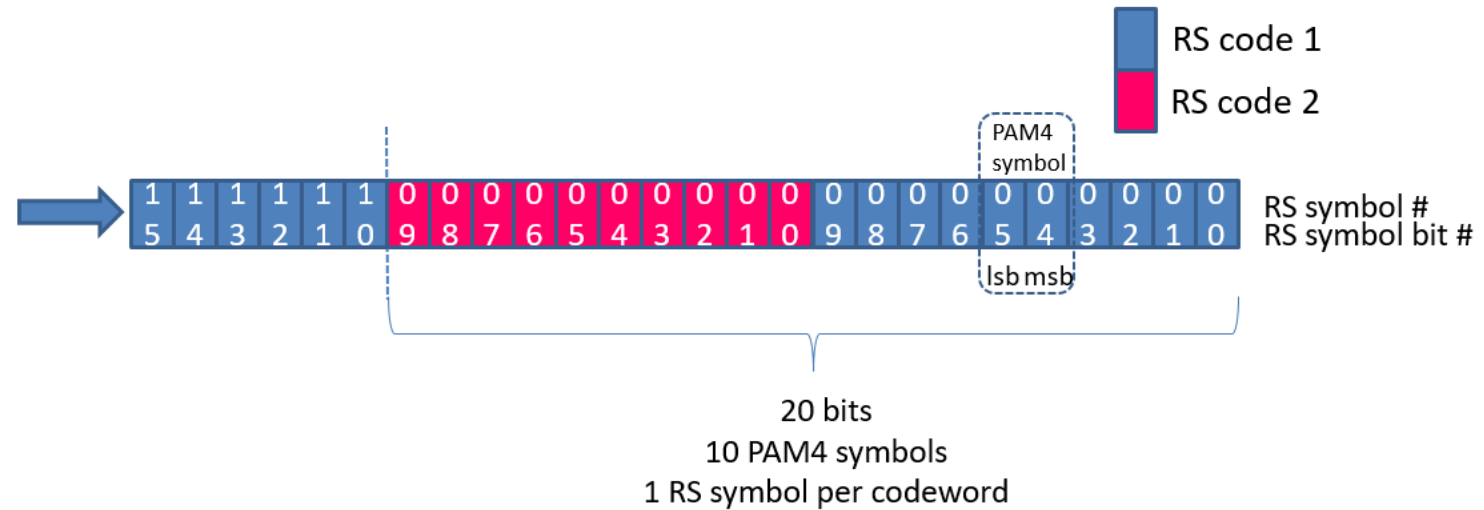
- Baseline proposal from:
 - [wang 3df logic 220623a.pdf](#)
 - 2 CW same as 200GE in CL 119
- Option 1.a
 - 2 CW, 8 PCS lanes, No bitmux
 - This is the proposal
- Option 1.b
 - 2 CW, 16 PCS lanes, 2:1 bitmux
 - Modified for comparison

PCS Option 2: 4 CW Interleave

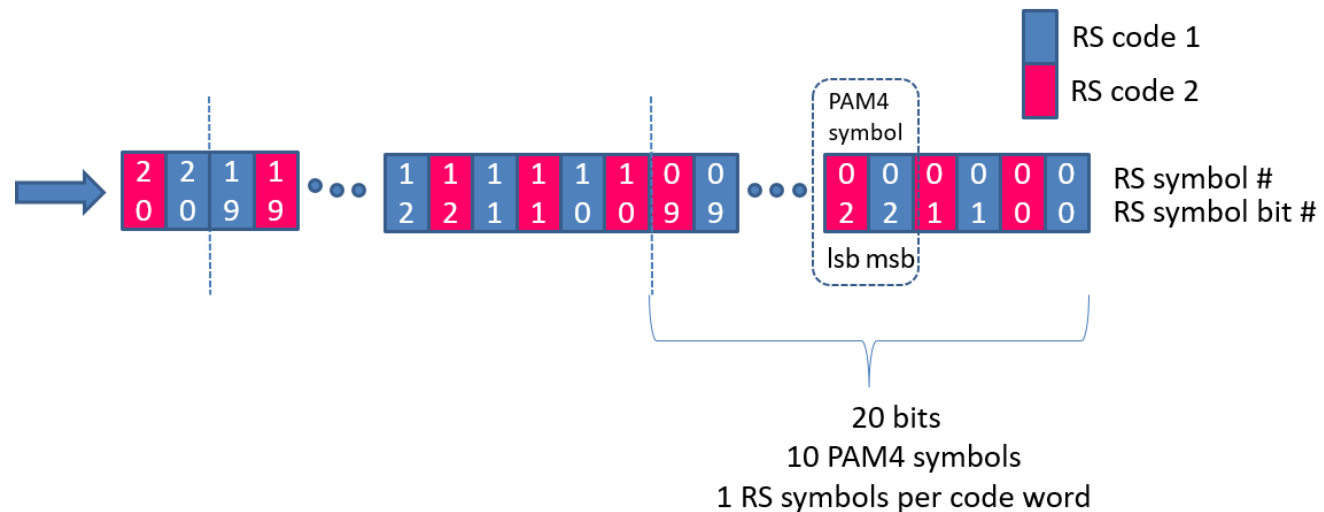
- Baseline proposal from:
 - [shrikhande 3df 01b 220517.pdf](#)
 - 4 CW in two 400G flows of 2 CW each
- Option 2.a
 - 4 CW, 32 PCS lanes, 4:1 bitmux
 - 4:1 bitmux within each 400G flow
 - Each PMD lane has bits from 2 CWs
- Option 2.b
 - 4 CW, 32 PCS lanes, 4:1 bitmux
 - 4:1 bitmux across 400G flows
 - Two lanes from each 400G flow in each set of four PCS lanes bitmux together
 - Each PMD lane has bits from all 4 CWs

Per-Lane Bit Order – Option 1

- Option 1.a:
 - CI = 2
 - BM = none



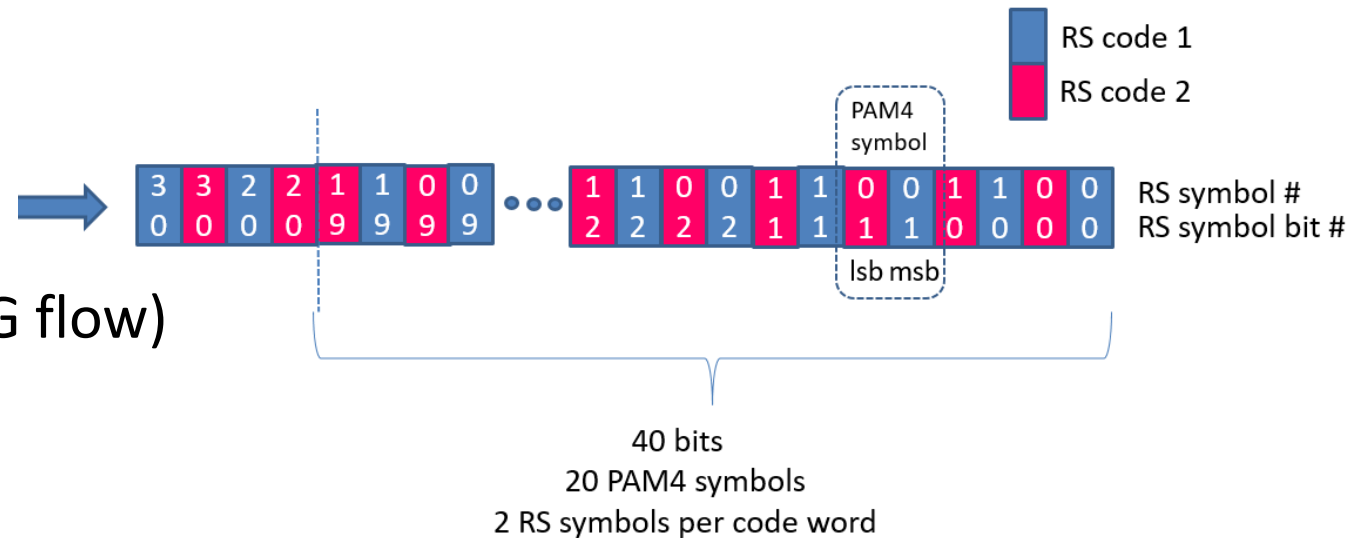
- Option 1.b:
 - CI = 2
 - BM = 2:1



Per-Lane Bit Order – Option 2

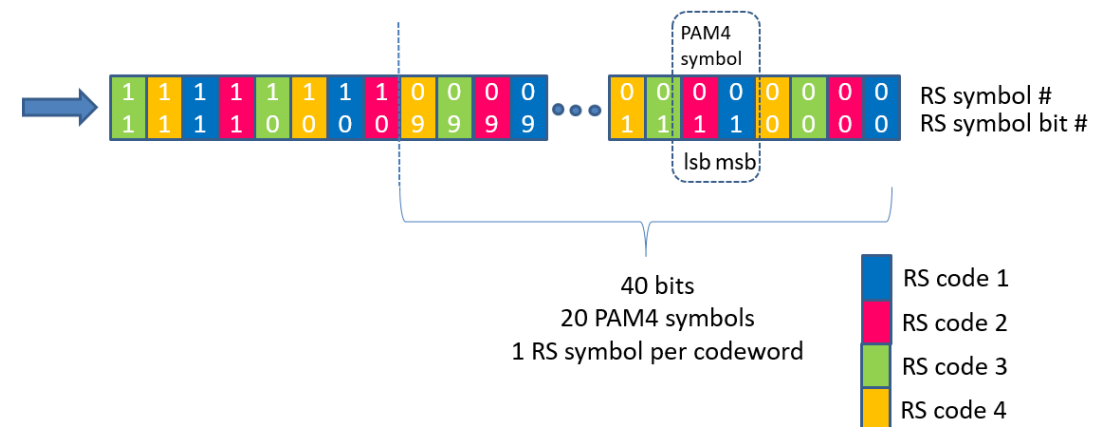
• Option 2.a:

- CI = 2 (single 400G flow)
- BM = 4:1 (4 from same 400G flow)



• Option 2.b:

- CI = 4 = 2 x 2 in parallel
- BM = 4:1 (2 from each 400G flow)

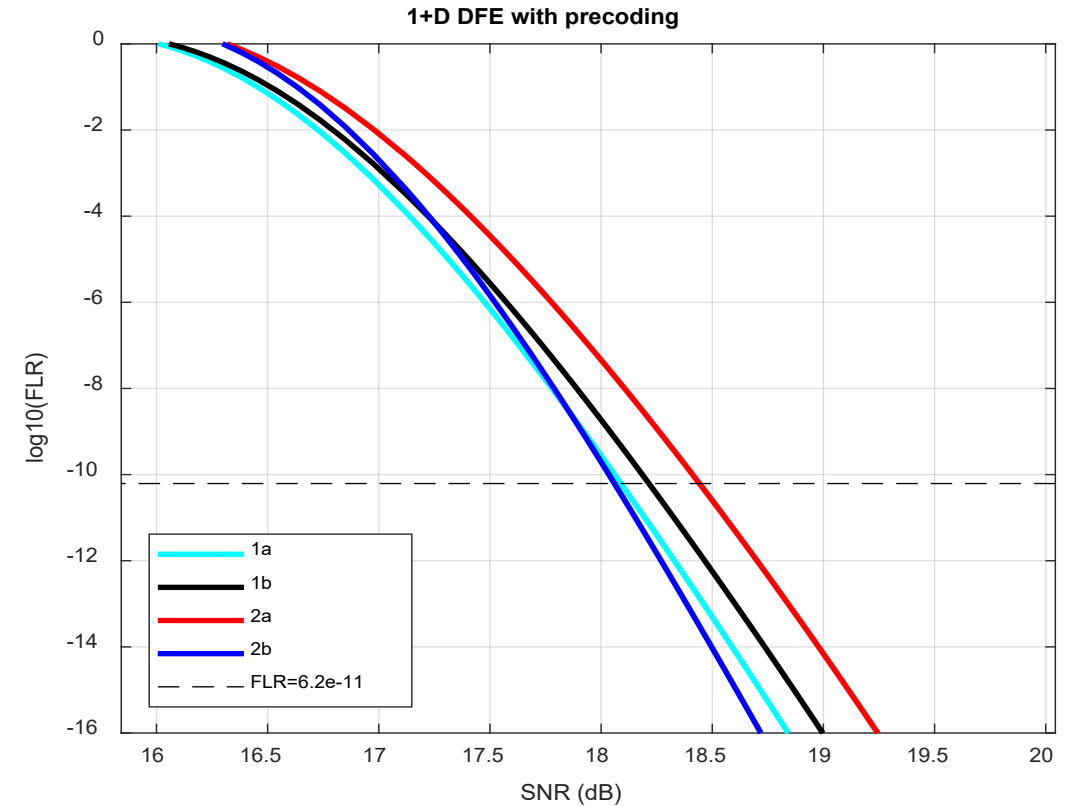
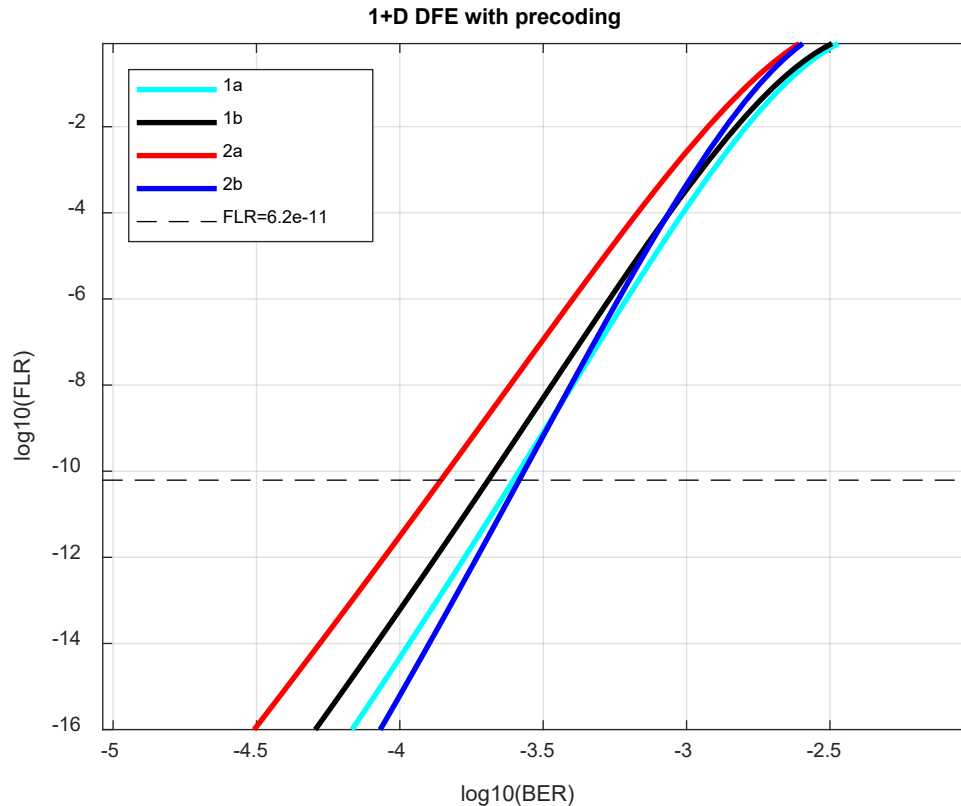


Burst Error Results for 8x100 PCS Options

Option	Required FLR	1+0.1D no precoding (a=0.01)		1+0.5D no precoding (a=0.375)		1+D with precoding (a=0.75)	
		Required SNR	Required DER	Required SNR	Required DER	Required SNR	Required DER
1.a	6.20E-11	17.49	6.09E-04	17.57	5.40E-04	18.09	2.49E-04
1.b	6.20E-11	17.49	6.07E-04	17.79	3.96E-04	18.22	2.03E-04
2.a	6.20E-11	17.52	5.79E-04	18.41	1.48E-04	18.44	1.39E-04
2.b	6.20E-11	17.52	5.80E-04	17.83	3.69E-04	18.06	2.61E-04

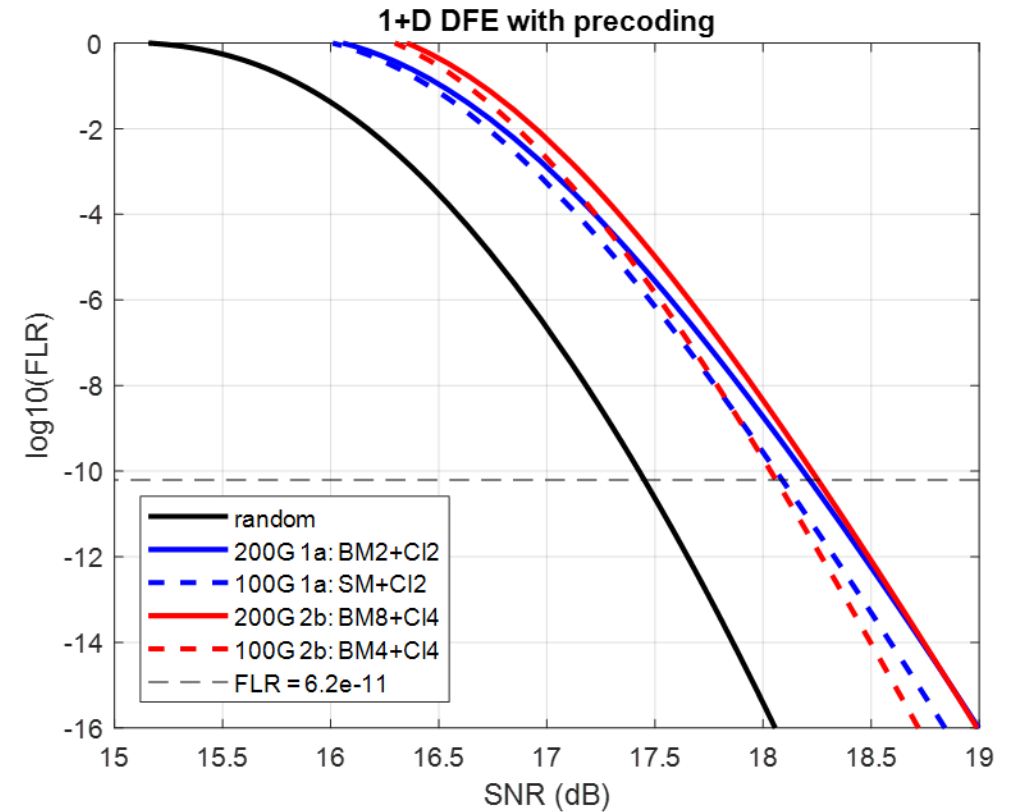
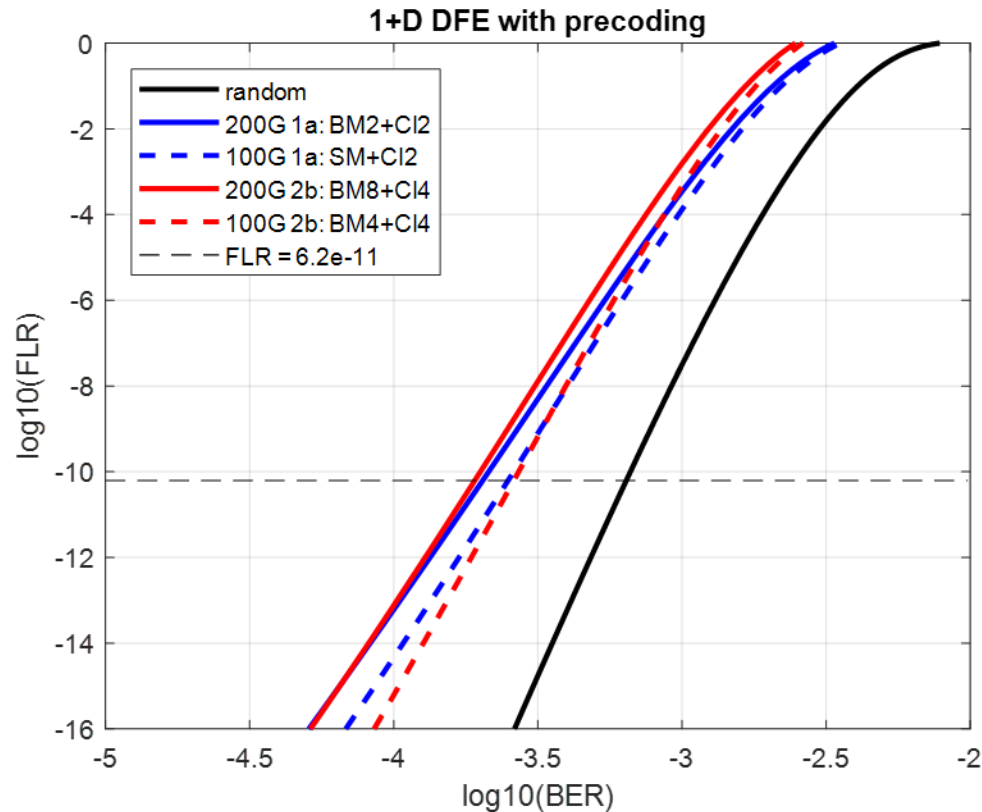
- 1+0.1D : Nearly random (a=0.01)
 - Option 1.a, 2 CW interleave, is 0.03dB better than 4 CW Interleave
- 1+D : High burst correlation (a=0.75)
 - Option 2.b, 4:1 bitmux across 4 CW, is best option by 0.03dB

FLR for Burst Errors with High Correlation



Ethernet compliant implementations must be below the $FLR=6.2E-11$ dotted line.
Option 2.b gets more advantageous as actual FLR decreases.

Looking toward 200G/lane PCS Options



Possible scaling from 8x100 to 4x200: Option 1.a: SM+CI2 → BM2+CI2
Option 2.b: BM4+CI4 → BM8+CI4

Very similar SNR required

Summary

- Both options meet the FLR requirement for Random Errors
 - Fewer CW Interleave is better for Random Errors due to FSF
 - Option 1 is better than Option 2 at the target FLR, but only slightly (0.04dB)
- Higher CW Interleave benefit can overcome higher bitmux ratio penalty for Correlated Burst Errors
 - Option 2.b is better than Option 1.a at target FLR of $6.2E-11$
 - But only slightly better (0.03dB)
- Option 1 and Option 2 are very close in FEC Performance
 - Option 2 can realize improved FEC gain by implementing “Cross Flow” bit mux (Option 2.b)
 - Options 2.a and 2.b are compatible with each other since RX reorders across all PCS lanes
- Future evaluations for 200G/Lane should look at other muxing options
 - For example: FEC symbol muxing or PAM4 symbol muxing in addition to bit muxing
 - Applies to 200GbE and 400GbE as well as 800GbE and 1.6TbE

Thank You.