

Comparison of Two 800GbE PCS and PMA Baseline Proposals for 100 Gb/s per lane PHYs

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Introduction

- A baseline specification is required for 800 Gb/s PCS/PMA that will be used for 100 Gb/s per lane (and possibly other) PMDs.
- Two baseline proposals have been presented to the Task Force.
- This presentation provides a concise comparison of the two proposals.

Two 800GbE PCS/PMA Baseline Proposals

Proposed Next Steps – Generate D1.0 based on 100 Gbps/lane progress

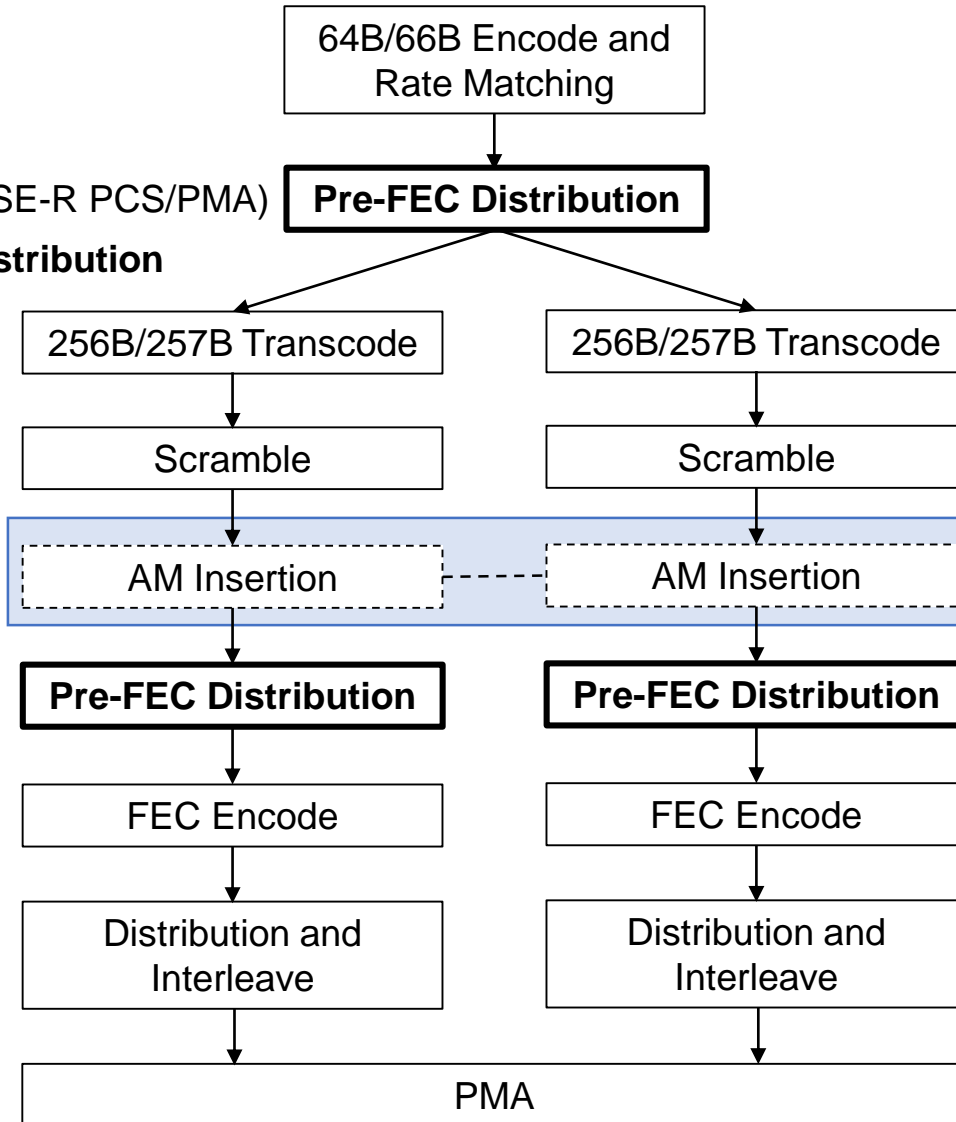
- See slides #3 and #5 for summary of what we have.
- What could D1.0 address at this time?
 - 800 GE introduction
 - 800 GE logic stack from RS to PMA, including FEC defined for 100 Gb/s per lane
 - all 100 Gbps/lane based PMDs for 400 GbE and 800GbE
 - 100 Gbps/lane AUIs for 800GbE
- What is missing at this time for the proposed D1.0?
 - For 800 GbE
 - logic stack, including FEC for 100 Gb/s per lane
 - Decision on FEC form, 2x Clause 119 or sped up Clause 119 ?
 - 100 Gb/s per lane KR/CR training details
 - 100 Gb/s per lane KR/CR auto-negotiation details
 - 100 Gb/s per lane CR MDI details
 - 100 Gb/s per lane Optical PMD MDI details
 - For 400 GbE
 - 400GBASE-DR4-2 PMD

References

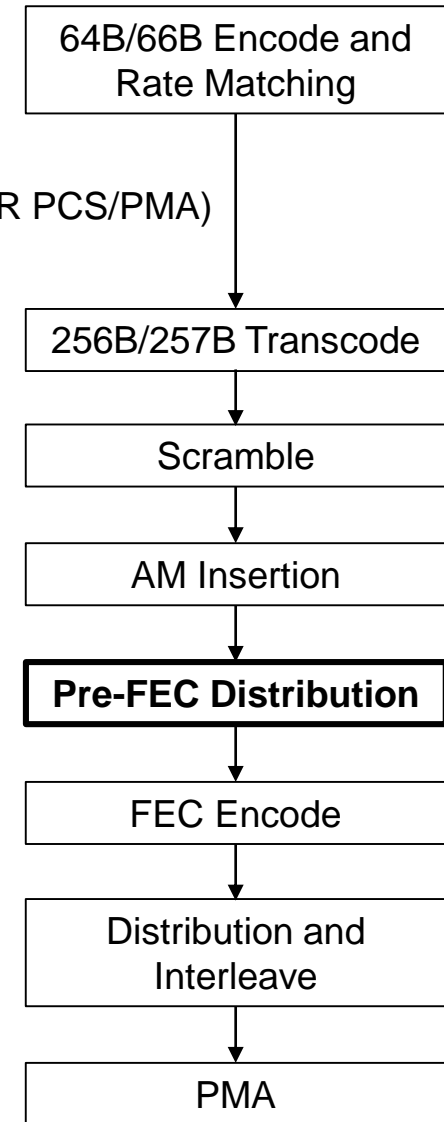
- Previous contributions in Task Force relating to the 800 Gb/s PCS/PMA baseline are listed here:
 - Option 1: 2X parallel Clause 119 (400GBASE-R PCS/PMA)
 - https://www.ieee802.org/3/df/public/22_03/shrikhande_3df_01_220329.pdf
 - https://www.ieee802.org/3/df/public/22_05/22_0517/shrikhande_3df_01a_220517.pdf
 - Option 2: Sped up Clause 119 (200GBASE-R PCS/PMA)
 - https://www.ieee802.org/3/df/public/22_03/wang_3df_01a_220308.pdf
 - https://www.ieee802.org/3/df/public/22_05/22_0517/he_3df_01_220517.pdf
 - https://www.ieee802.org/3/df/public/adhoc/logic/22_0623/wang_3df_logic_220623a.pdf

Comparison of Candidate Options: Functional View

Option 1:
2X CL119 (400GBASE-R PCS/PMA)
2 steps Pre-FEC distribution



Option 2:
Sped up CL119 (200GBASE-R PCS/PMA)
1 step Pre-FEC distribution



Comparison of Candidate Options: Parameter View

	Option 1: 2X CL119	Option 2: Sped up CL119
Number of FEC codewords	4X	2X
Interleave	2X	2X
Latency	$\geq a+12.8\text{ns}$	a
BER(Bit Error Ratio)	1.00E-13	1.00E-13
FLR(Frame Loss Ratio)	1.24E-10	6.20E-11
Number of PCS lanes	32 PCS lanes @ 25 Gb/s	8 PCS lanes @ 100 Gb/s
Support 25/50 Gb/s per lane	Yes	No
Number of Alignment Markers	32	8
PMA	4:1 for 100 Gb/s per lane	1:1 for 100 Gb/s per lane
Clock content challenge	Need further work	No
Reuse of implementation	Largely (replication/muxing)	Largely (speed-up)
Reuse of standard specification	Largely	Completely
Fast time to market	Yes	Yes

Option 1 Advantages

- Support 50 Gb/s and 25 Gb/s per lanes.
 - However, there are no plans and objectives to define specifications for electrical or optical interfaces using these lane rates.
- Can partially reuse 400GBASE-R PCS/PMA design without speed-up as in [shrikhande_3df_01a_220517](#), with following exceptions.
 - “AM values are made unique across the two flows”
 - “AM insertion is aligned across the two flows”
 - “AM lock: per lane, same as CL119”
 - “De-skew: across 32 PCS lanes”
 - Reorder across 32 PCS lanes.
 - “Minor modification” on CL 119 state diagrams.

Option 2 Advantages

- Lower digital resources:
 - Less storage required (2 codewords rather than 4).
 - Fewer PCS lanes to manage (synchronization, states, etc.).
- Low FLR for same pre-FEC BER and BER Objective.
- RS(544,514) FEC symbol interleave from 2 codewords in each 100 Gb/s PCS lane.
- Known low clock content penalty due to alignment markers.
- Lower latency.
- Almost 100% reuse of IEEE 802.3bs CL119 specifications (just increase speed).
- Fast time to market for all.
 - Reuse of 200GBASE-R PCS/PMA design and test benches.

Conclusion

- The technical advantages of option 2 (4X speed-up 200GBASE-R PCS/PMA) are numerous.
- 800 Gb/s Ethernet is only now being defined and has a long life ahead.
 - Choosing the better technical solution NOW is important.

Thanks!