On clock content issue over two parallel 400G PCS flows

Ryan Wong (Broadcom)
June 30, 2022
IEEE 802.3 df Logic Ad Hoc

Introduction

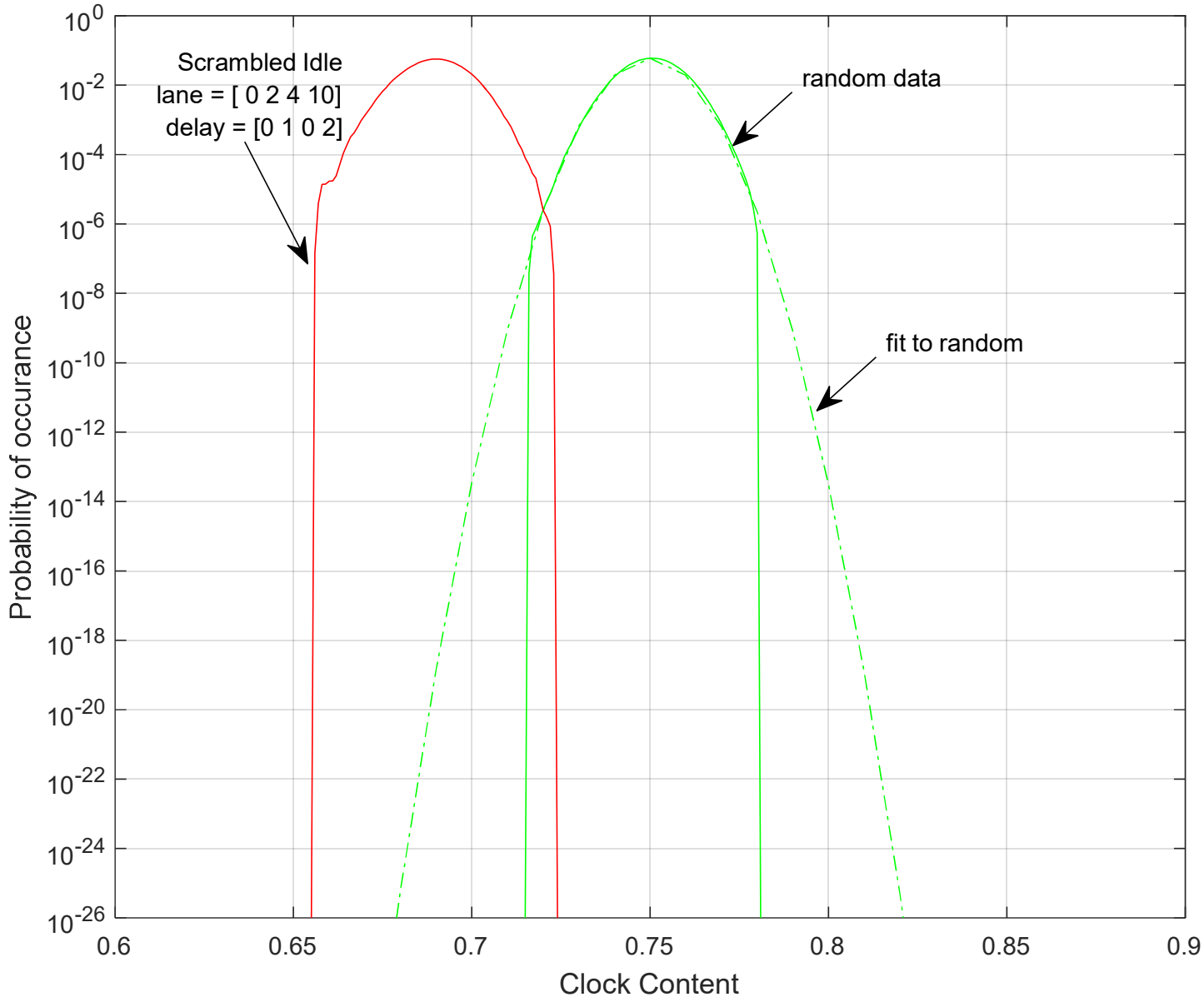
- For a few “rogue” combinations of 4 PCS lanes with particular relative delays over 200GbE and 400GbE, the entire distribution of clock content for scrambled idle data shifts to lower values for both “symmetric transitions through average” and the “all transitions” plots.
  - There is some loss of clock content for these “rogue” cases.
  - No fixes were added to the standard.

– References

  - For clock content definition, anslow_01_1016_logic
  - For issue of unusual clock content, anslow_01_121916_elect.pdf
  - For impact on CDR/test pattern, ghiasi_02_0317_logic.pdf
  - For theoretical analysis, wertheim_3bs_01_0317.pdf
  - For possible solutions, gustlin_3bs_02_0317.pdf

400GbE clock content, all transitions

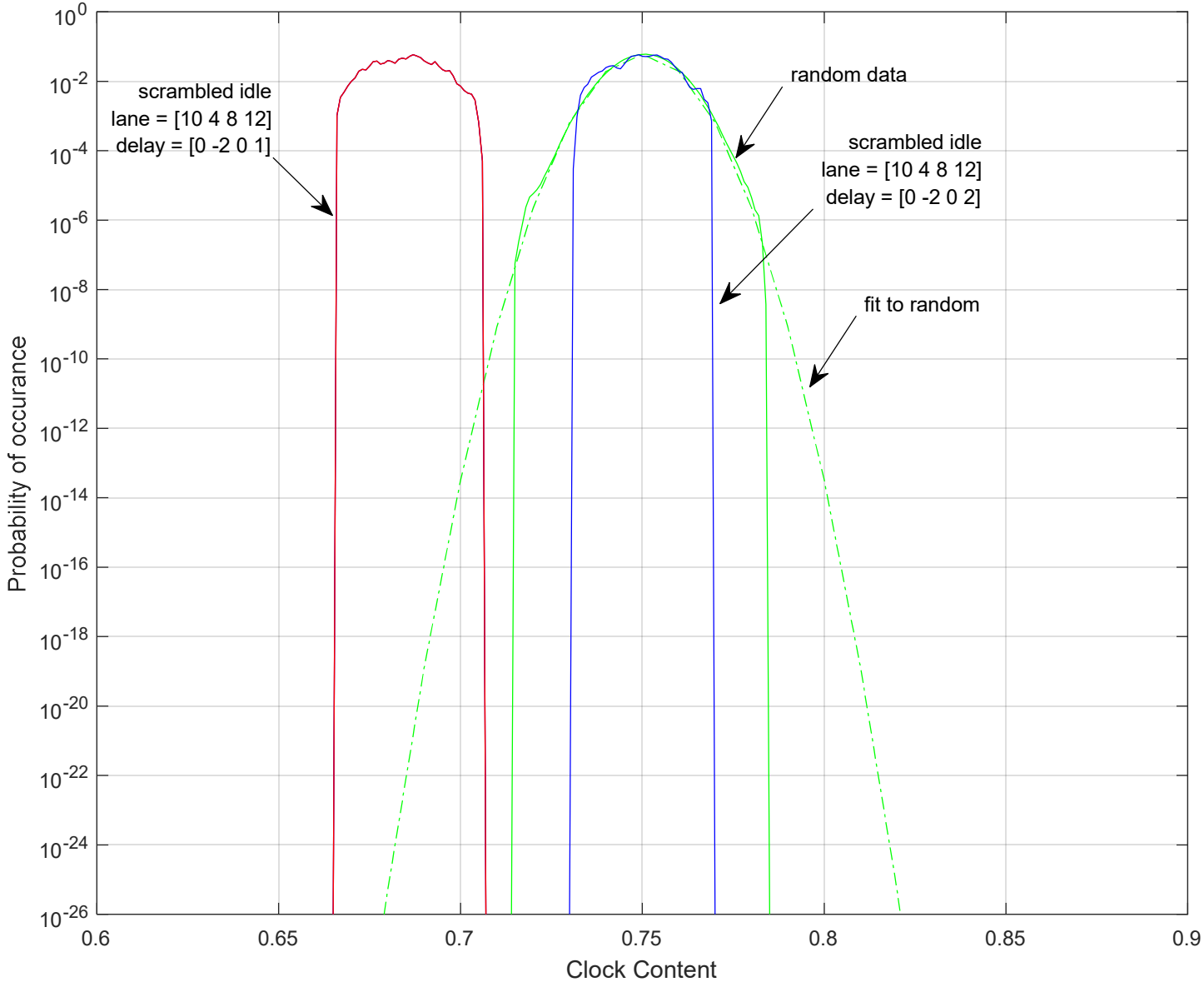
-Lane=[0, 2, 4, 10]/Delay=[0, 1, 0, 2]



TWO PARALLEL 400G PCS FLOWS

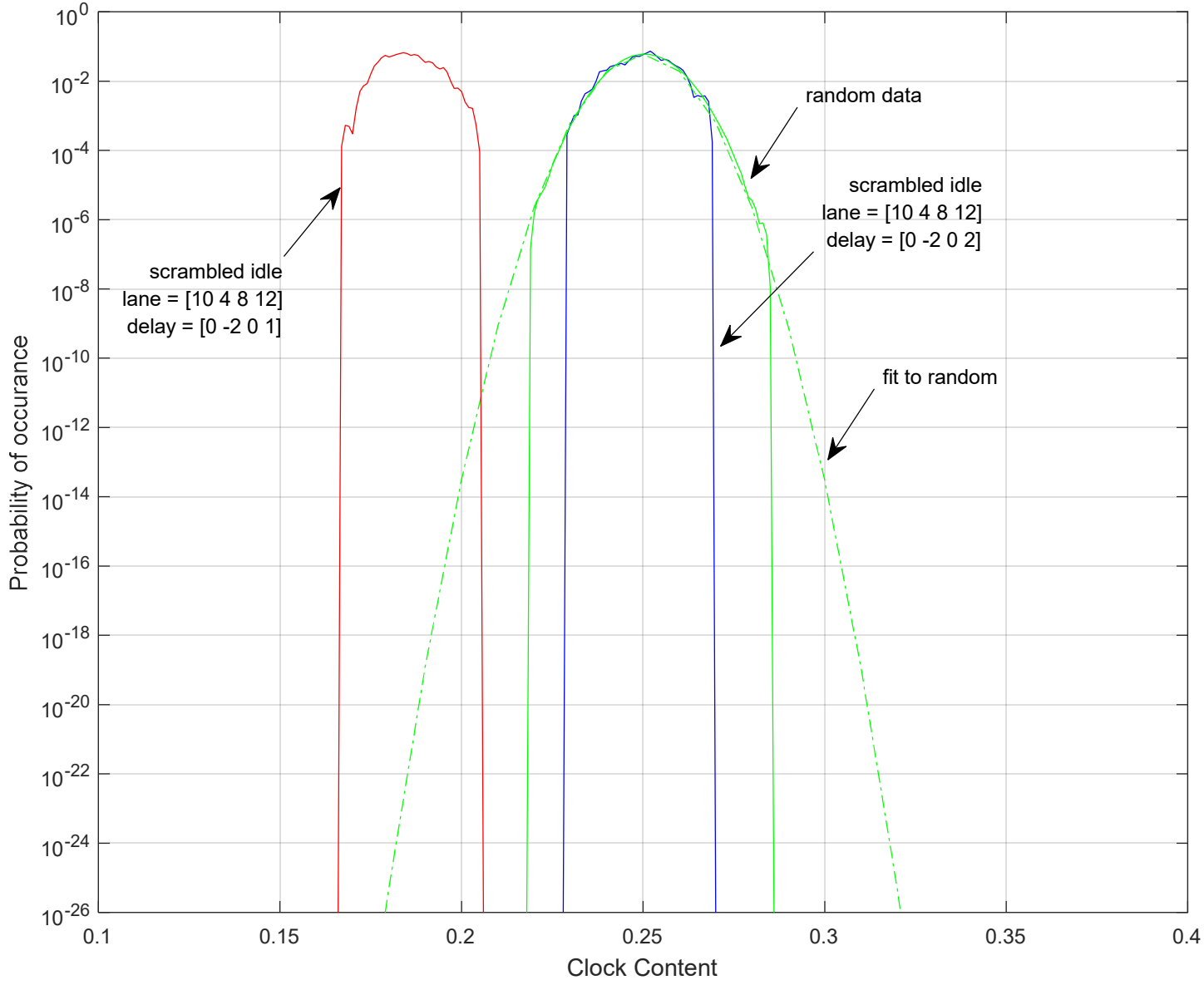
800GbE clock content, all transitions

-Lane=[10, 4, 8, 12]/Delay=[0, -2, 0, 1]



800GbE clock content, symmetric transitions

-Lane=[10, 4, 8, 12]/Delay=[0, -2, 0, 1]



800GbE search

- Combinations of 800GbE PCS lanes for 4:1 bit interleaving to form 100Gb/s lanes were searched to find any unusual clock content with delays between -10 to +10 bits. Gray coding and PAM4 were assumed.
  - For all possible combinations from lanes 0-15 (flow #1), 2356 out of 404,520,480 possibilities were identified as having unusual clock content similar to the plots shown in the previous slides.
  - For all possible combinations from lanes 16-31 (flow #2), the search gave the same results as lanes 0-15 as they are two 400G PCS flows.
  - For all natural pairs from lanes 0-15 and lanes 16-31 (e.g. [0 1 16 17],[2, 3, 16, 17],……,[14 15 30 31]), the search did not find any with unusual clock content out of 14,224,896 possibilities
  - For all pairs from lanes 0-15 and the “equivalent” pairs from 16-31 (e.g. [0 1 16 17],[0 2 16 18],……,[14 15 30 31]), the search did not find any with unusual clock content out of 26,671,680 possibilities

Summary

- A search of combinations of 800GbE PCS lanes for 4:1 bit interleaving to form 100Gb/s lanes were carried out to identify cases with unusual clock content.
- The issue of unusual clock content for two parallel 400G PCS flows is the same as that of 400GbE.

THANK YOU