Thoughts on PCS, PMA Skew Limits for 800 Gb/s Ethernet

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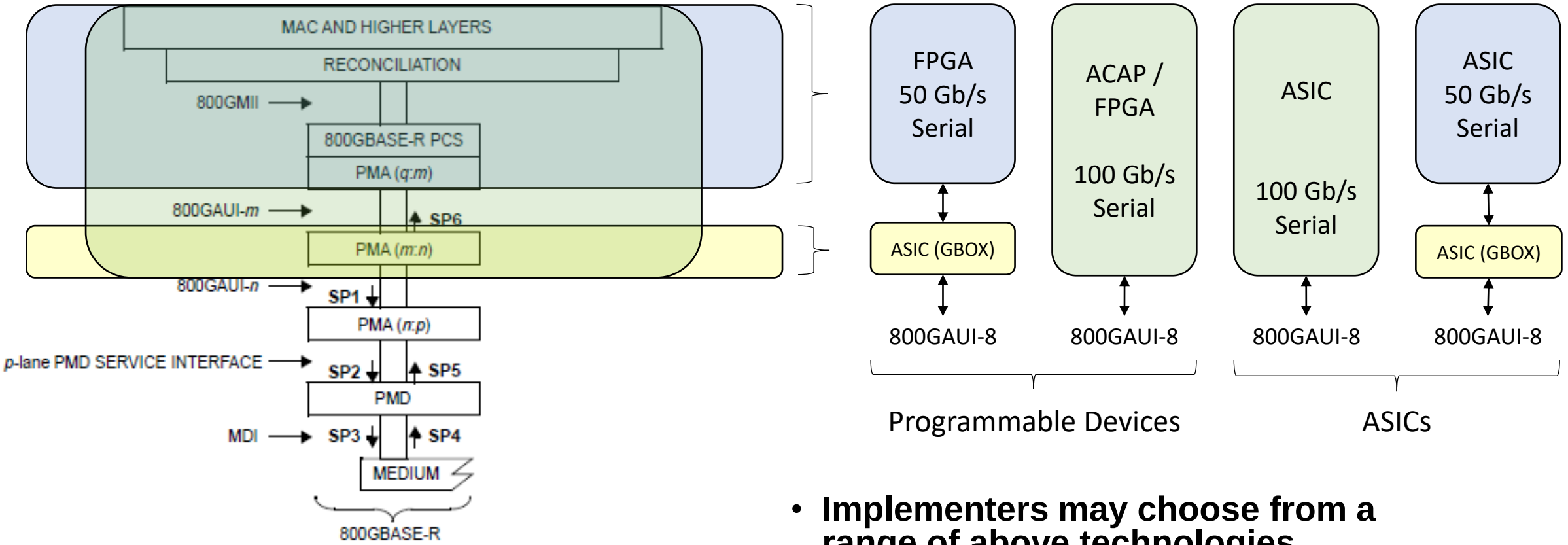
IEEE P802.3df Logic Ad Hoc

Background

- **Discussion in ran_3df_03_230130.pdf proposed new values for maximum skew**
  - Proposed updates to P802.3df Table 169-5 – Summary of Skew constraints for 800GBASE-R
  - The presentation contains several links to previous presentations
    - Those previous slides show the origin of the maximum skew values found in P802.3df/D1.1
- **This presentation takes another look at the 800 Gb/s Ethernet PCS and PMA skew constraints**
- **Consideration is given to implementations across multiple technologies**
  - Programmable devices (FPGA, ACAP)
  - Application specific devices (ASIC)

Technology Choices – PCS, PMA

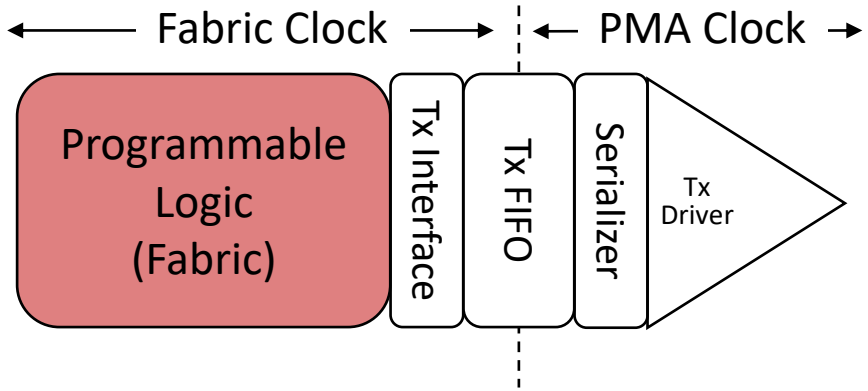


Source: Excerpt from Figure 169-5 P802.3df/D1.1

- **Implementers may choose from a range of above technologies**
  - To enable implementation freedom, maximum skew constraints should permit many possibilities

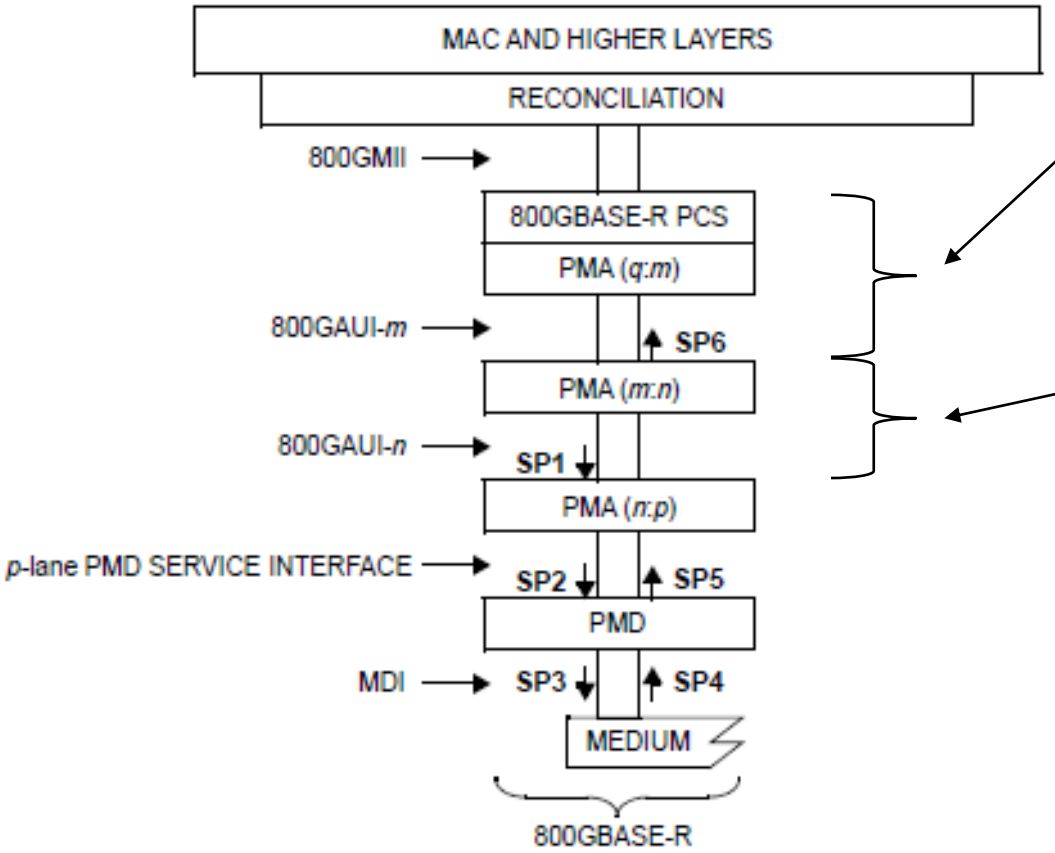
Programmable Devices – Flexibility

- **Programmable devices offer significant flexibility to implementers**
  - Serial transceiver supports many interface width options on the interface to the programmable logic (fabric)
  - Logic for MAC/RS/PCS/FEC can be implemented in the fabric
- **The table shows a representative set of supported configurations**
  - Device A
    - Supports 53.125 Gb/s rate
  - Device B
    - Supports 53.125 and 106.25 Gb/s rates
- **PMA internal clock cycle of 2.4 ns**
  - One FIFO entry



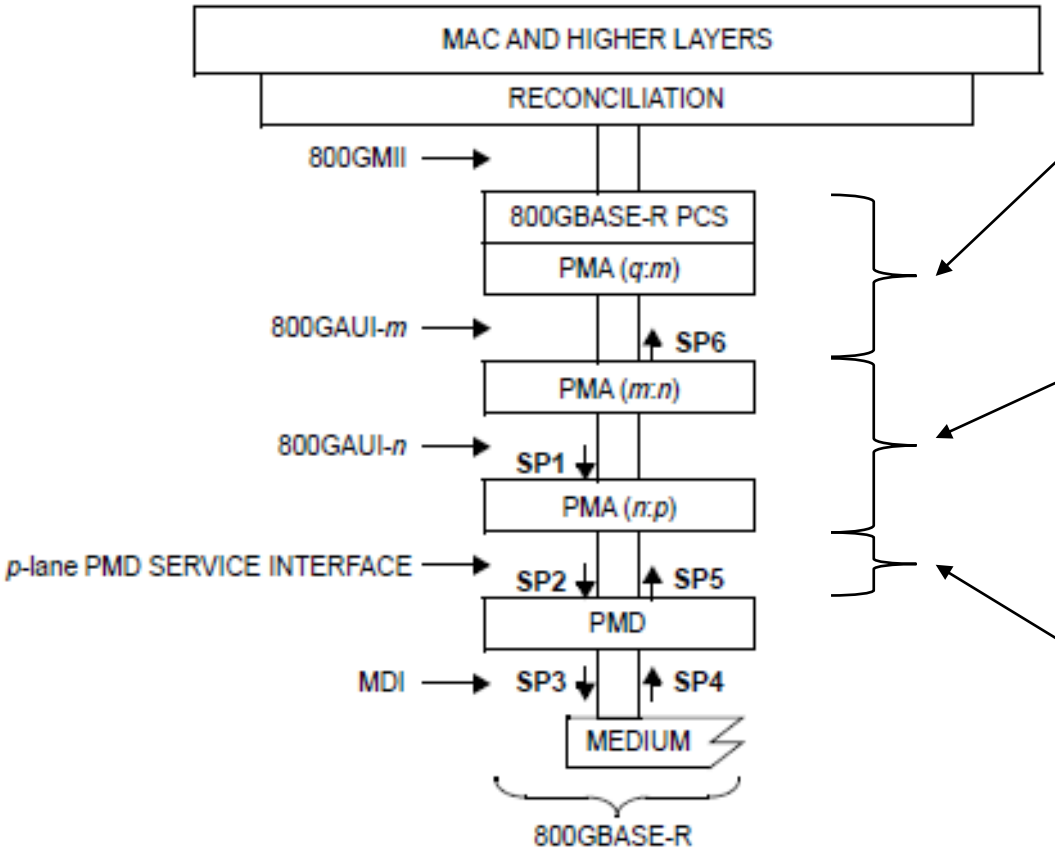
Example Device	Serial Rate (Gb/s)	Fabric I/F Width (bits)	Fabric Clock Freq (MHz)	PMA Internal Data Width (bits)	PMA Internal Clock (MHz)	One PMA Internal Cycle (ns)
A, B	53.125	80	664.063	128	415.039	2.409
A, B	53.125	128	415.039	128	415.039	2.409
A, B	53.125	160	332.031	128	415.039	2.409
A, B	53.125	256	207.520	128	415.039	2.409
B	106.25	320	332.031	256	415.039	2.409
B	106.25	512	207.52	256	415.039	2.409

Contributors to Tx skew



- **Tx PCS, FEC, PMA(q:m), and 800GAUI-m**
  - 2.4 ns (128 bits) due to FIFO fill difference
  - 2.4 ns (128 bits) due to serializer
  - Small amount of package Tx trace mismatch
  - 0.88 ns (board trace mismatch up to 4”)
- **Tx PMA(m:n) and 800GAUI-n**
  - Small amount of package Rx trace mismatch
  - 2.4 ns (128 bits) due to deserializer
  - 2.4 ns (128 bits) due to FIFO fill difference
  - 2.4 ns (128 bits) due to serializer
  - Small amount of package Tx trace mismatch
  - 0.44 ns (board trace mismatch up to 2”)
- **At SP1, estimate a maximum 13.32 ns of skew**
  - Propose 15 ns

Contributors to Rx skew



- **Rx 800GAUI-m, PMA(q:m), FEC, PCS**
  - 0.88 ns (board trace mismatch up to 4”)
  - Small amount of package Rx trace mismatch
  - 2.4 ns (128 bits) due to FIFO fill difference
  - 2.4 ns (128 bits) due to deserializer
- **Rx 800GAUI-n, PMA(m:n)**
  - 0.44 ns (board trace mismatch up to 2”)
  - Small amount of package Rx trace mismatch
  - 2.4 ns (128 bits) due to deserializer
  - 2.4 ns (128 bits) due to FIFO fill difference
  - 2.4 ns (128 bits) due to serializer
  - Small amount of package Tx trace mismatch
- **PMD service interface, PMA (n:p)**
  - Unquantified skew
- **Beyond SP6, estimate a maximum 5.68 ns of skew**
  - Propose 8 ns

Proposed Skew Values for Table 169-5

Between Skew Points	Existing Maximum Skew (ns)	Existing Maximum Skew for 800GBASE-R PCS lane (UI)
PCS Tx to SP1	29	≈ 770
SP6 to PCS Rx	20	≈ 531

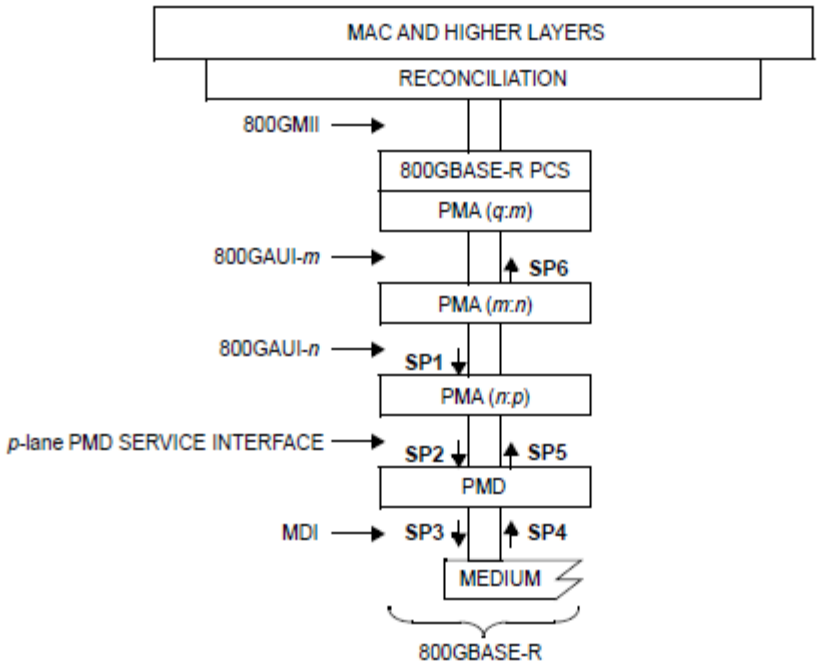
Between Skew Points	Proposed Maximum Skew (ns)	Proposed Maximum Skew for 800GBASE-R PCS lane (UI)
PCS Tx to SP1	15	≈ 398
SP6 to PCS Rx	8	≈ 611

Existing **Proposed**

Thank You!

Backups

Skew Points – 802.3df/D1.1



800GAUI-n = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
q=32
m=8
n=8
p=8

Figure 169–5—800GBASE-R Skew points for a PHY with multiple 800GAUI-n

Existing Skew Constraints – 802.3df/D1.1

Table 169–5—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 800GBASE-R PCS lane (UI)[b]	Notes[c]
SP1	29	≈ 770	See 173.4.3
SP2	43	≈ 1142	See 173.4.3, 124.3.2, 162.6.2, 163.6.2, 167.3.2
SP3	54	≈ 1434	See 173.4.3, 124.3.2, 162.6.2, 163.6.2, 167.3.2
SP4	134	≈ 3559	See 173.4.3, 124.3.2, 162.6.2, 163.6.2, 167.3.2
SP5	145	≈ 3852	See 173.4.3, 124.3.2, 162.6.2, 163.6.2, 167.3.2
SP6	160	≈ 4250	See 173.4.3
At PCS receive	180	≈ 4781	See 172.2.5.1

[a] The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b] The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 37.64706 ps at PCS lane signaling rate of 26.5625 GBd.
[c] Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.