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IEEE P802.3dg Next-Level PHY Considerations for 100BASE-T1L

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Introduction

- This presentation covers some considerations for the definition of the PHY line coding for 100BASE-T1L
- This presentation asserts that we need to take into consideration the overall context of not just the PHY and channel but also the interaction with the power components
- The presentation outlines the work, the analysis and methodology that we can employ to provide the task force with the data that will help make the PHY line coding decisions

100BASE-T1L PHY Performance Design Target

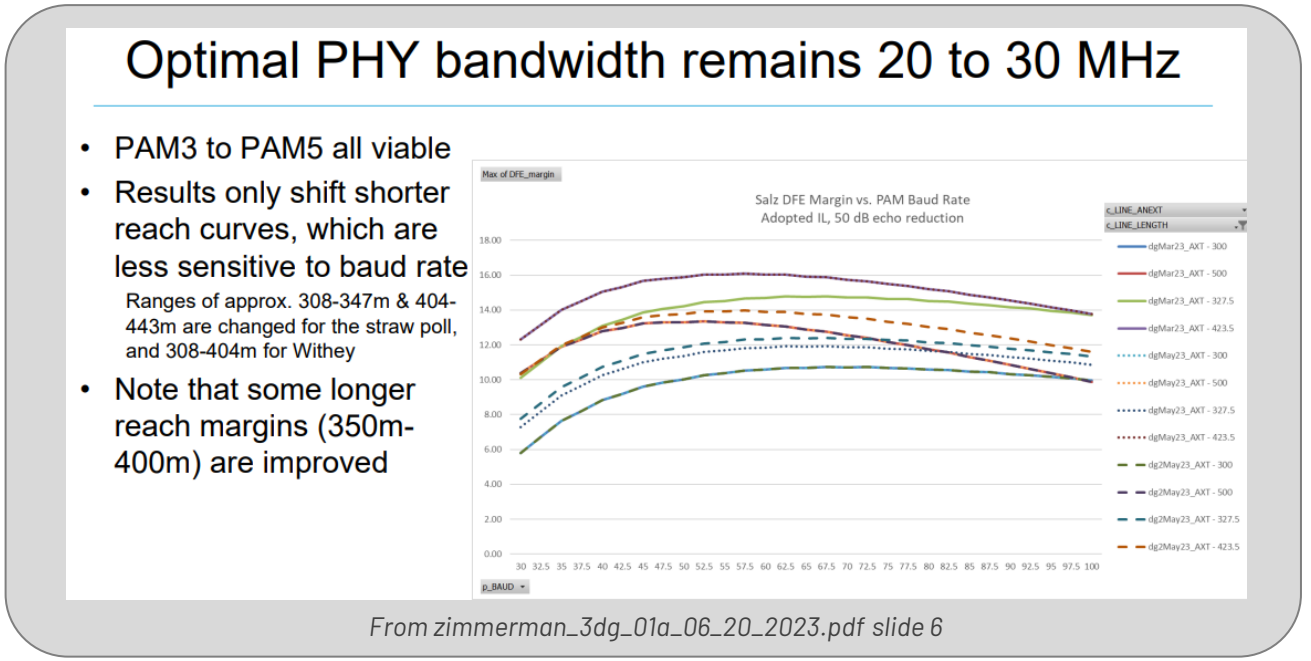
- The 802.3dgTF has agreed the following objectives for 100BASE-T1L
  - 100 Mb/s, full-duplex, point-to-point in industrial environments
  - At least 500m reach supporting 5 inline connectors over single pair cable
    - The standard will define **Insertion Loss**, **Return Loss**, **PSANEXT**, **PSAACR-F**, **Delay**
    - May include a requirement for **Coupling Attenuation** or **Shielding**
    - At present looks like at 18 gauge or 16 gauge cable to meet 500 m
  - Supporting power on the same pair, e.g. SPoE
  - Supporting Intrinsically Safe devices and systems
  - Supporting Fast-Startup
    - For the PHY this is time to complete Auto-Neg and PHY link-up time
  - Supporting a low latency mode for shorter reach application
- Market expects the following features
  - Low power, low latency and low cost

Reference Comparison with Previous BASE-T PHYs

- For context we can compare this with previous BASE-T PHYs
  - 10BASE-T1L
    - 10M full-duplex over 1000 m of single pair cable with 10 inline connectors
      - In practice used 18 gauge cable and achieved > 2000 m depending on the noise
    - 7.5 MSym/s PAM-3 4B3T line coding with running disparity to control DC balance
    - Controller/Responder timing with echo cancellation and equalization
  - A host of previous BASE-T PHYs have led the way with very similar architectures
    - 100BASE-TX (MLT-3 with 8B10B), 1000BASE-T (PAM-5 with 4D code), 100BASE-T1 (PAM-3 with 3B2T & 4B3B), 1000BASE-T1 (PAM-3 with 3B2T & 80B81B), 10GBASE-T (PAM-16 with DSQ128 code)
    - All except 100BASE-TX are Controller/Responder timing with echo cancellation, equalization, scramblers, PCS encoding, etc.
- This is a well worn and well understood path

802.3dg Presentations on SNR Analysis

- We have had a number of 802.3dg presentations on the SNR Analysis of the channel and resulting encoding that can achieve 100M at up to 500 m; for example:
  - graber_GT10MSPE_01_11082021.pdf
  - Tingting_3dg_01_18_01_2023.pdf
  - zimmerman_3dg_01a_06_20_2023.pdf



From zimmerman_3dg_01a_06_20_2023.pdf slide 6

- All show that we can use PAM-3 or PAM-4 or PAM-5
  - No clear cut winner between these based on 1st order SNR Analysis
- Some presentations have explored the option of using FEC

802.3dg Presentations on the Channel Specification

- We have had a number of 802.3dg presentations on the Channel Specification
  - graber_3dg_02_03152023.pdf
  - Fischer_3dg_01a_05172023.pdf
  - tellas_3dg_01a_06_20_2023.pdf

- Based on the 1st order analysis we are making good progress on the Channel Specification

Link Segment Transmission Models

- Insertion Loss: (graber_3dg_02_03152023 slide 4)
  $5.42*SQRT(f_{MHz})+0.044*f_{MHz}+1.76/SQRT(f_{MHz}) + 5*0.02*SQRT(f_{MHz})$
- Return Loss: (graber_01_03152023 slide 13)
  $9+8* f_{MHz}$ dB ($f_{MHz} < 0.5$ MHz) , 13 dB ($0.5 \le f_{MHz} < 20$ MHz)
  $13-10*LOG10(f_{MHz}/20)$ ($20 \le f_{MHz} \le 100$ MHz)
- PSANEXT, PSAACR-F: (graber_03a_03152023.pdf slide 10)
  - PSANEXT: $50 + 5*N$ dB, ($f_{MHz} < 10$ MHz), $50 + 5*N - 15*LOG10(f_{MHz}/10)$ (10 MHz $\le f_{MHz}$)
    - N = 0 for *IL(20 MHz)* < 16 dB, N = 0.4*(for 16 dB ≤ *IL(20 MHz)* < 21 dB, N= 2 for 21 dB ≤ *IL(20 MHz)*
  - PSAACR-F: $50 + 5*N$ dB, ($f_{MHz} < 2$ MHz), $36 + 5*N - 20*LOG10(f_{MHz}/10)$ (2 MHz $\le f_{MHz}$)
    - N = 0 for *IL(20 MHz)* < 16 dB, N = 1 for 16 dB ≤ *IL(20 MHz)* < 21 dB, N= 2 for 21 dB ≤ *IL(20 MHz)*
- *Proposal modifies N in the mid range, from about 310m to about 405m*

From zimmerman_3dg_01a_06_20_2023.pdf slide 5

- Clearly PHY performance is dependent on the channel
  - More details analysis of PHY performance and the line coding options may result in some iterations here

PHY Line Coding and Channel Decisions

- In the task force we have had good convergence towards the specification of the channel
  - But it is also clear based on voting on motions that we don't have all the information we need and not everyone is ready to make decisions here
- In the task force we have had very good 1st order SNR analysis on the channel and line coding options which has given us a very good bound on the range of options
- We now need to get to a 2nd order analysis to make a decision

Analysis Required to make PHY Line Code Decisions

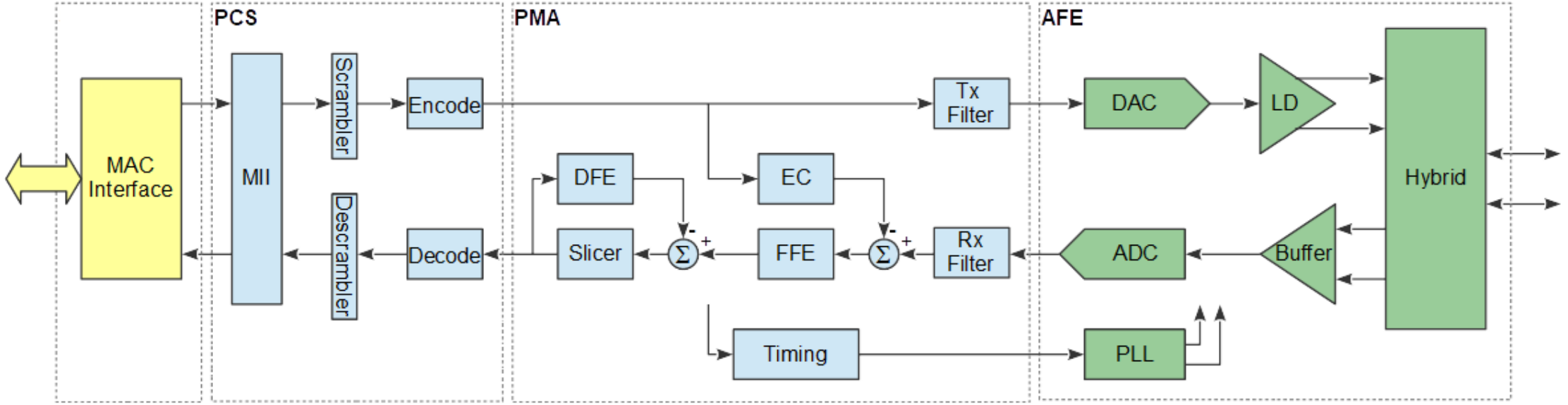
- How do we decide on the line coding?
  - PAM-3 or PAM-4 or PAM-5 and PCS encoding
- What work / analysis do we need to do?
  - What methodologies do we employ for that work?
- What results do we need to enable the Task Force to decide

What are the Trade-Offs

- Reach v Performance
  - BER and SNR margin over 0 to 500 m
  - In presence of AWGN and EFT
- Cost/Complexity: PHY power, analog performance needed, digital gates
- Impact on SPoE: External component cost

Standard BASE-T PHY Architecture

- The following is a generic block diagram of a BASE-T PHY architecture
  - Comparable with many previous Task Force presentations, see notes for examples
  - There are 3rd order implementation differences, driven by vendor differentiation
  - But these won't impact our 2nd order analysis



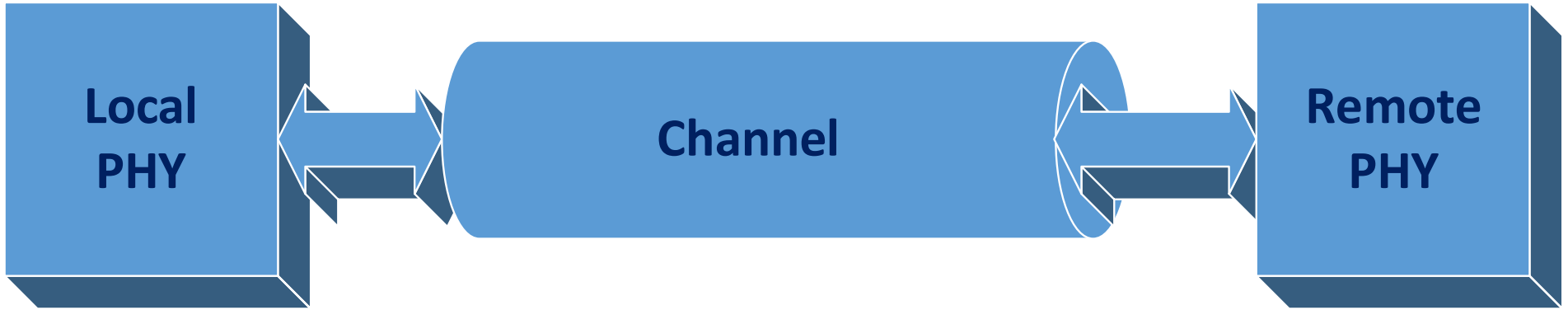
Other example PHY architecture diagrams
10BASE-T1L .cg Jan 2017 Graber_10SPE_10_0117.pdf slide 4

Generic Model of 100BASE-T1L PHY and Channel

- A generic PHY architecture and channel model allows us to construct a local and remote PHY with a channel
- This can be a simulation model or it can be a hardware emulation
  - A simulation model has the advantage that you can explore a huge number of permutations of channels and architecture details and analog parameters
  - For the 2nd order analysis we need both are valid approaches
- With this approach we get a much more accurate measure of the actual BER / SNR margin performance verses reach on the corresponding channel parameters being considered
  - Estimates of analog requirements and digital complexity can be validated
  - Analysis of the impact on the PoDL external components can be validated

Generic Model of 100BASE-T1L PHY and Channel

- A time domain simulation of local PHY a channel and remote PHY is run for a range of channel parameters / cable lengths
  - Generates BER and SNR data against reach



Complexity of SPoE verses PoE

- In PoE where we have 2-pairs, power is applied at the center tap of the transformers
  - Positive to one transformer pair and negative to the 2nd transformer
  - Hence, half of the current flows in each of the wires in the pair, travelling in the same direction on both wires
    - So down from the center tap on one half of the winding and up on the other half of the winding
  - Hence the flux cancels and thus the cost of an inductor the required OCL is reasonable
- In SPoE we only have a single pair and the current has to travel in opposite directions on each wire
  - So the current travels in the same direction in both halves of the winding
  - And the magnetic flux adds and the result is that the cost and size of an inductor with the same OCL as PoE is much higher
    - This is so that we avoid saturation in the inductor
    - For reference previous IEEE presentations have discussed the trade-off of inductor size and OCL in more detail, see for example Stewart_3dd_01_09072021.pdf and paul_01_da_120220.pdf

Impact of Droop on the Inductor Size for SPoE

- In any baseband signaling, even using scramblers and encoding there are sequences of symbols of the same sign
  - DC content cannot get through the transformer or capacitor coupling, resulting in droop or Base Line Wander (BLW)
  - Ideally in any given window we minimize the length of these runs
  - Even a well design scrambler has low probability events with specific sequences
- The PHY transmitter and Receiver must allow for extra signal range to account for BLW
  - In some BASE-T PHYs these effects can double the required signal range
  - On the PHY receiver side this cost is in lost SNR – which is even more important than gates or bits because you can't get it back
- The lower the inductance (OCL) the greater this effect for a given sequence length
- Controlling the running disparity is a method to limit the length of the sequence of symbols of the same sign, reducing BLW
- Running disparity allows us to use lower OCL inductors in SPoE results in lower cost and smaller size inductors!

Consider SPoE and PHY Encoding at the Same Time

- The key here is to include the consideration of SPoE up front in the definition of the PHY line code
- As an example in 10BASE-T1L, we ended up having to revisit the issue of droop and the external components for SPoE after .cg was closed
  - Presentations to 802.3dd to address 10BASE-T1L droop – **after the fact**
  - Stewart_3dd_01_09072021.pdf
  - Murray_3dd__01b_03082022.pdf
  - Brychta_3dd_01_03082022.pdf
- This time lets figure these issues out in parallel

10BASE-T1L used 4B3T PCS Encoding

- A major innovation introduced in 10BASE-T1L was the PCS encoding that controlled the running disparity
- This was introduced for Intrinsic Safety so the signal amplitude could be guaranteed
  - Relying on a scrambler can only reduce the probability of long sequences
- As discussed controlling the running disparity is also a significant benefit to the PHY
- The 4B3T PCS encoding in 10BASE-T1L ensures the disparity is bounded by +/-3
  - 4B3T encodes 4-bits into 3 x PAM-3 symbols
  - There are 27 permutations of 3T symbols
    - Pair positive / negative disparity with a single code
    - Use (0,0,0) for COMMA code
    - Use the other 16 for the 4-bit mapping

PAM-3 with 4B3T					
No of +/- in Sequence	Sum 0	Sum ±1	Sum ±2	Sum ±3	Total
0	1				
1		3			
2	6		3		
3		3		1	
Sub-Totals	7	6	3	1	17
Bits/Symbol = 1.33	6	6	3	1	16

- One option for 100BASE-T1L is to use the same PAM-3 4B3T encoding scheme at 75 MSym/s
  - Note, that a standard PAM-3 3B2T scheme would be 66.6 MSym/s - so it was very small cost in symbol rate

PAM-5 8B4T Encoding Options

- Following the same methodology and approach a running disparity scheme can easily be developed for PAM-5 coding
- We can map 4 PAM-5 symbols into 8 bits for a 8B4T encoding

PAM-5 with 8B4T										
	Sum 0	Sum ±1	Sum ±2	Sum ±3	Sum ±4	Sum ±5	Sum ±6	Sum ±7	Sum ±8	Total
No of Sequences	85	160	136	104	70	40	20	8	2	625
Pairs	85	80	68	52	35	20	10	4	1	355
Sub-Totals	**85**	**80**	**68**	**52**						**285**
Bits/Symbol = 2	**84**	**80**	**68**	**24**						**256**

- This results in a maximum disparity of +/-3
- Another option for 100BASE-T1L is to use a PAM-5 8B4T encoding scheme at 50 MSym/s

Summary

- Good progress has been made in the task force on the first level of analysis on the PHY line coding and channel specification
- We have a reasonable bound on good options to be considered
- A time domain simulation and 2nd level analysis will provide more accurate results for reach verses BER performance
- This will gives us the data that the task force can consider for the trade-offs with the different approaches