

Consideration on the PHY Baseline for 802.3dg

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Introduction

- Both [zimmerman 3dg 01a 03 15 2023.pdf](#) and [Tingting 3dg 01a 15032023.pdf](#) have shown that the consensual link segment parameters insertion loss, return loss, and crosstalk, provide enough SNR margin to PHY design for trunk application. It is time to discuss PHY major features including PCS coding, FEC, bit-to-symbol mapping, and scrambling etc. for the trunk.
- We need to answer the following two questions before designing PCS and PMA for 802.3dg:
 - Is FEC necessary? Measurement of EFT noise needs to be done in order to obtain accurate evaluation.
 - Will 200m spur be added to 802.3dg? If so, strictly controlled disparity is required. Blocking coding may be different from the case without spur.
- Anyway, it can be summarized into three possible situations:
 - FEC is not required, regardless of spur in 802.3dg.
 - FEC is required, and only trunk is considered in 802.3dg.
 - FEC is required, and spur application is also covered by 802.3dg.
- In this presentation, we give our preliminary consideration on the PHY baseline for all the three cases.

In case FEC is not required

- In 802.3cg for 10BASE-T1L, link segment and PHY parameters of spur enables it achieve similar SNR margin as the trunk. We can follow the same design rule for 802.3dg. In such way, similar performance and noise environment make trunk and spur agree on the requirement of FEC.
- If FEC is not required, 802.3dg can reuse the PCS and PMA of 10BASE-T1L for both trunk and spur. This will significantly accelerate 802.3dg project.
- Flexible data rates (e.g. 25Mbps, 50Mbps) between 10Mbps and 100Mbps may be considered as new features of 802.3dg, since the throughput growth of trunk or spur is much slower than that of data center.

In case FEC is required

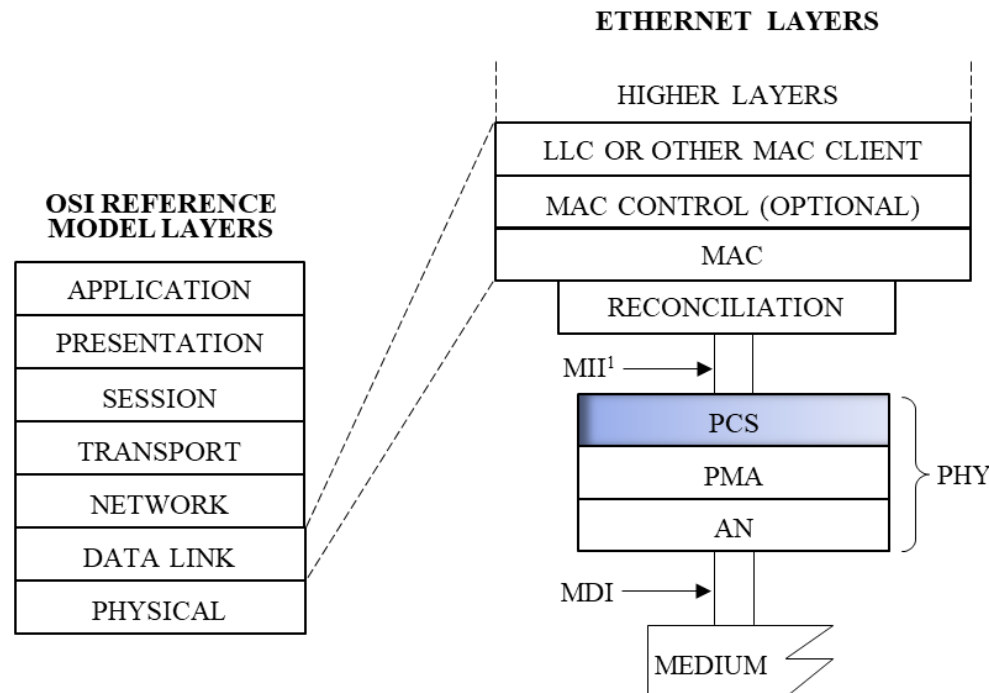
- PAM3, PAM4, and PAM5 are all viable for the trunk, based on the consensual link segment parameters.
 - PAM4 allows simple bit-to-symbol mapping.
 - PAM3 requires block coding. Generally, the coding efficiency and complexity increases with block size.
 - PAM5 is only used in 1000BASE-T. TCM is too complicated for 802.3dg with reasonably large bandwidth.
- With coding efficiency, complexity, and compatibility taken into account, **PAM3 and PAM4 are better candidates for 802.3dg.**
 - If 802.3dg only focuses on the trunk, 3B2T providing high coding efficiency with lowest complexity, is the best choice for PAM3.
 - If spur is included in 802.3dg, block coding with strictly limited disparity is required. 4B3T may be the right choice for PAM3, and 8B/10B can be considered for PAM4.

Block Coding	Efficiency
3B2T	94.64%
4B3T	84.12%
7B5T	88.33%
10B7T	90.13%
11B7T	99.15%
19B12T	99.9%

Application	Coding and Format	FEC	BER Requirement
10BASE-T1L	4B3T PAM3	No	10^{-10}
100BASE-T1	4B3B, 3B2T PAM3	No	10^{-10}
1000BASE-T1	80B/81B, 3B2T PAM3	RS-FEC (450, 406, 2^9)	10^{-10}
1000BASE-T	8B1Q4, 4D-PAM5	4D-8 State Trellis Code	10^{-10}
MultiGBASE-T1	64B/65B, PAM4	RS-FEC (360, 326, 2^{10})	10^{-12}

In case FEC is required (Cont.)

- PCS function blocks mainly include PCS transcoding, FEC, and scrambling.
 - PCS transcoding enables data signal distinguished from control information, and labels the start and the end of MAC frame.
 - FEC ensures low frame error rate after error correction.
 - Scrambling randomizes the data stream, whitens emission spectrum by avoiding undesired spurs. The induced high transition density also enables easy CDR.
- FEC for 802.3dg may lie within the PCS layer. For latency-sensitive motor feedback communication and other situations (e.g. low insertion loss and low crosstalk), FEC is not required and can be bypassed through auto-negotiation or management interface.



PCS Transcoding

- PCS transcoding used in IEEE 802.3 standards include 4B/5B, 8B/10B, 64B/66B, and $8n/8n+1$ (e.g. 64B/65B, 80B/81B, 256B/257B etc.).
- For $8n/8n+1$ coding, the overhead decreases with the increment of block size, at the cost of increased complexity.
- Considering the tradeoff between overhead and complexity, PCS transcoding can be chosen from 64B/66B, 64B/65B, and 80B/81B.
- If 802.3dg covers both trunk and spur, coding with strictly limited disparity (such as 4B3T or 8B/10B) is required. The induced low coding efficiency biases the use of 64B/65B or 80/81B with relatively low overhead.

Thoughts on FEC

- The key driving force for FEC in 802.3dg is to correct burst errors, which can be induced by DFE, ringing, and EMI. TCM used in 1000BASE-T has poor tolerance to burst errors. Reed-Solomon FEC is a better choice and has been widely deployed in 802.3 standards.
- As specified by IEC61000-4-4, the fastest burst rate can reach 100 kHz (10 μ s). Therefore, FEC with small block size (<1000 bits) only gets one burst.
- FEC overhead, coding gain, burst error protection time, latency, complexity, and re-use are main concerns for FEC design. Single burst duration of 50ns requires burst error correction larger than 5 bits for 100BASE-T1L.
 - Interleaving is not required, as there exist many eligible FEC code words, meeting the requirements.
- Considering that FEC decoding is performed after block decoding (e.g. 3B2T, 4B3T, or 8B/10B), bits per symbol of RS FEC can be chosen to match the block size.
 - RS FEC can be in $GF(2^6)$ or $GF(2^9)$ for 3B2T PAM3, while $GF(2^8)$ for 4B3T PAM3.
 - For PAM4 with 8B/10B, RS FEC can be in $GF(2^8)$. $GF(2^6)$ may be also considered if 8B/10B is not required (i.e. only trunk covered by 802.3dg).

Scrambling

- Scramblers in 802.3 standards can be classified into self-synchronization (commonly use 58-bit polynomial) and side-stream scrambler. Compared with self-synchronizing scrambling, side-stream scrambler avoids the error multiplication problem but requires accurate frame sync.
 - Self-synchronizing scrambler with 58-bit polynomial has been widely deployed in MultiGBASE-T and MultiGBASE-R.
 - 33-bit side-stream scrambler is mainly used in full-duplex single pair Ethernet from 10Mbps to 25Gbps, covering EMC-sensitive applications (e.g. industry and automotive).
- 33-bit side-stream scrambler is a good choice for 802.3dg. To meet EMC requirement, scrambling can be implemented after FEC pre-coding, while descrambling before FEC decoding.

Application	Scrambler Polynomial		Scrambler Type
10BASE-T1L	Master: $1+x^{13}+x^{33}$, Slave: $1+x^{20}+x^{33}$		side-stream scrambler
100BASE-T1	Master: $1+x^{13}+x^{33}$, Slave: $1+x^{20}+x^{33}$		side-stream scrambler
1000BASE-T1	Training Mode: Master: $1+x^{13}+x^{33}$ Slave: $1+x^{20}+x^{33}$	Data Mode: Master: $1+x^4+x^{15}$ Slave: $1+x^{11}+x^{15}$	side-stream scrambler
MultiGBASE-T1 (802.3ch)	Master: $1+x^{13}+x^{33}$, Slave: $1+x^{20}+x^{33}$		side-stream scrambler
1000BASE-T	Master: $1+x^{13}+x^{33}$, Slave: $1+x^{20}+x^{33}$		side-stream scrambler
MultiGBASE-T	Master: $1+x^{39}+x^{58}$, Slave: $1+x^{19}+x^{58}$		self-synchronizing scrambler
MultiGBASE-R	Master: $1+x^{39}+x^{58}$, Slave: $1+x^{19}+x^{58}$		self-synchronizing scrambler

Conclusion

- With coding efficiency, complexity, and compatibility taken into account, PAM3 and PAM4 are good candidates for 802.3dg.
- If FEC is not needed, 802.3dg can reuse the PCS and PMA of 10BASE-T1L. Flexible data rates may be considered as the new feature for 802.3dg.
- In case FEC is required, RS FEC is a good choice. The PCS transcoding, block coding or bit-to-symbol mapping depends on whether spur is included in 802.3dg.
 - For only trunk, 3B2T PAM3 or PAM4 with PCS transcoding chosen from 64B/66B, 64B/65B, and 80B/81B can be considered.
 - If spur is included, block coding with strictly bounded disparity (e.g. 4B3T or 8B/10B) is required. 64B/65B and 80B/81B with lower overhead and acceptable complexity are better.
 - Interleaving is not required, as there exist many FEC code words (<1000 bits) providing burst error correction larger than 5 bits. Apart from FEC overhead, coding gain, latency, and complexity, block coding (3B2T, 4B3T, 8B/10B) also needs to be taken into account for RS FEC design.
- 33-bit side-stream scrambler is a good choice for 802.3dg.

Thank you!