Thoughts on the new MII

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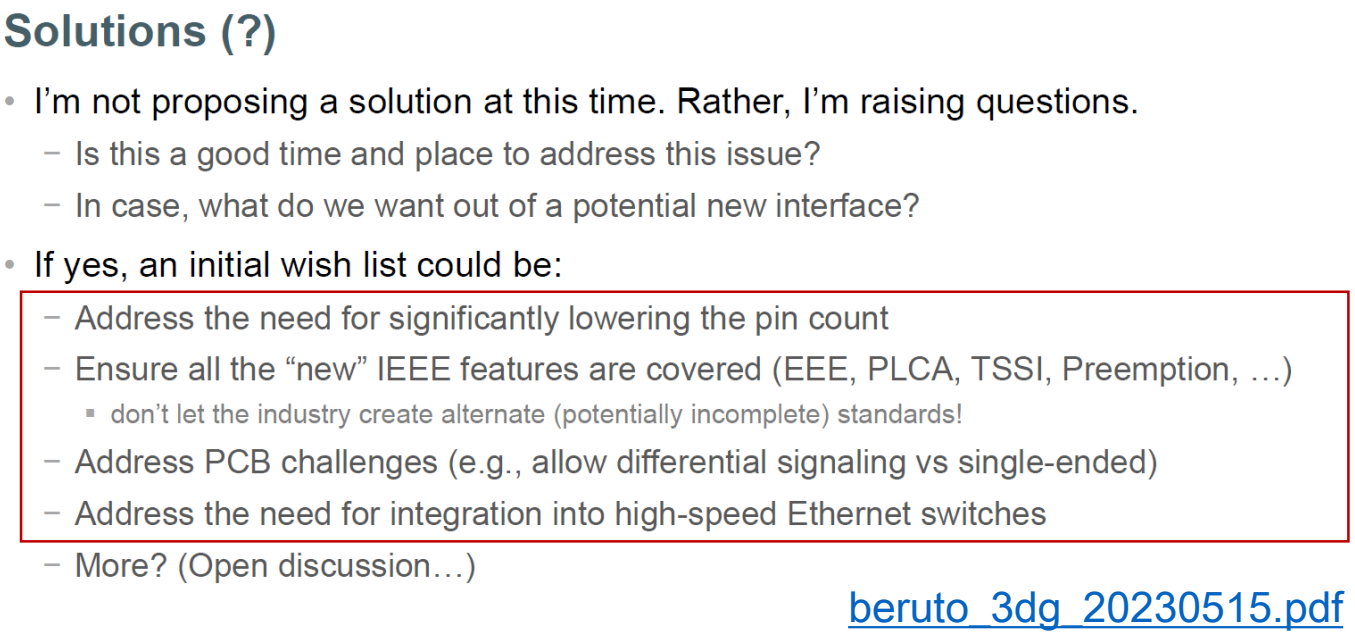
Goal of this presentation

- Piergiorgio Beruto has presented the problems and opportunities in today's MAC/PHY interface for SPE application (beruto_3dg_20230515.pdf).
- This presentation shows some preliminary thoughts on the MII interface for 802.3dg. It is NOT a MII baseline proposal.
  - Serdes technology can be a good solution to significantly reduce the pin count.
  - Supporting the "new" IEEE features (PLCA, EEE, ….) can be realized by using specific code groups of block coding (e.g. 4B/5B, 8B/10B).
  - Differential signals may be preferred for high-speed scenarios due to the performance advantage.
  - The MII interface supports multiple low-speed SPE PHYs connect to a high-speed Ethernet switch interface.



Solutions (?)

- I'm not proposing a solution at this time. Rather, I'm raising questions.
  - Is this a good time and place to address this issue?
  - In case, what do we want out of a potential new interface?
- If yes, an initial wish list could be:
  - Address the need for significantly lowering the pin count
  - Ensure all the "new" IEEE features are covered (EEE, PLCA, TSSI, Preemption, …)
    - don't let the industry create alternate (potentially incomplete) standards!
  - Address PCB challenges (e.g., allow differential signaling vs single-ended)
  - Address the need for integration into high-speed Ethernet switches
  - More? (Open discussion…)

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MII interface with a high pin count

- The parallel MII interface requires 18 pins (including management pins), while pins are valuable resource.

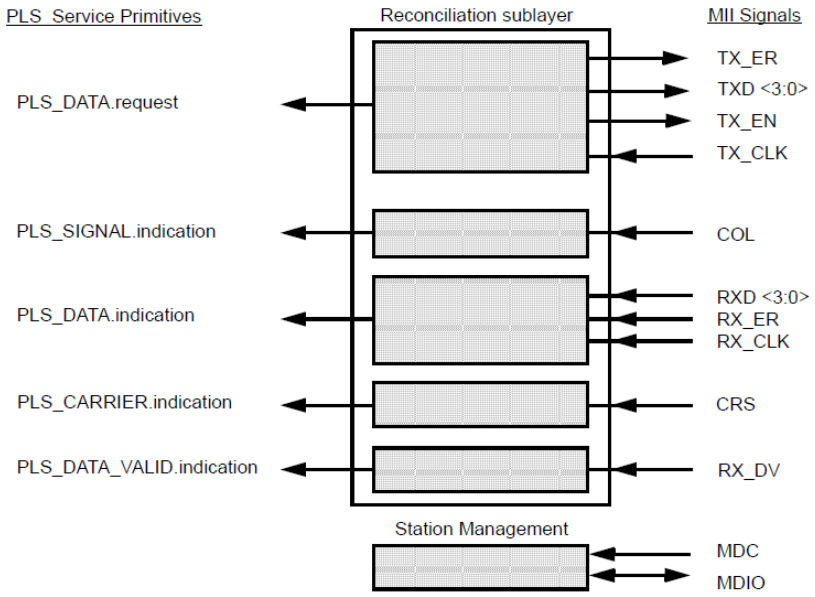
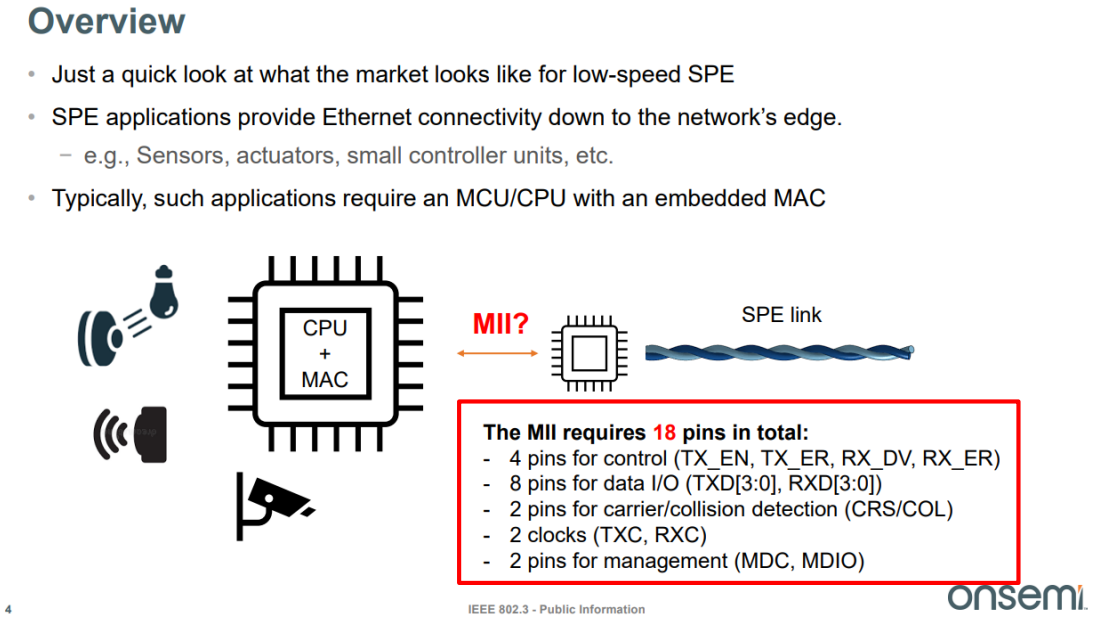


Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

Source: IEEE Std 802.3



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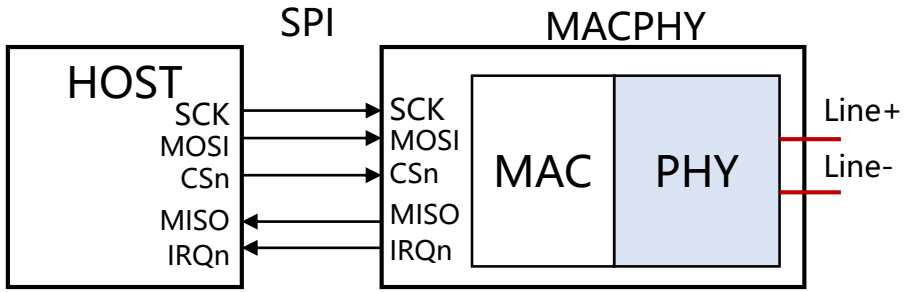
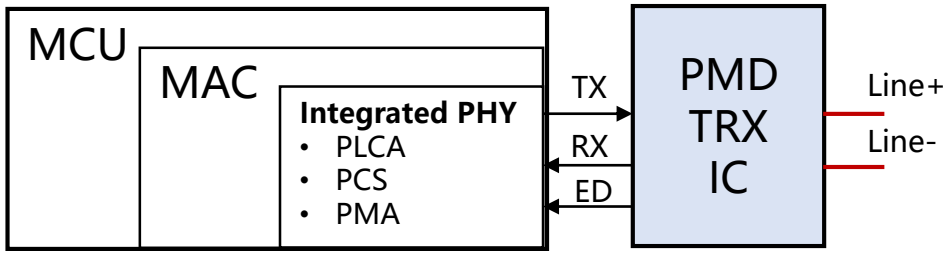
Practical solutions to reduce the pin count

- **MACPHY SPI** supports both data (Ethernet frames) and control (register access) transactions over a single serial peripheral interface, reducing the original pin count from 18 to 5.
  - It is not the MII interface.
  - Increasing SPI from current 10 Mbps to 100Mbps may be challenging, due to increased sensitivity to CM interference.
- **PMD transceiver interface**: the transceiver retains the analog part, while the digital portion of the PHY is integrated into MCU or switch core. Only 3 pin is required.
  - This interface is similar to the RS-485 or CAN solution, not the MII interface, and is for 10BASE-T1S only.



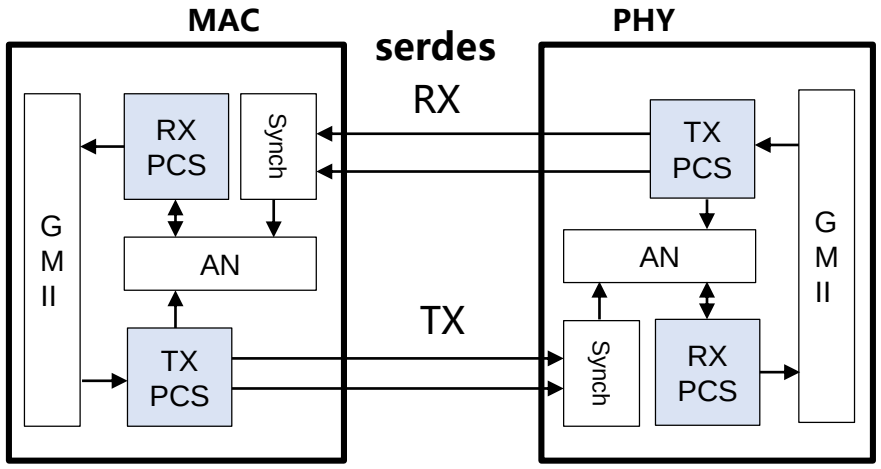
Block diagram of OPEN Alliance 10BASE-T1x MAC-PHY SPI



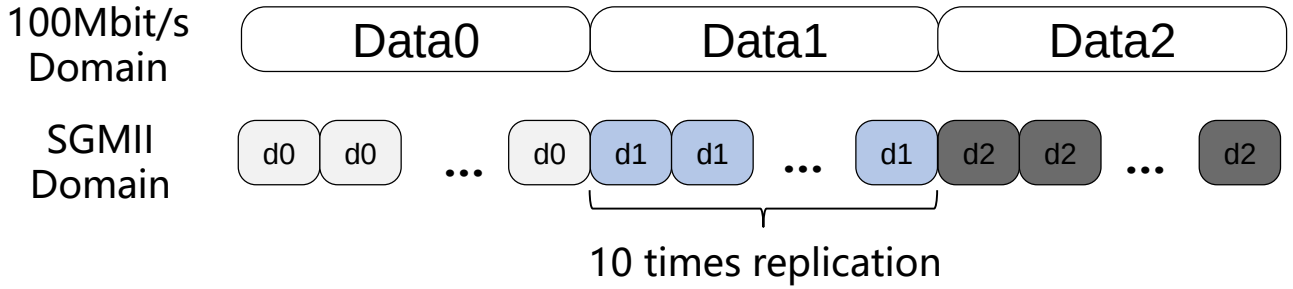
Block diagram of OPEN Alliance 10BASE-T1S PMD Transceiver Interface

Considerations may be needed for SGMII on SPE

- SGMII based on 802.3z utilizes 4 pins to transmit and receive serial differential signal, allowing line rate up to 1.25Gbps.
- To match low-speed SPE PHY, SGMII replicates each frame byte by multiple times (e.g. 10/100 times for 100M/10M), while the line rate between MAC and PHY keeps 1.25G.
- Further power consumption and complexity reduction may be required, especially for embedded systems.

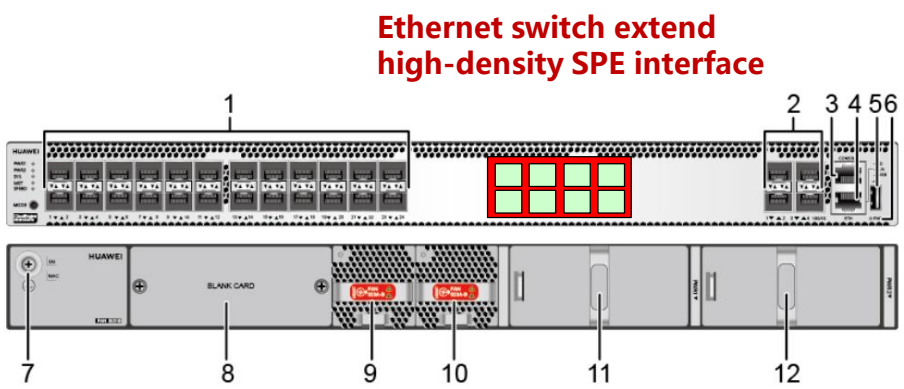


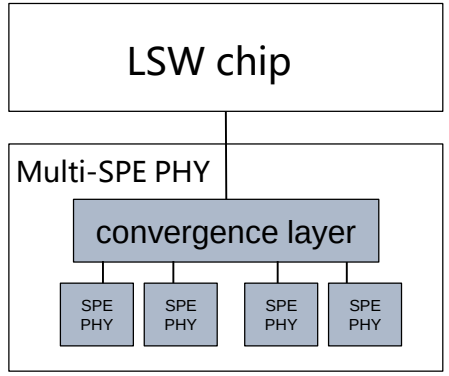
Block diagram of SGMII



To support multi-SPE PHY

- "Normal" Ethernet switch chip supports 12, 24, ... PHYs with high-speed interfaces. If a single MII interface supports multiple low-speed SPE PHYs, the switch chip can use a few high-speed interfaces to realize high-density access.
- QSGMII allows quad PHYs connect to a single multiplexed high-speed link, yet resulting in different PHY types.
- The new MII solution is better to support independent PHYs implementation, consequently reduce the PHY volume.





Conclusions

- The parallel MII interface has a large number of pins and is not widely used in practice.
- There are non-MII interfaces (MACPHY SPI, PMD transceiver interface) with lower pins in the industry, which are usually used in low-speed or dedicated applications.
- Compared with the aforementioned schemes, serialized MII interface deploying differential signals is more attractive, and the industry has already done so (e.g. SGMII). However, power consumption and complexity reduction may be needed for embedded systems.
- The MII supporting multiple low-speed SPE PHYs enables better adapt to high-speed Ethernet switching chip interfaces, and expands high-density SPE interfaces.

Thank you!